Automotive Fault-Protected CAN FD Transceiver with Signal Improvement Capability and Standby Mode

1. Descriptions

MCAN1462 is a member of the MCAN146x family of transceivers that provides CAN Signal Improvement Capability (SIC) function to significantly reduce signal ringing in a complex network. MCAN1462 can be viewed as a simple replacement for MCAN1044. It is pin compatible and is easily to replace MCAN1044 without any hardware and software changes. MCAN1462 family meets the ISO11898-2(2016) High Speed CAN (Controller Area Network) physical layer standard. All devices support CAN FD networks up to 10 Mbps (megabits per second). Devices with the "V" suffix part numbers have a secondary power supply input for I/O level shifting the input pin thresholds and RXD output level. These devices have a low power standby mode for remote wake request feature. Additionally, all devices incorporate several protection features to enhance device and network robustness.

2. Application

- Automotive and Transportation
  - Body Electronics / Lighting
  - ADAS / Safety/ Infotainment applications

3. Features

- AEC-Q100 Grade 1
- Implements Signal Improvement Capability (SIC), as defined in CiA 601-4
- Meets the ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards
- Support classic CAN and CAN FD up to 10 Mbps
- Operating Mode：Normal mode and Standy mode
- Ideal passive behavior when unpowered
- I/O Voltage range supports 3.3 V and 5 V MCUs
- Protection features
  - Bus Fault protection: ±58 V
  - Under-voltage protection on V_{CC} and V_{IO} (V variants only) supply terminals
  - Driver dominant time out (TXD-DTO)
  - Data rates down to 4 kbps
- Thermal shutdown protection (TSD)
- Receiver common mode input voltage: ±30 V
- Typical loop delay: 110 ns
- Junction temperatures from –40°C to 150°C
- Available in SOP-8 package and leadless DFN3*3 package

4. Typical Application Diagram

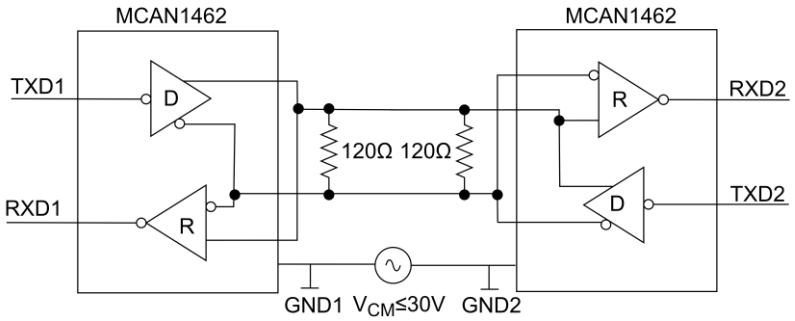


Figure 1. Typical Application Diagram

5. Order Information

Part Number	Package Type	Package Qty	Eco Plan	MSL	VIO Function
MCAN1462XAB-Q1	SOP-8	4k/ reel	RoHS & Green	MSL-1	Not Support
MCAN1462VXAB-Q1	SOP-8	4k/ reel	RoHS & Green	MSL-1	Support
MCAN1462XDB-Q1	DFN3*3	3k/ reel	RoHS & Green	MSL-2	Not Support
MCAN1462VXDB-Q1	DFN3*3	3k/ reel	RoHS & Green	MSL-2	Support

6. Pin Configuration and Functions

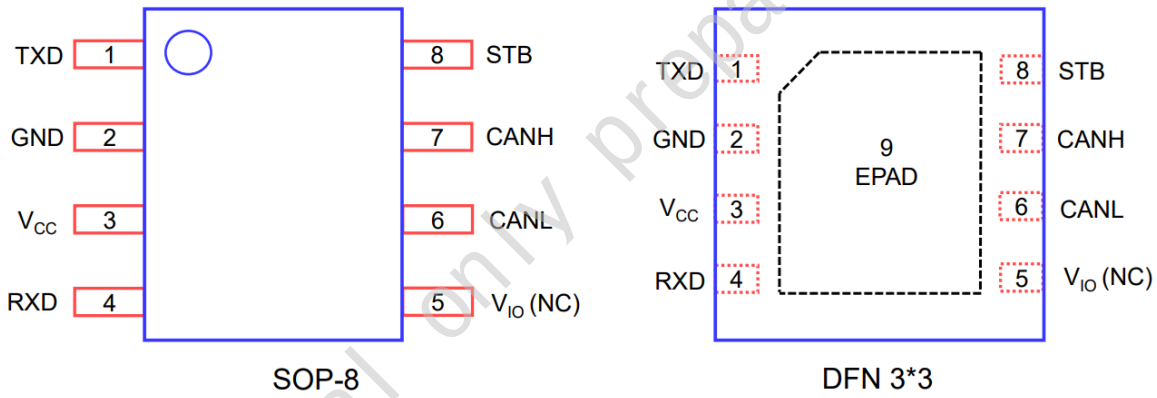


Figure 2. Pin Function (top view)

Table 1. Pin Functions

Pin			I/O	Description
Number	Name	'V' version Name		
1	TXD		Digital Input	CAN transmit data input
2	GND		GND	Ground
3	V_{CC}		Power	Transceiver 5-V supply voltage
4	RXD		Digital Output	CAN receive data output
5	NC	—	—	No Connect
5	—	V_{IO}	Power	Transceiver I/O level shifting supply voltage (Devices with "V" suffix only)
6	CANL		Output	Low level CAN bus input/output line
7	CANH		Output	High level CAN bus input/output line
8	STB		Digital Input	Standby Mode control input (active high)
9	—	EP	GND	Exposed PAD, connect to GND to enhance the thermal performance

7. Specifications

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
V_{CC}	5-V bus supply voltage range	–0.3	6	V
V_{IO}	I/O Level Shifting Voltage Range	–0.3	6	V
V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)	–58	58	V
$V_{(Diff)}$	Max differential voltage between CANH and CANL	–58	58	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range (TXD, STB)	–0.3	6	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range (RXD)	–0.3	6	V
$I_{O(RXD)}$	RXD (Receiver) output current	–8	8	mA
T_J	Virtual junction temperature range	–40	150	°C
T_{STG}	Storage temperature range	–65	150	°C

7.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002/ANSI/ESDA/JEDEC JS-001(1)	On pins TXD, GND, VCC, RXD, VIO, STB	±6	kV
			ESD Resistivity to GND, CANH, CANL	±5	kV
			On any pin	±3	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)		±2	kV
		IEC 61000-4-2 (150pF, 330Ω discharge circuit) (3)	ESD Resistivity to GND, CANH, CANL with PESD2CANFD27L and ACT45B-2P-TL003	±30	kV

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

(3) Testing performed by OEM-approved independent 3rd party, EMC report available upon request

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	5-V Bus Supply Voltage Range	4.5	5.5	V
V_{IO}	I/O Level-Shifting Voltage Range	2.95	5.5	
$I_{OH(RXD)}$	RXD terminal HIGH level output current	-4		mA
$I_{OL(RXD)}$	RXD terminal LOW level output current		4	
T_A	Operating temperature	-40	125	°C

7.4 Thermal Information

Thermal Metric		MCAN1462		UNIT
		SOP-8	DFN 3*3	
$R_{\theta JA}$	Junction-to-air thermal resistance	98	42	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	43	10	°C/W
T_{TSD}	Thermal shutdown temperature	180	180	°C
T_{TSD_HYS}	Thermal shutdown hysteresis	20	20	°C

7.5 Electrical Characteristics

Over recommended operating conditions with T_A= -40°C to 125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Normal mode (Dominant)	R_L = 60 Ω, STB = 0 V, TXD = 0 V, C_L = open, R_{CM} = open, see Figure 3.		40	70	mA
		R_L = 50 Ω, STB = 0 V, TXD = 0 V, C_L = open, R_{CM} = open, see Figure 3.		44	80	mA
	Normal mode (Recessive)	R_L = 50 Ω, TXD = V_{IO}, STB = 0 V, C_L = open, R_{CM} = open, see Figure 3.		2.6	8	mA
	Standby mode	Devices with the “V” suffix (I/O level-shifting) R_L = 50 Ω, STB = V_{IO}, TXD = V_{IO}, C_L = open, R_{CM} = open, see Figure 3.		0.5	2	µA
		Devices without the “V” suffix (5-V only) R_L = 50 Ω, TXD = V_{CC}, STB = V_{CC}, C_L = open, R_{CM} = open, see Figure 3.		11.5	20	µA
I_{IO}	Normal mode (Dominant)	Devices with the “V” suffix (I/O level-shifting) TXD = 0 V, STB = 0 V, RXD floating.		105	200	µA
	Normal mode (Recessive)	Devices with the “V” suffix (I/O level-shifting) TXD = V_{IO}, STB = 0 V, RXD floating.		19	48	µA
	Standby mode	Devices with the “V” suffix (I/O level-shifting) TXD = STB = V_{IO}, V_{CC} = 0 or 5.5 V.		11	18	µA

UV_{VCC}	Rising undervoltage detection on V_{CC}	All devices		4.2	4.4	V
	Falling undervoltage detection on V_{CC}		3.6	4.0		V
$V_{HYS(UVVCC)}$	Hysteresis voltage on UV_{VCC}			200		mV
UV_{VIO}	Undervoltage detection on V_{IO}	Devices with the “V” suffix (I/O level shifting)	1.4		2.85	V
$V_{HYS(UVVIO)}$	Hysteresis voltage on UV_{VIO}			500		mV

STB Terminal (Mode Select Input)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IH}	High-level input voltage	Devices with the “V” suffix (I/O level shifting)	0.7			V_{IO}
	High-level input voltage	Devices without the “V” suffix	0.7			V_{CC}
V_{IL}	Low-level input voltage	Devices with the “V” suffix (I/O level shifting)			0.3	V_{IO}
	Low-level input voltage	Devices without the “V” suffix			0.3	V_{CC}
I_{IH}	High-level input leakage current	STB = V_{CC} = V_{IO} = 5.5 V.	-2		2	µA
I_{IL}	Low-level input leakage current	STB = 0 V, V_{CC} = V_{IO} = 5.5 V.	-20		-2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.5 V, V_{CC} = V_{IO} = 0 V.	-1		1	µA

TXD Terminal (CAN transmit Data Input)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IH}	High-level input voltage	Devices with the “V” suffix (I/O level shifting)	0.7			V_{IO}
	High-level input voltage	Devices without the “V” suffix	0.7			V_{CC}
V_{IL}	Low-level input voltage	Devices with the “V” suffix (I/O level shifting)			0.3	V_{IO}
	Low-level input voltage	Devices without the “V” suffix			0.3	V_{CC}
I_{IH}	High-level input current	TXD = V_{CC} = V_{IO} = 5.5 V.	-1		1	µA
I_{IL}	Low-level input current	TXD = 0 V, V_{CC} = V_{IO} = 5.5 V.	-150		-20	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{CC} = V_{IO} = 0 V.	-1		1	µA
C_I	Input capacitance			2		pF

RXD Terminal (CAN Receive Data Output)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	Devices with the “V” suffix (I/O level shifting) I_O = –4 mA, See Figure 6.	0.8			V_{IO}
		Devices without the “V” suffix I_O = –4 mA, See Figure 6.	0.8			V_{CC}
V_{OL}	Low-level output voltage	Devices with the “V” suffix (I/O level shifting) I_O = +4 mA, See Figure 6.			0.2	V_{IO}
		Devices without the “V” suffix I_O = +4 mA, See Figure 6.			0.2	V_{CC}
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V, V_{CC} = 0 V, V_{IO} = 0 V.	-1	0	1	µA

Driver Electrical Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{O(DOM)}$	Bus output voltage (Dominant)	STB = 0 V, TXD = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open, See Figure 4.	CANH	2.75		4.5	V
			CANL	0.5		2.25	V
$V_{O(REC)}$	Bus output voltage (Recessive)	TXD = V_{CC} or V_{IO}, V_{IO} = V_{CC}, STB = 0 V, R_L = open, R_{CM} = open, See Figure 4.	CANH	2	0.5*V_{CC}	3	V
			CANL	2	0.5*V_{CC}	3	V
$V_{O(STB)}$	Bus output voltage (Standby mode)	STB = V_{IO}, R_L = open, R_{CM} = open, See Figure 4.	CANH	-0.1		0.1	V
			CANL	-0.1		0.1	V
			CANH-CANL	-0.2		0.2	V
$V_{OD(DOM)}$	Differential output voltage (Dominant)	STB = TXD = 0 V,45 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open, See Figure 4.		1.4		3	V
		STB = TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open, See Figure 4.		1.5		3	V
		STB = TXD = 0 V, R_L = 2240 Ω, C_L = open, R_{CM} = open, See Figure 4.		1.5		5	V
$V_{OD(REC)}$	Differential output voltage (Recessive)	TXD = V_{IO}, STB = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open, See Figure 4.		-12		12	mV
		TXD = V_{IO}, STB = 0 V, R_L = open, C_L = open, R_{CM} = open, See Figure 4.		-50		50	mV

V_{SYM}	Output symmetry (Dominant or Recessive)	TXD = V_{IO}, STB = 0 V, R_L = 60 Ω, C_{split} = 4.7 nF, C_L = open, R_{CM} = open, TXD = 250kHz, 1Mhz See Figure 4.	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry	STB = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open, See Figure 4.	-0.4		0.4	V
$I_{OS(SS\_DOM)}$	Short-circuit steady-state output current, dominant, Normal mode	STB = 0 V, V_{CANH} = -15 V to 40 V, CANL = open, TXD = 0 V, See Figure 4.	-115		115	mA
		STB = 0 V, V_{CANL} = -15 V to 40 V, CANH = open, TXD = 0 V, See Figure 4.	-115		115	mA
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current, recessive, Normal mode	STB = 0 V, –27 V ≤ V_{BUS} ≤ 32 V, V_{BUS} = V_{CANH} = V_{CANL}, TXD = V_{IO}.	-5		5	mA
$R_{ID(DOM)}$	Differential input resistance in dominant phase	TXD = 0, STB = 0V.		42		Ω
$R_{ID(ACTIVE\_REC)}$	Differential input resistance in active recessive drive phase	Duration from TXD low-to-high edge to elapse of active recessive drive period		92		Ω

Receiver Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{CM}	Common mode range, Normal mode.	STB = 0 V.	-30		30	V
V_{IT+}	Positive-going input threshold voltage, Normal mode.	STB = 0 V, TXD = V_{IO}, -30 V ≤ V_{CM} ≤ +30 V.			900	mV
V_{IT-}	Negative-going input threshold voltage, Normal mode.		500			mV
V_{HYS}	Hysteresis voltage	STB = 0 V.		120		mV
V_{CM_STB}	Common mode range, Standby mode.	STB = V_{IO}, 2.95 V ≤ V_{IO} ≤ 5.5 V.	-12		12	V
		NO V_{IO}, STB = V_{CC}.	-12		12	V
$V_{IT(STB)}$	Input threshold voltage, Standby mode.	STB = V_{CC} or V_{IO}.	400		1150	mV
$V_{REC(RX)}$	Receiver recessive voltage, Normal mode	-30V ≤ VCANH ≤ +30 V, -30V ≤ VCANL ≤ +30 V, STB = 0 V	-3		0.5	V
	Receiver recessive voltage, Standby mode	-12V ≤ VCANH ≤ +12 V, -12V ≤ VCANL ≤ +12 V, STB = V_{CC} or V_{IO}.	-3		0.4	V
$V_{DOM(RX)}$	Receiver dominant voltage, Normal mode	-30V ≤ VCANH ≤ +30 V, -30V ≤ VCANL ≤ +30 V, STB = 0 V	0.9		9	V
	Receiver dominant voltage, Standby mode	-12V ≤ VCANH ≤ +12 V, -12V ≤ VCANL ≤ +12 V, STB = V_{CC} or V_{IO}.	1.15		9	V

$I_{LKG(OFF)}$	Power-off bus input leakage current	V_{CANH} = V_{CANL} = 5 V, V_{CC} = V_{IO} = 0 V.			4.8	µA
C_I	Input capacitance to ground (CANH or CANL) (3)	TXD = V_{CC}, V_{IO} = V_{CC}.		27		pF
C_{ID}	Differential input capacitance (CANH to CANL) (3)	TXD = V_{CC}, V_{IO} = V_{CC}.		13.5		pF
R_{ID}	Differential input resistance	STB = 0 V, TXD = V_{CC} = V_{IO} = 5 V, -30 V ≤ V_{CM} ≤ 30 V.	40		90	kΩ
R_{IN}	Input resistance (CANH or CANL)		20		45	kΩ
$R_{IN(M)}$	Input resistance matching	V_{CANH} = V_{CANL} = 5 V.	-1		+1	%

Device Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, See Figure 7.		110	140	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive			110	140	ns
t_{MODE}	Mode change time, from Normal to Standby or from Standby to Normal	See Figure 9.		12	30	µs
t_{WK_FILTER}	Filter time for valid wake up pattern	See Figure 13.	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Wake up timeout value	See Figure 13.	0.8		6	ms

Driver Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pHR}	Propagation delay time, high TXD to driver recessive (Dominant to Recessive)	STB = 0 V, R_L = 60 Ω, C_L = 100 pF, R_{CM} = open, See Figure 3, See Figure 4.		63	80	ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (Recessive to Dominant)			63	80	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHR} - t_{pLD}\|$)			0.2	10	ns
t_R	Differential output signal rise time			12	30	ns
t_F	Differential output signal fall time			12	40	ns
t_{TXD_DTO}	Dominant timeout	STB = 0 V, TXD = 0 V, RL = 60 Ω, CL = open, See Figure 10.	2.6		3.8	ms

Receiver Switching Characteristic

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pRH}	Propagation delay time, bus recessive input to high output (Dominant to Recessive)	STB = 0 V, $C_{L(RXD)}$ = 15 pF, See Figure 6, See Figure 7.		45	110	ns
t_{pDL}	Propagation delay time, bus dominant input to low output (Recessive to Dominant)			38	110	ns
t_R	RXD Output signal rise time			5	20	ns
t_F	RXD Output signal fall time			5	25	ns

Signal Improvement Timing Characteristics Characteristic

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{SIC\_TX\_base}$	Signal Improvement time TX-base	Time from rising edge of the TXD signal to the end of the signal improvement phase	230	340	530	ns
$\Delta t_{bit(Bus)}$	Transmitted bit width variation	STB = 0 V, RL= 60Ω, C_L=100pF	-10		10	ns
$\Delta t_{bit(RXD)}$	Received bit width variation		-30		15	ns
Δt_{REC}	Received timing symmetry		-20	-	15	ns

FD Timing Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, See Figure 6.	490		510	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns		190		210	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ =125 ns(3)		115		135	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ =100 ns(3)		90		110	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns		470		520	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns		170		220	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 125 ns(3)		95		145	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 100 ns(3)		75		125	ns
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$, See Figure 6.	-20		15	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns		-20		15	ns

	Receiver timing symmetry with $t_{BIT(TXD)}$ = 125 ns(3)		-20		15	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 100 ns(3)		-20		15	ns

Notes:

(1) All typical values are at 25 °C and supply voltages of V_{CC} = 5 V and V_{IO} = 5 V，R_L = 60 Ω.

(2) All parameters are measured at T_A = 25 °C (unless otherwise noted).

(3) Measured during characterization and not an ISO 11898-2:2016 parameter.

7.6 Parameter Measurement Information

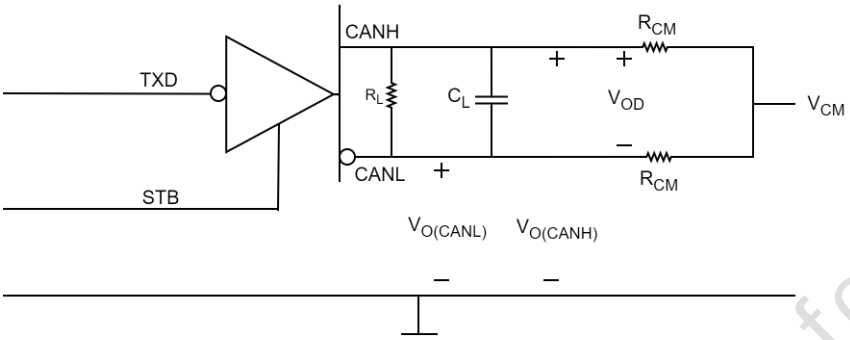


Figure 3. Driver Test circuit

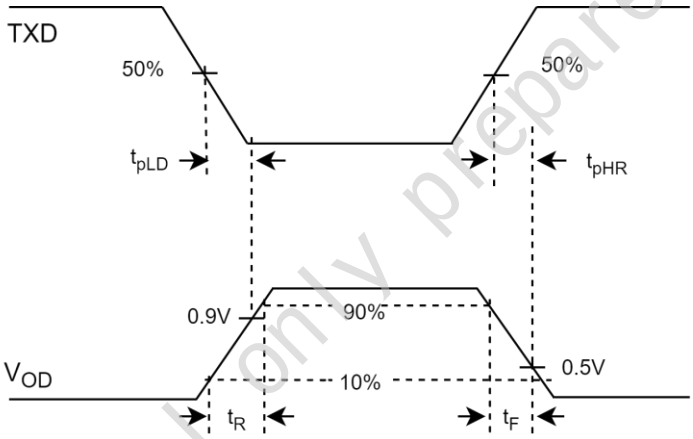


Figure 4. Driving characteristic measurement

A. The input pulse TXD is supplied by a generator with the following characteristics: t_R≤10ns, t_F≤10ns. The rising edge and the falling edge of the TXD should be as fast as possible.

B. C_L includes instrumentation and capacitance introduced by other CAN nodes.

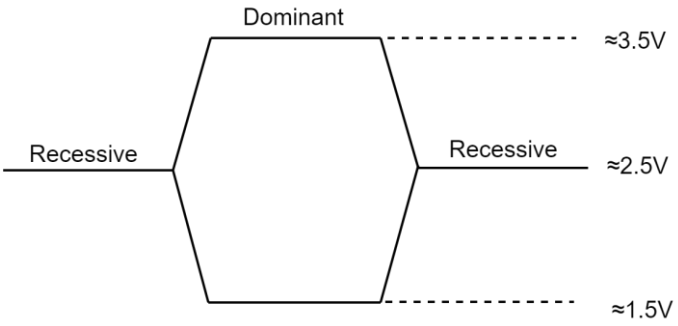


Figure 5. Bus Logic State and Voltage Definitions

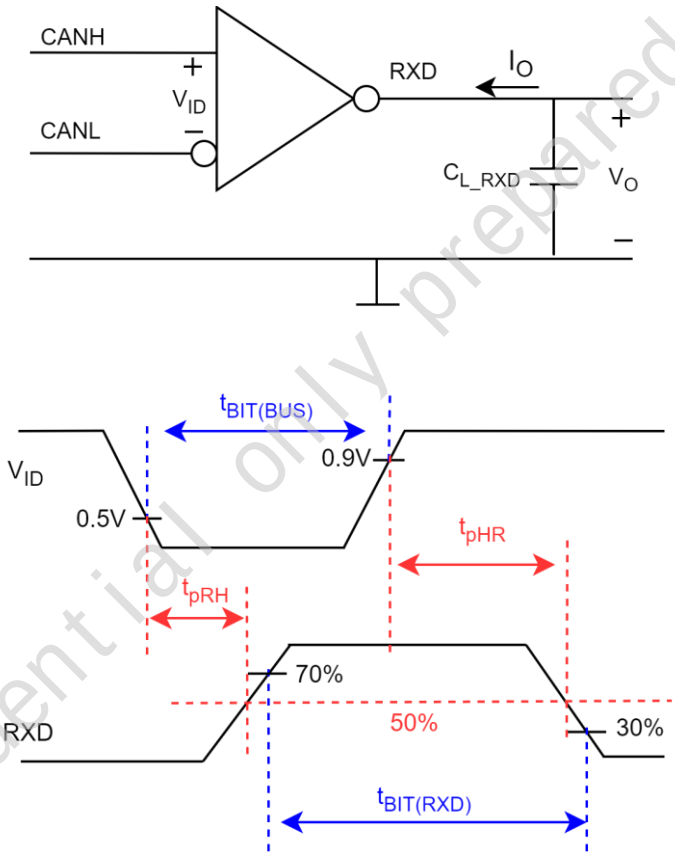


Figure 6. CAN FD Timing Parameter Measurement

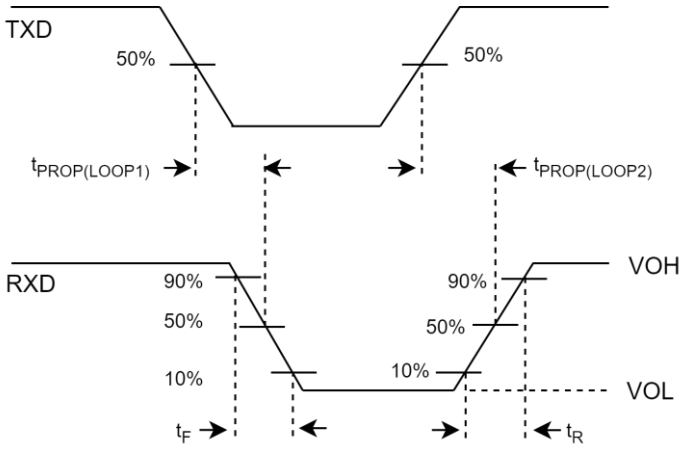


Figure 7. $T_{PROP(LOOP)}$ and Receiver Parameter Measurement

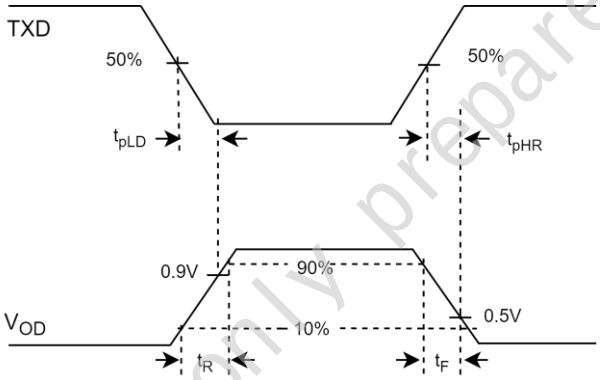


Figure 8. Driver Waveform and Parameter Measurement

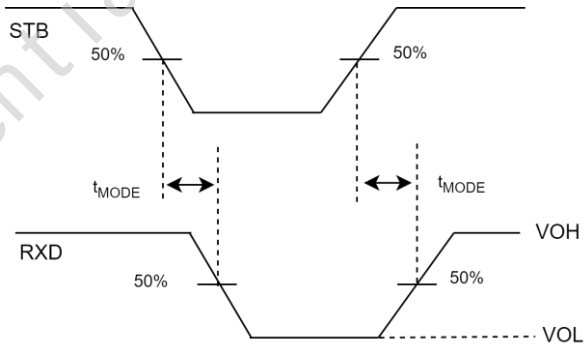


Figure 9. t_{MODE} Measurement

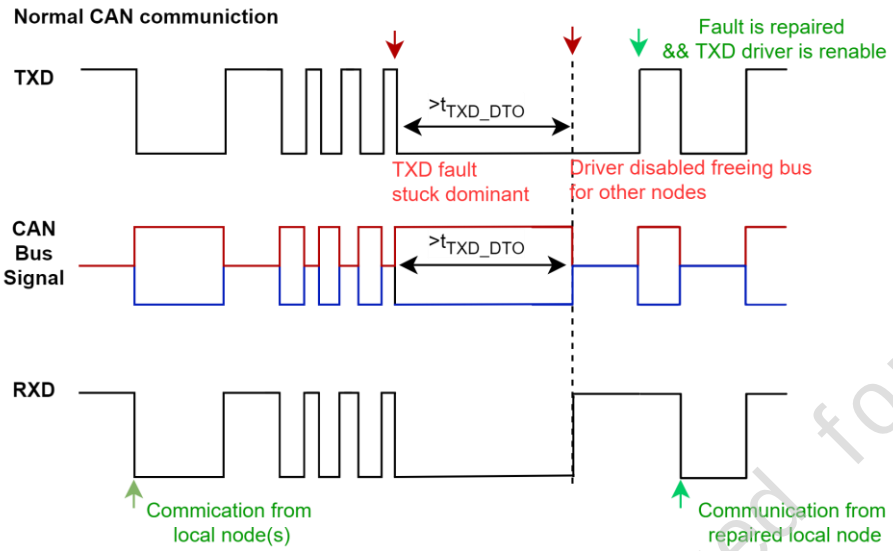


Figure 10. TXD Dominant Timeout Parameter Measurement

8. Detailed Description

8.1 Overview

MCAN1462 family are the interface between CAN controller and physical layers, and are used to convert digital signals to differential signals. They are designed for data rates up to 10 Mbps for CAN FD and enhanced higher data rates in long and highly-loaded networks. These CAN transceivers meet the ISO11898-2(2016) physical layer standard and CiA 601-4 Singal Improvement capability (SIC). These devices are backward compatible for supporting classic and CAN FD network application. MCAN1462 with low electromagnetic emission and improved electromagnetic immunity, enhances the robustness in complex network. MCAN1462 is a stand-alone transceiver with Standby mode allowed for low current consumption. These devices provide several protection features to enhance device robustness in some abnormal situations.

Signal Improvement is added to minimize the signal ringing in the complex star topologies especially when the maximum data rate is achieved. Signal Improvement is done by forcing transmitter output impedance to be 100Ω during the active recessive phase. The device continues to strongly drive the bus recessive until $t_{SIC\_TX\_BASE}$ so that the dominant-to-recessive signal edge is clean at the sampling point.

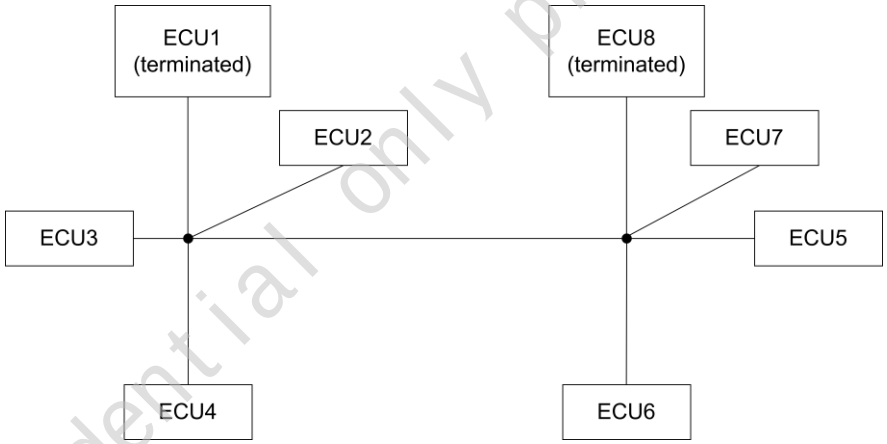


Figure 11 CAN Network: Star topology

8.2 Functional Block Diagram

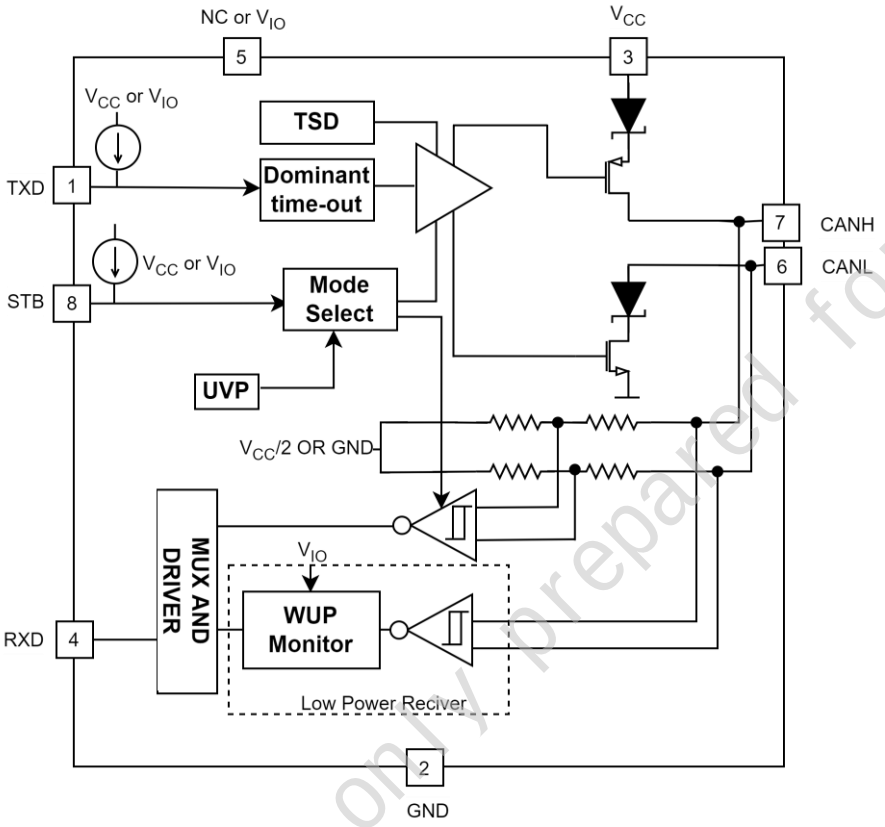


Figure 12. Function Block Diagram

8.3 Feature Description

8.3.1 Normal Mode

The CAN driver and receiver are fully operational, and CAN communication is bi-directional in Normal mode. The transmitter can convert digital data into differential data on the bus lines and the receiver converts the transmitter data on the bus lines into the digital data and outputs to pin RXD. The common-mode voltage on the bus lines is controlled internally.

8.3.2 Standby Mode

When there is no activity on the bus lines, transceiver can enter Standby mode to reduce the current consumption further by putting pin STB high. The bus lines are biased to ground to minimize the supply current in Standby mode. Transmitter cannot convert digital data into differential data on the bus lines and the high-speed receiver blocks are turned off to reduce supply current. The low-power receiver monitors the bus lines and is supplied by VIO even though the pin VCC is not supplied. In Standby mode, the pin RXD remains high until there are any activities occurring on the bus. When any activities exist on the bus, only the signals longer than tWK_FILTER are reflected on pin RXD. Pin RXD goes low to signal a wake-up request when recognizes WUP signals, then MCU can push pin STB low to change MCAN1462 to Normal mode.

8.3.3 TXD Dominant Timeout (DTO)

During Normal mode, the TXD DTO circuit prevents the transceiver from driving bus lines permanently dominant and blocking Normal network communication in event of hardware or software failure. When TXD is held dominant longer than tTXD_DTO, the DTO circuit would disable the CAN bus driver until a rising edge on TXD happens. This releases the bus lines to recessive state for communication between other nodes on the network during a TXD dominant timeout time. The TXD dominant time-out time also defines the minimum possible bit rate.

8.3.4 Internal Biasing of TXD and STB Input Pins

If TXD and STB are left floating, pins TXD and STB have internal pull-up resistors (to VIO) to ensure a defined state. It is helpful to minimize supply current in Standby mode.

8.3.5 Thermal Shutdown Protection (TSD)

MCAN1462 turns off the CAN driver circuits if the junction temperature exceeds the thermal shutdown temperature. The CAN bus lines will be recessive and block the TXD-to-Bus transmission path until the junction temperature drops at least below 160℃, which is the thermal shutdown temperature minus the thermal shutdown hysteresis. MCAN1462 minimizes the operating current by blocking the TXD-to-Bus path while keeping the Receiver-to-RXD path operational during TSD.

8.3.6 Undervoltage Detection on Pins V_{CC} and V_{IO}

MCAN1462 places the device in protected mode if VCC or VIO drops below the UVLO threshold. If VCC drops below the UVVCC, the transceiver enters the operation states shown on Table 3. If VIO drops below the **UVVIO**, the bus output is high impedance and the transceiver disengages from the bus until VIO recovered. This protects the bus during under-voltage detection at either VCC or VIO supply terminals.

8.3.7 Over Current Protection

During Normal mode, the over-current-protection (OCP) circuitry prevents MCAN1462 from damages by limiting the maximum working current when the CAN bus connects to the battery incorrectly. OCP circuitry limits the current flowing into MCAN1462 when an incorrect voltage is put on the CANH/CANL.

8.3.8 Unpowered Device

The device is designed to be ideal passive if it is unpowered. There is extremely low leakage current through the bus and the logic terminals when the unpowered device is connected to the CAN network. This is critical if some nodes of the network are unpowered while the rest of the network remains in operation. All terminals have extremely low leakage currents when the device is unpowered to avoid loading down other CAN nodes.

8.3.9 Wake Up Pattern (WUP) in Standby Mode

The MCAN1462 family uses a remote wake request feature to indicate to MCU that the bus is active, and to return to Normal mode from Standby mode. The devices use the multiple filtered dominant wake up pattern to wake up nodes under Standby mode. Once a WUP has been received, the RXD output follows the BUS signal with special pattern to indicate to the host controller that the node should return to Normal mode. The WUP contains a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. Bus signals that last less than tWK_FILTER(MIN) will be ignored. The WUP should finish within tWK_TIMEOUT, otherwise it is not a valid WUP. Bus signals that last more than tWK_FILTER(MIN) but less than tWK_FILTER(MAX) may not be viewed as a valid WUP. Bus signals that last more than tWK_FILTER(MAX) will always be detected as part of valid WUP. Once the full WUP has been detected, the device starts to drive the RXD output to follow the BUS signal with some special pattern. Once the first filtered dominant signal is received, the low-power receiver starts waiting for the filtered recessive signal and the other bus traffic lasted less than $t_{WK\_FILTER(MIN)}$ will not reset the monitor. After receiving the second dominant signal longer than

t_{WK_FILTER}, the device will drive the RXD to be low for the remainder of any dominant signal. For an additional layer of robustness and to prevent MCAN1462 from false wake-ups, the device implements a wake-up timeout feature. In order to have a successful remote wake-up event, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in current state without waking up.

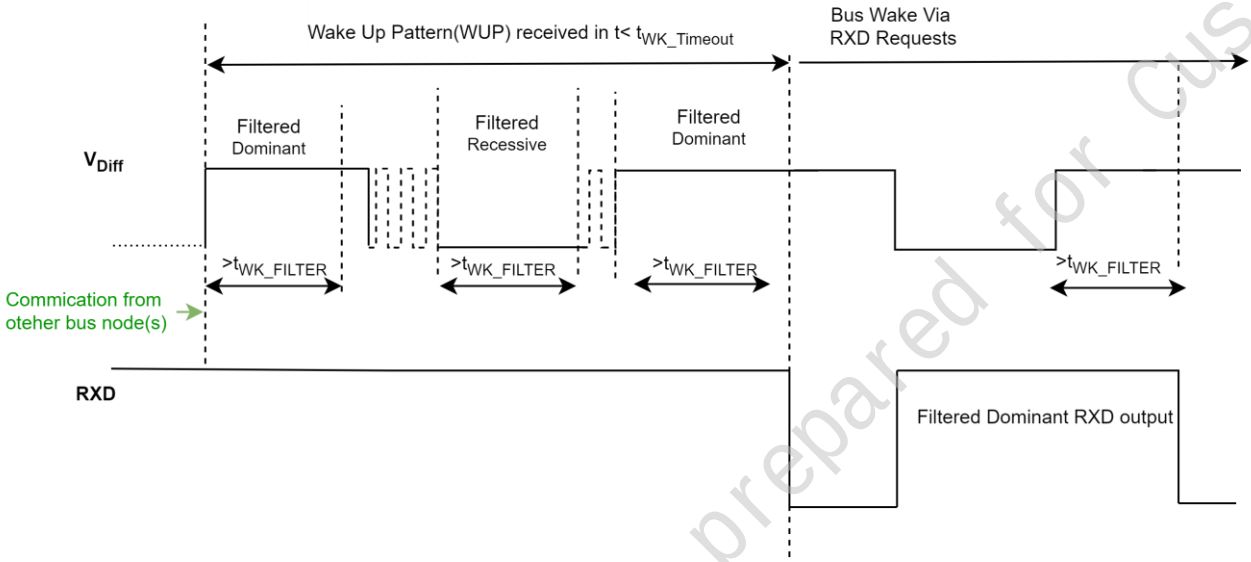


Figure 13. Wake Up Pattern

8.4 Device Functional Modes

The device operates in two modes: Normal mode and Standby mode. A low level on pin STB selects Normal mode. Both the driver and receiver are enabled and RXD mirrors bus state when the device operates in Normal mode. A high level on pin STB selects Standby mode, during which both the driver and receiver are disabled with only the low-power receiver monitoring the bus line, and the RXD output is high (VIO provided). The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests. The bus voltage is biased to ground in Standby mode. Once the low power receiver detects the wake-up pattern, RXD pin is pulled down to indicate to MCU with RXD following the CAN bus with tWK_FILTER. The local controller should monitor RXD for transitions from high to low and reactivate the device to normal mode by pulling the STB pin low.

8.4.1 CAN Bus States

The CAN bus has two states during operation on the Normal mode: dominant and recessive. In the dominant bus state, CAN bus is driven differentially, corresponding to a logic low on TXD and RXD. In recessive state, the bus is biased to $V_{CC}/2$ via high-resistance internal input resistors R_{IN}, corresponding to a logic high on TXD and RXD. Low Power Standby mode is activated by setting STB terminal high and CAN bus is biased to ground via internal high resistance input resistors R_{IN}.

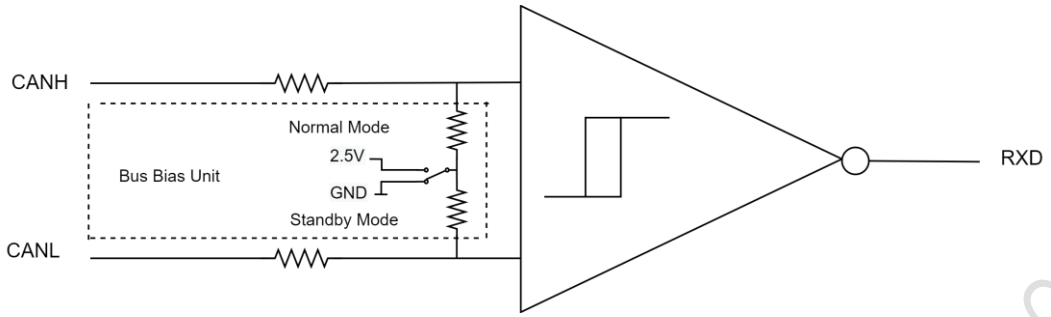


Figure 14. Bus Bias Unit and Receiver

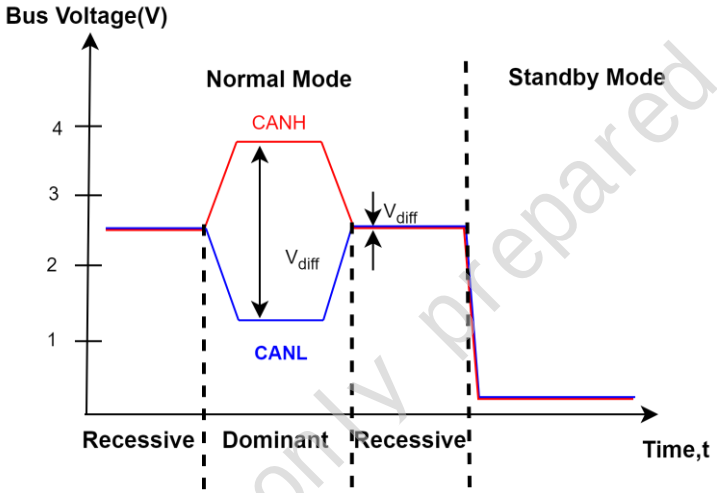


Figure 15. Bus State and Bus Bias

Table 2. Performance with STB Control (Device with the V suffix)

STB	MODE	DRIVER	RECEIVER	BUS BIAS	RXD
LOW	Normal Mode	Enabled	Enabled	$V_{CC}/2$	Mirror Bus
HIGH	Standby Mode	Disabled	Disabled Low Power Receiver is active	ground	High

Table 3. Under-voltage Lockout (Devices with the V suffix)

V_{CC}	V_{IO}	STATE	TRANSMITTER	RECEIVER	RXD
$>UV_{VCC}$	$>UV_{VIO}$	STB=Low Normal	Enable	High speed receiver	Mirror Bus(1)
		STB=High Standby	Disable	Low power receiver (2)	Bus Wake RXD Request
$< UV_{VCC}$	$> UV_{VIO}$	STB=Low Protected Mode	Disable	Disable	High
		STB=High Standby	Disable	Low speed receiver	Bus Wake RXD Request
$> UV_{VCC}$	$< UV_{VIO}$	Protected Mode	Disable	Disable	High impedance
$< UV_{VCC}$	$< UV_{VIO}$	Protected Mode	Disable	Disable	High impedance

Notes:

(1) Mirror bus state: logic low if CAN bus is dominant, logic high if CAN bus is recessive.

(2) Low power receiver: receiver monitors the bus activity and accepts bus wake up request.

8.4.2 Driver and Receiver Function Tables

Table 4. Driver Function Table

DEVICE	CAN DIFFERENTIAL INPUTS		BUS STATE
	STB	TXD	
All Devices	L	L	Dominant
		H or Open	Recessive
	H or Open	X	High impedance

Table 5. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS	BUS STATE	RXD TERMINAL
Normal	$V_{ID} \geq V_{IT+(MAX)}$	Dominant	L
	$V_{IT-(MIN)} < V_{ID} < V_{IT+(MAX)}$	Indetermined	Indetermined
	$V_{ID} \leq V_{IT-(MIN)}$	Recessive	H

9. Application and Implementation

9.1 Application Information

The CAN transceivers with a host microprocessor are typically used in automotive and industrial applications. MCAN1462 can be configured for both 5V and 3.3V microprocessor applications. MCAN1462 is typically used in the following network shown on Figure 17, and the bus termination should be placed on the two far end.

9.2 Typical Applications

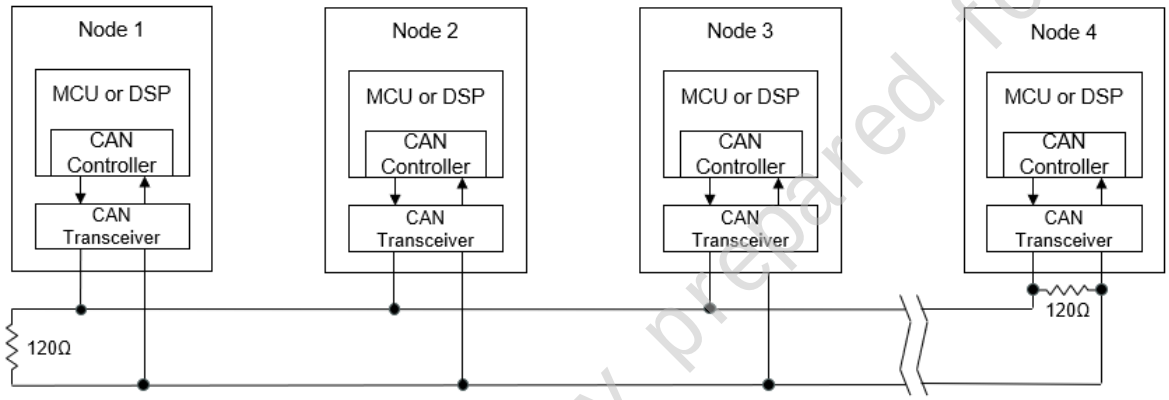


Figure 16. Typical CAN Bus Application

9.3 CAN Termination

The characteristic impedance of the twisted pair cable is required to be equal to the characteristic impedance of the line. The terminated resistors need to place at the both end of the cable to prevent signal reflections. Stubs should be kept as short as possible to reduce unnecessary signal reflections. In order to keep common-mode voltage stable, especially in the high ambient temperature environment, split termination should be used.

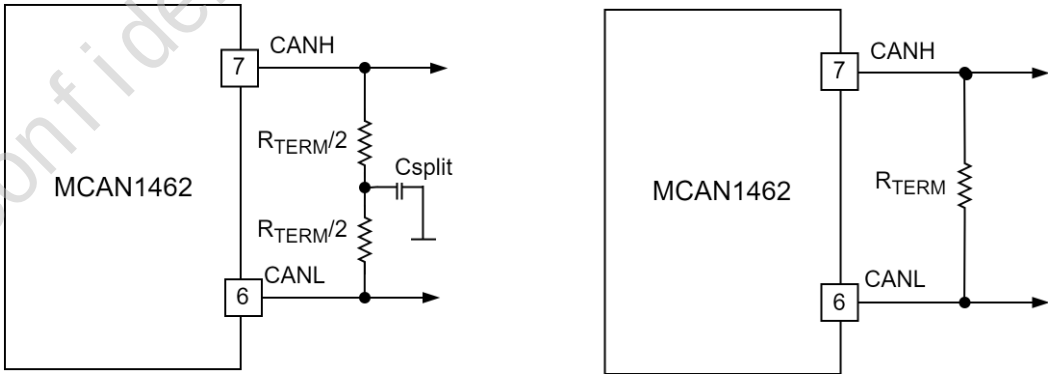


Figure 17. Termination

The family of transceivers are suitable for both 5-V only applications and 3.3 V application where devices with the V suffix are used for 3.3 V micro-controller.

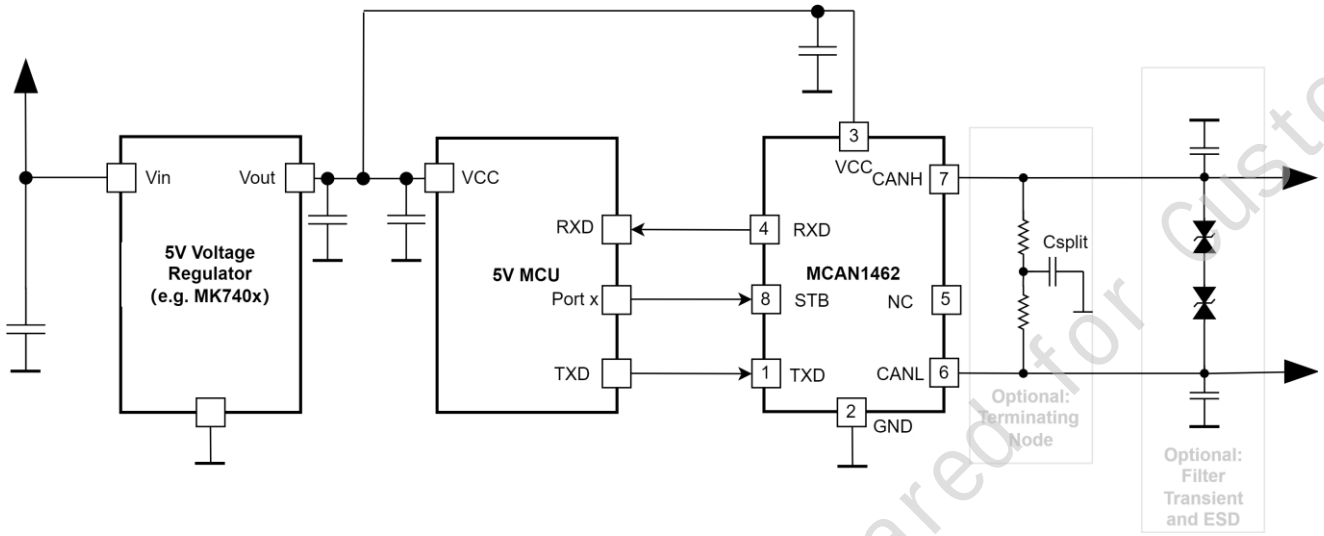


Figure 18. Typical CAN Bus Application with 5V MCU

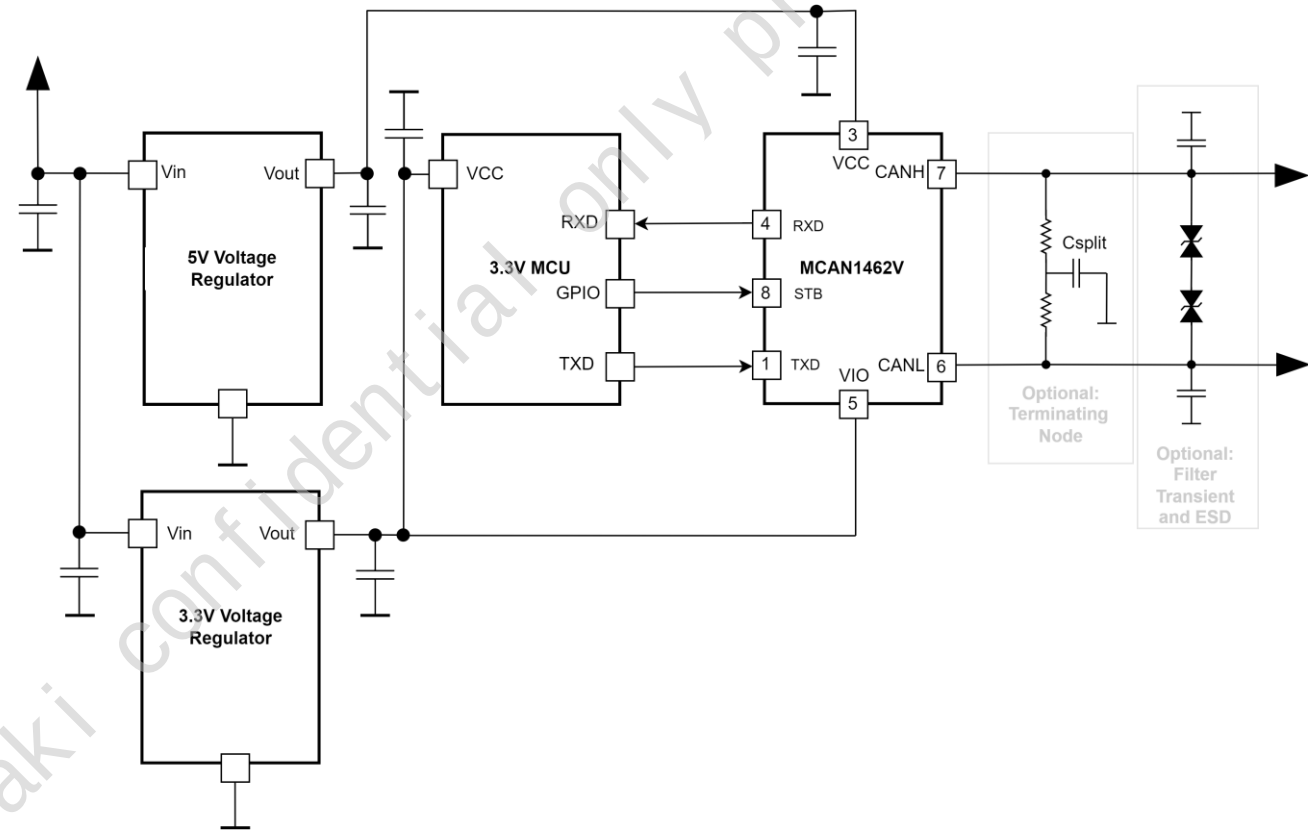


Figure 19. Typical CAN Bus Application with 3.3V MCU

10. Power Supply Recommendations

The devices are designed to operate from input supply voltage V_{CC} between 4.5 V and 5.5 V and I/O level shifting supply voltage V_{IO} between 2.95 V and 5.5 V. Both supply inputs should be regulated where a bulk capacitance should be placed near the pin V_{CC} and a bypass capacitor should place as close to the V_{IO} supply pin as possible. It helps reduce supply ripple and compensate for the parasitic capacitance and inductance on the designed PCB power plane. If the ripple on the supply pin is not acceptable, capacitor with greater capacitance should be adopted.

11. Layout

Reliable CAN bus design needs to use external transient protection device to protect the CAN device from suffering surge transients in the environment. Devices can deal with some ESD problems with the ESD protection inside. However, PCB design needs to consider higher levels of ESD immunity and external protection device such as TVS diodes needs to be used.

11.1 Layout Guidelines

- Place the protection circuitry as close to the bus connector as possible.
- Use supply and ground planes to provide low inductance.
- Bypass capacitors should place as close to V_{CC} as possible.
- Split termination is recommended to reduce common-mode EMI emission.
- In order to limit current of the TXD, RXD and STB line, serial resistor may be used.
- For devices with level shifting, bypass capacitors should be placed as close to V_{IO} as possible. For devices without level shifting, left the pin floating.

11.2 Layout Example

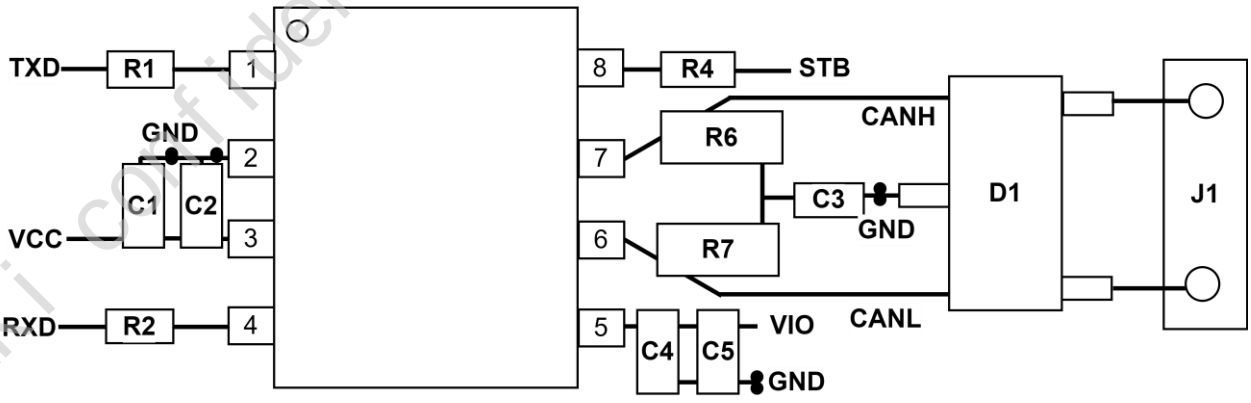


Figure 20. Layout Example

12. Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

13. Mechanical, Packaging

13.1 SOP-8 Package Size

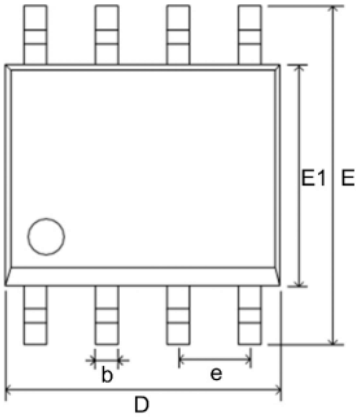


Figure 21. SOP-8 Top View

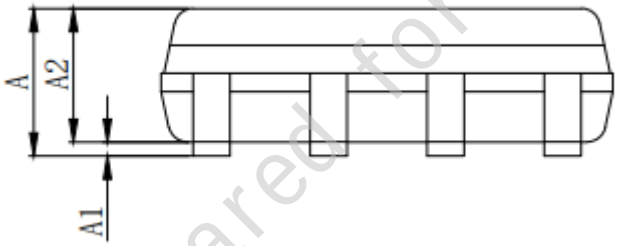


Figure 22. SOP-8 Side View

Figure 23. SOP-8 Side View

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.3	1.55	1.75
A1	0.05	-	0.25
A2	1.25	1.40	1.65
b	0.33	-	0.51
c	0.20	-	0.25
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27(BSC)		
L	0.4	-	1.27
θ	0°	-	8°

13.2 SOP-8 Recommended Land Pattern

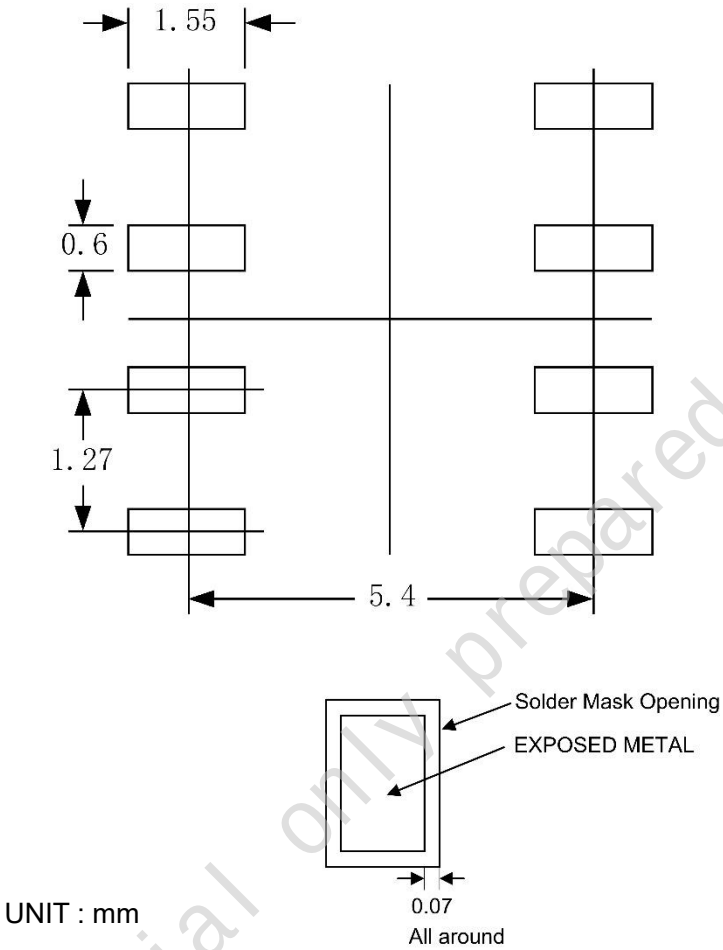


Figure 24. Recommended SOP-8 Land Pattern

13.3 DFN 3*3 Package Size

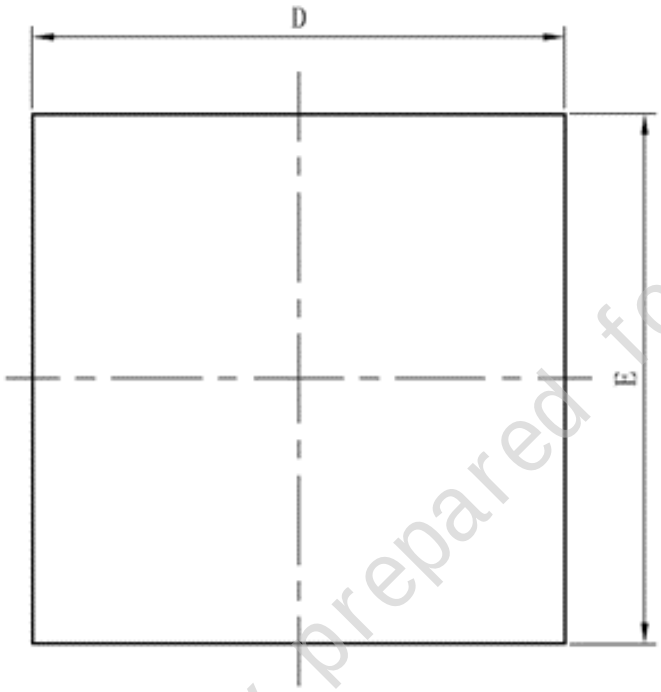


Figure 25. DFN 3*3 Top View

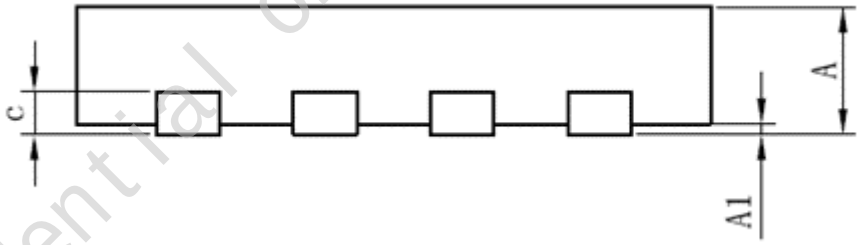


Figure 26. DFN 3*3 Side View

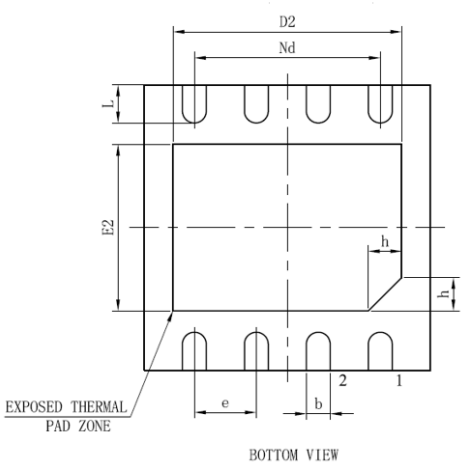


Figure 27. DFN 3*3 Side and Bottom View

SYMBOL	Millimeter		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	-	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e	0.65 BSC		
Nd	1.95 BSC		
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30

13.4 DFN 3*3 Recommended Land Pattern

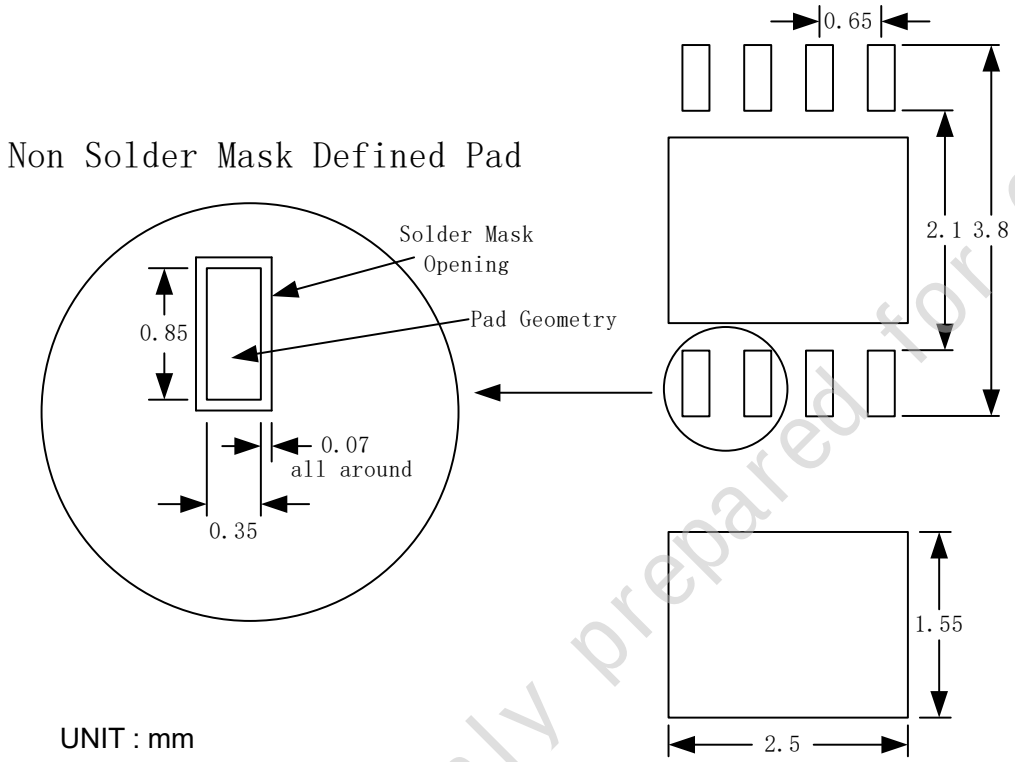


Figure 28. DFN 3*3 Land Pattern Data

14. Reel and Tape Information

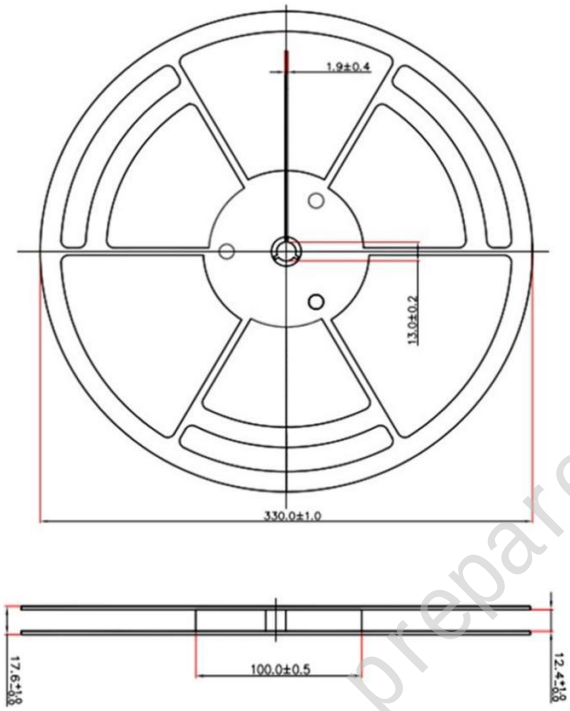
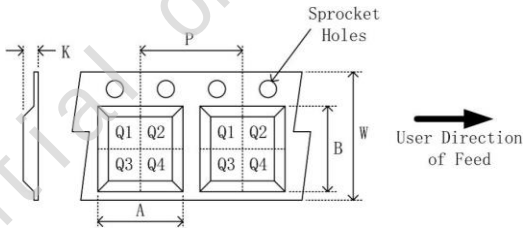


Figure 29. Reel Dimensions



Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
MCAN1462XAB-Q1	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8±0.1	4±0.1	12±0.1	Q1
MCAN1462VXAB-Q1	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8±0.1	4±0.1	12±0.1	Q1
MCAN1462XDB-Q1	DFN 3*3	8	3000	3.3±0.1	3.3±0.1	1.1±0.1	8.0±0.1	4±0.1	12.0±0.3	Q2
MCAN1462VXDB-Q1	DFN 3*3	8	3000	3.3±0.1	3.3±0.1	1.1±0.1	8.0±0.1	4±0.1	12.0±0.3	Q2

Figure 30. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

15. Tape and Reel Box Dimensions

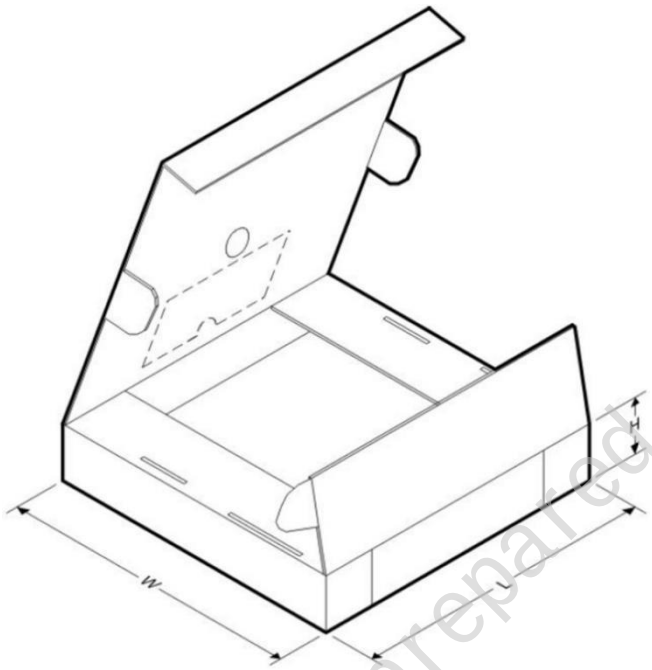


Figure 31. Box Dimensions

Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MCAN1462XAB-Q1	SOP-8	8	8000	360	360	65
MCAN1462VXAB-Q1	SOP-8	8	8000	360	360	65
MCAN1462XDB-Q1	DFN 3*3	8	3000	360	360	65
MCAN1462VXDB-Q1	DFN 3*3	8	3000	360	360	65