Single-Port IEEE 802.3af/at PSE Controller

1. Description

The MK3614E is a high-density integrated autonomous single Ethernet port power sourcing equipment (PSE) controller designed for use in IEEE 802.3af/at Power over Ethernet (PoE) systems. The device provides powered device (PD) detection, classification, current limit, load disconnect detection, and operating current levels. The device features intelligent protection circuitry and allows the delivered to PD power up to 35W. The device integrates a 0.3Ω power MOSFET and a current-sensing resistor, which enables the non-PoE protocol adapter to be feasibly retrofitted into a PSE adapter with the PoE protocol only requiring a few external components.

The MK3614E's LED pin is an open-drain output. The pin outputs simple digital logic signals, which indicate various operating statuses and fault conditions. The device supports Midspan or Endpoint mode. The Midspan mode function has a longer detection back-off timer.

2. Applications

- IEEE 802.3af and 802.3at Power-Sourcing Equipment (PSE)
- Power over Ethernet Switches/Routers
- IP Phone Systems
- IP Camera Systems
- 5G Small Cells

3. Features

- IEEE 802.3af and 802.3at compatible
- Fully autonomous operation, no external controller required
- Up to 35W for PSE Applications
- 0.2mA standby current (Midspan mode)
- Integrated an 80V 0.3Ω power MOSFET and current-sensing resistor
- Multi-point detection
- Class 3 and Class 4 configuration
- Supports reset operation
- LED status indication
- Supports Midspan and Endpoint modes
- 8-pin ESOP-8 package with thermal pad

4. Typical Application

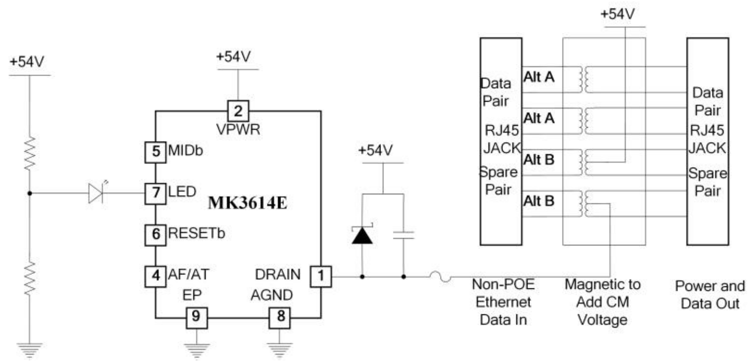


Figure 1. Typical Application Diagram for 802.3at Midspan Configuration

5. Order Information

Order Part Number	Descriptions
MK3614EXAD	ESOP-8, tape, 4k/reel

6. Pin Configuration and Functions

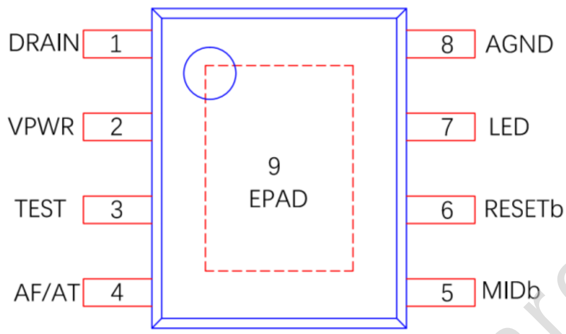


Figure 2. Pin Function (top view)

Table 1. Pin Functions

Pin		I/O	Description
NO.	Name		
1	DRAIN	Analog Power Output	MOSFET drain output.
2	VPWR	Analog Power Input	Positive PoE voltage (+44V to 57V) relative to AGND.
3	TEST	—	Connect to AGND.
4	AF/AT	Digital Input	Pull up to internal VDD rail with 10μA current. Connect to AGND for AF configuration, leave floating for AT configuration.
5	MIDb	Digital Input	Pull up to internal VDD rail with 10μA current. Connect to AGND to set 2.7 seconds detection backoff timing (Midspan)， leave floating for Endpoint configuration.
6	RESETb	Digital Input	Pull up to internal VDD rail with 20μA current. Active low device reset input. Connect a 120kΩ to 200kΩ resistor to AGND.
7	LED	Digital Output	Open drain output pin, turn on an external LED when a PoE PD is connected and powered. Refer to LED section for more details.
8	AGND	Analog Ground	Analog ground.
9	EPAD	—	Exposed pad, it should be connected to AGND, connect to power ground plane for better thermal performance.

7. Specifications

7.1 Absolute Maximum Ratings [1]

		MIN	MAX	Units
Input voltages	VCC VPWR, DRAIN to AGND	-0.3	80	V
	LED to AGND	-0.3	35	
	TEST, AF/AT, RESETb, MIDb to AGND	-0.3	7	
Operating Junction Temperature, T_J		-40	150	℃
Storage Temperature, T_{stg}		-65	160	
Soldering Temperature (10 second), T_{sld}			260	

Note:

(1) Stresses beyond the “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in “RECOMMENDED OPERATING CONDITIONS”. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 [2]	2000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

7.3 Recommended Operating Conditions

		MIN	MAX	Units
Recommended Operation Conditions	VPWR, DRAIN to AGND	32	60	V
	LED to AGND	0	30	
	TEST, AF/AT, MIDb, RESETb, MIDb to AGND	0	5.5	
	Junction Temperature	-40	+125	℃

7.4 Thermal Information

		Value	Units
Package Thermal Resistance	θ_{JA} (Junction to ambient)	30	°C/W
	θ_{JC} (Junction to case)	10	

7.5 Electrical Characteristics

Conditions are –40°C < T_J < 125 °C, V_{PWR} = 54 V unless otherwise noted. Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted.

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Power Supply Voltages						
V_{UVLO_ON}	V_{PWR} UVLO Input Voltage		25.5	28	—	V
V_{UVLO_OFF}	V_{PWR} UVLO Input Voltage		—	31	33.5	V
Power Supply Currents (1)						
I_{PWR}	V_{PWR} Supply Current	During normal operation (Detection + Idle), MIDb=Float	—	0.45	—	mA
		During normal operation (Detection + Idle), MIDb=GND	—	0.2	—	mA
Detection Specifications						
I_{DET_SC}	Detection Short Circuit Current	Measured when DRAIN is shorted to VPWR	—	1.5	5	mA
V_{PORT}	Detection Voltage When R_{DET} = 24 kΩ	V_{PWR} - V_{DRAIN}, primary detection voltage	2.8	4	—	V
		V_{PWR} - V_{DRAIN}, secondary detection voltage	—	8	10	V
T_{DET}	Detection Time		—	320	500	ms
T_{IDLE}	Detection Idle Time	MIDb=Float	—	315	—	ms
		MIDb=GND		2700		ms
R_{GOOD} (1)	Signature Resistance		—	25	—	kΩ
R_{DET_MIN} (1)	Minimum Signature Resistance @ PD		15	17	19	kΩ
R_{DET_MAX} (1)	Maximum Signature Resistance @ PD		26.5	30	33	kΩ
C_{REJECT}	Reject Signature Capacitance		—	2.2	10	µF
Classification Specifications						
V_{CLASS}	Class Event Voltage	V_{PWR} - V_{DRAIN}, Class current between 0 and 51 mA	15.5	—	20.5	V

I_{CLASS_LIM}	Class Event Current Limitation	Measured when DRAIN is shorted to VPWR	51	—	95	mA
T_{CLE}	Class Event Timing	Assigned PD Class 0, 1, 2, 3, 4	6	—	30	ms
I_{CLASS_REGION}	Classification Current Region	Class Signature 0	0	—	5	mA
		Threshold between Class Signature 0 or 1	5	—	8	mA
		Class Signature 1	8	—	13	mA
		Threshold between Class Signature 1 or 2	13	—	16	mA
		Class Signature 2	16	—	21	mA
		Threshold between Class Signature 2 or 3	21	—	25	mA
		Class Signature 3	25	—	31	mA
		Threshold between Class Signature 3 or 4	31	—	35	mA
		Class Signature 4	35	—	45	mA
		Threshold between Class Signature 4 or invalid Class	45	—	51	mA
Classification Mark Specifications						
V_{MARK}	Mark Event Voltage	V_{PWR} - V_{DRAIN}, Mark current between 0 and 5 mA	7	—	10	V
I_{MARK_LIM}	Mark Event Current Limitation	Measured when DRAIN is shorted to VPWR	51	—	95	mA
T_{ME}	Mark Event Timing	Assigned PD Class 4	6	—	12	ms
Current Limit and Overcurrent						
I_{CUT}	Overcurrent Threshold	TA=25°C, AF/AT=0b	—	410	—	mA
		TA=25°C, AF/AT=1b	—	710	—	mA
T_{CUT}	Overcurrent Time Limit		50	—	75	ms
I_{INRUSH}	Output Current in POWER_UP State	TA=25°C, all assigned PD Classes, V_{PORT} > 30 V	—	465	—	mA
I_{LIM}	Current Limit	TA=25°C, Power-on, assigned PD Class 0, 1, 2, 3	—	485	—	mA
		TA=25°C, Power-on, assigned PD Class 4	—	825	—	mA

T_{LIM}	Short Circuit Time Limit	Power-on, assigned PD Class 0, 1, 2, 3	50	—	75	ms
		Power-on, assigned PD Class 4	10	—	75	ms
Load Disconnect						
I_{PORT_DIS}	DC MPS Current	Current per pairset	—	7.5	10	mA
T_{MPDO}	PD MPS Dropout Time Limit		300	—	400	ms
MOSFET On Resistance						
R_{DSON}	FET Resistance	100mA drain to source current		290		mΩ
Digital Pin Characteristics						
V_{IL}	Input Low Voltage	AF/AT, RESETb, MIDb			1	V
V_{IH}	Input High Voltage	AF/AT, RESETb, MIDb	2			V
I_{LK}	Input Leakage	AGND < VIN < VDD, AF/AT, RESETb, MIDb	-1	—	1	µA
I_{PU}	Pullup Current to VDD	AF/AT, MIDb = 0V	-13	-10	-7	µA
I_{PU}	Pullup Current to VDD	RESETb = 0V	-26	-20	-14	µA
Over Temperature Protection (1)						
T_{RISE}	Rising Threshold		—	150	—	℃
T_{FALL}	Recover Threshold		—	130	—	℃

Note:

(1) Values are verified by characterization on bench, not tested in production.

7.6 Typical Characteristics

Typical values are at V_{PWR} = 54V, TA = 25°C, Endpoint mode with a Class 0 PD, unless otherwise noted

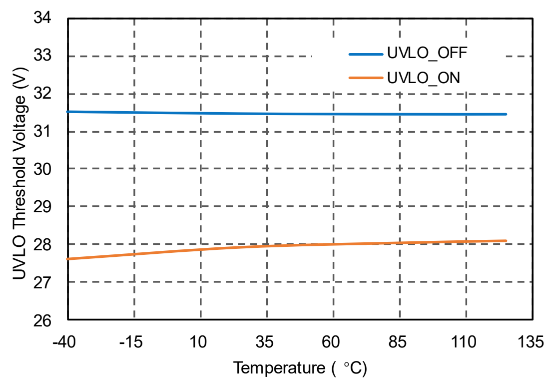


Figure 3. V_{PWR} UVLO Threshold Voltage vs. Temperature

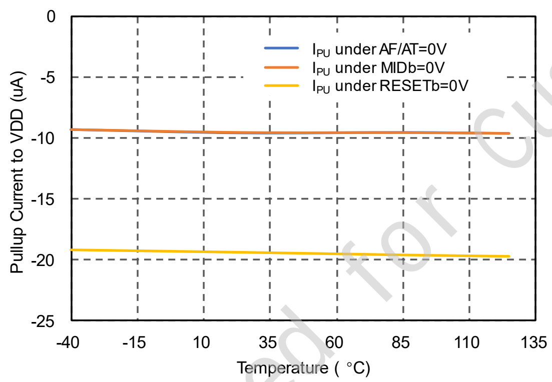


Figure 4. Digital Pin Pullup Current to VDD

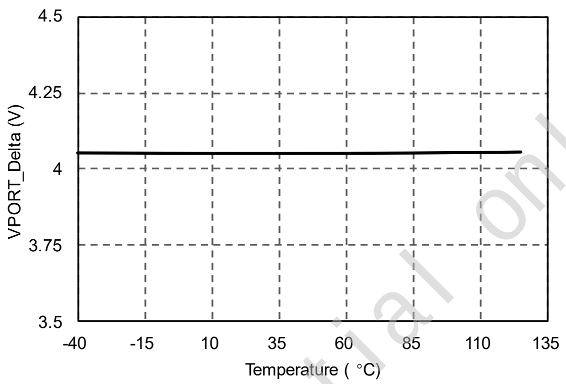


Figure 5. Voltage Difference Between Detection Points vs. Temperature

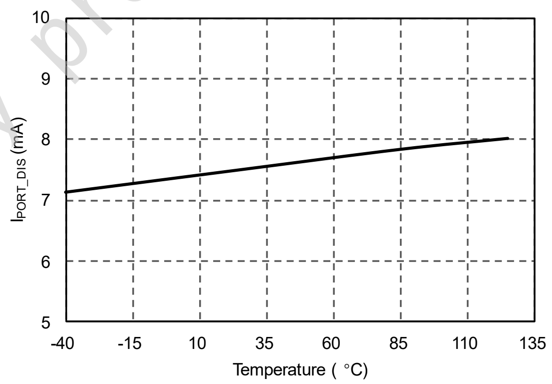


Figure 6. DC Maintain Power Signature

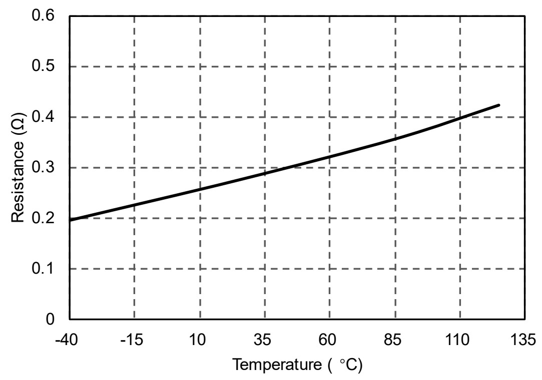


Figure 7. Internal FET Resistance vs. Temperature

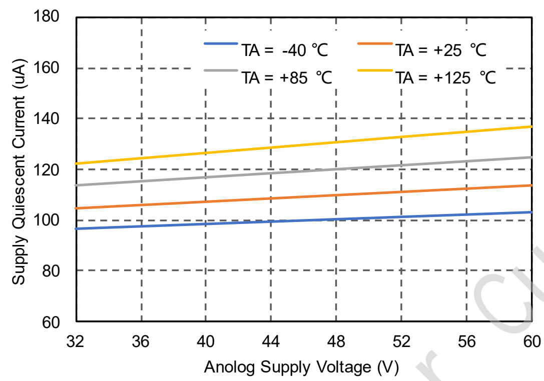


Figure 8. VPWR Current vs. Temperature (RESETb = 0V)

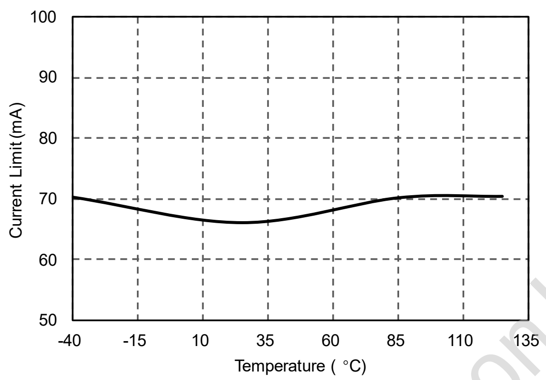
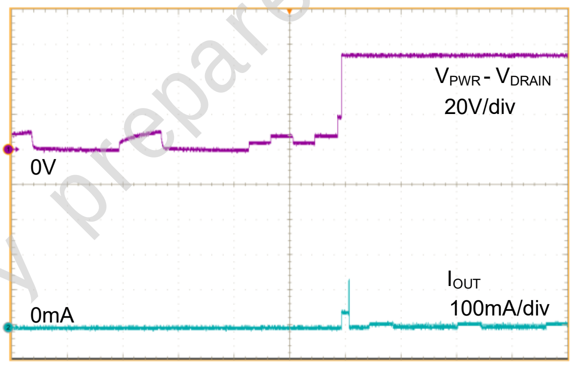
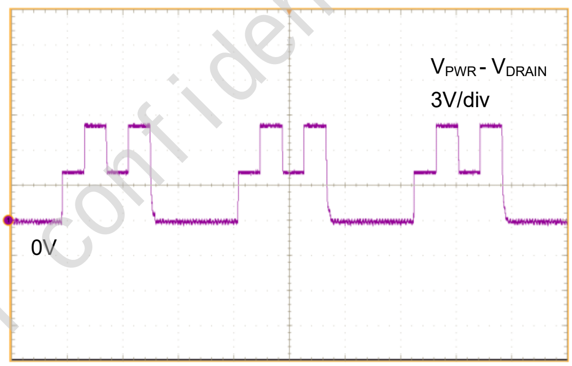


Figure 9. Classification and Mark Current Limit vs. Temperature



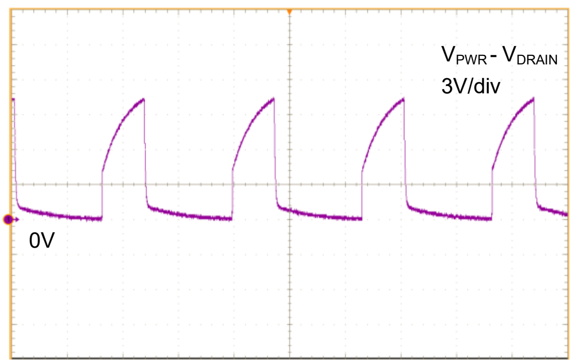
Time(200ms/div)

Figure 10. Startup with a valid PD



Time(200ms/div)

Figure 11. Detection with invalid PD (33kΩ)



Time(200ms/div)

Figure 12. Detection with invalid PD (Open)

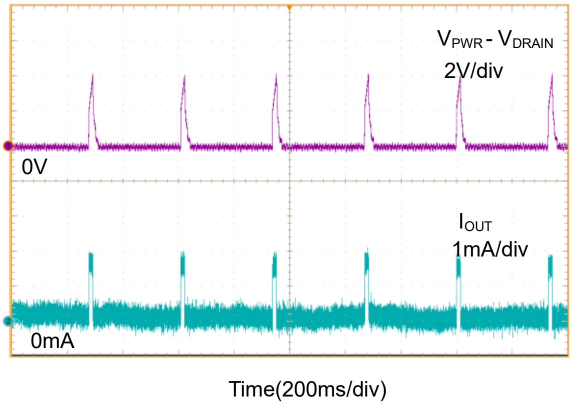


Figure 13. Detection with invalid PD (24kΩ and 10μF)

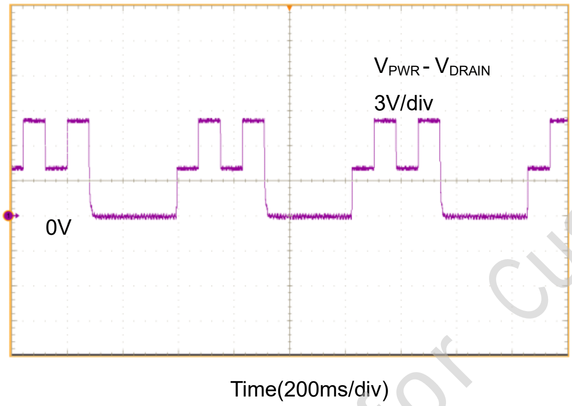


Figure 14. Detection with invalid PD (15kΩ)

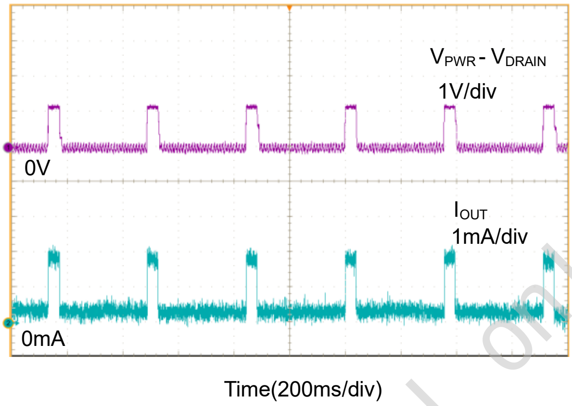


Figure 15. Detection with output shorted

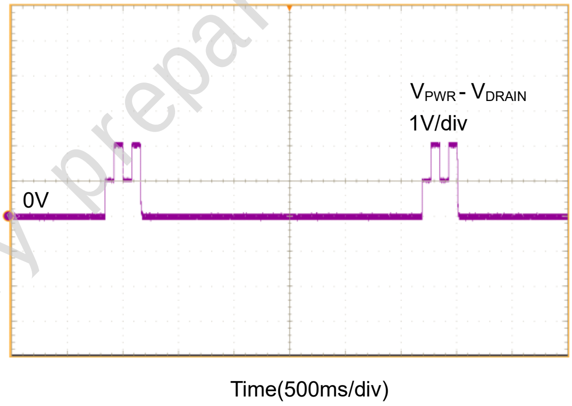


Figure 16. Detection in Midspan with invalid PD (15kΩ)

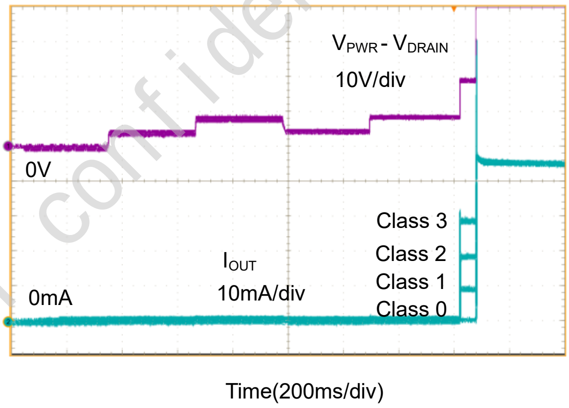


Figure 17. Classification with different PD invalid PD (15kΩ)

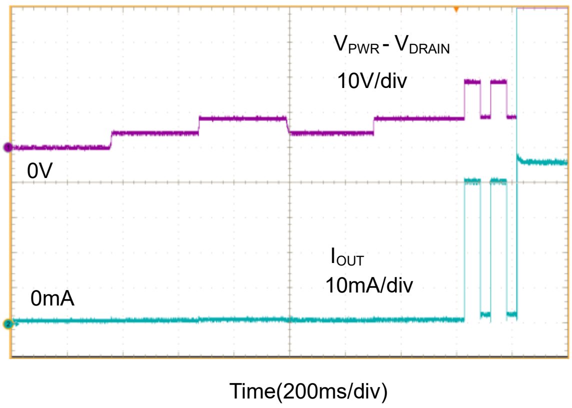


Figure 18. Classification with PD Class 4

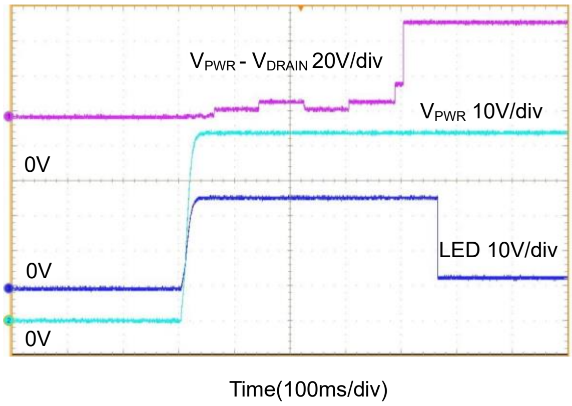


Figure 19. LED function of the PD powered from V_{PWR}

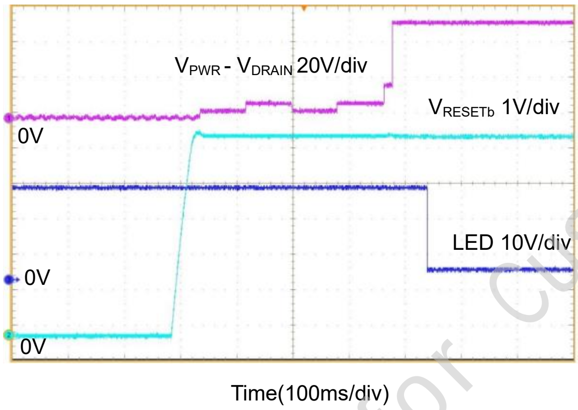


Figure 20. LED function of the PD powered from V_{RESETb}

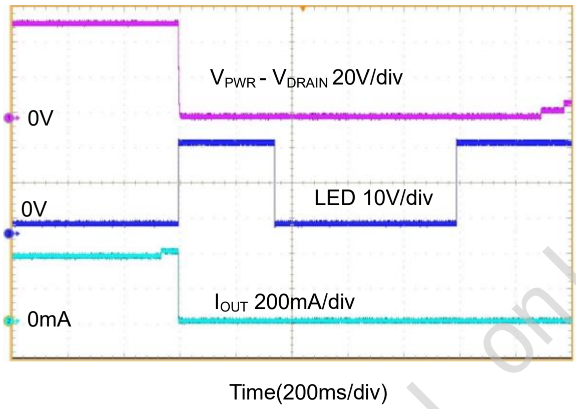


Figure 21. LED function of ICUT

8. Detailed Description

8.1 Overview

The MK3614E is a high-density integrated autonomous single-port PSE controller designed for use in IEEE 802.3af/at PoE systems. The device provides PD detection, classification, current limit, load disconnect detection and operating current levels. The MK3614E provides up to 35W to the Ethernet port. Besides, the MK3614E features intelligent protection circuitry including input undervoltage lockout, over-temperature protection, overcurrent timeout, port short protection, load-disconnect detection timeout, port voltage slew-rate limit during startup, operating status, fault conditions indicated by LED.

8.2 Functional Block Diagram

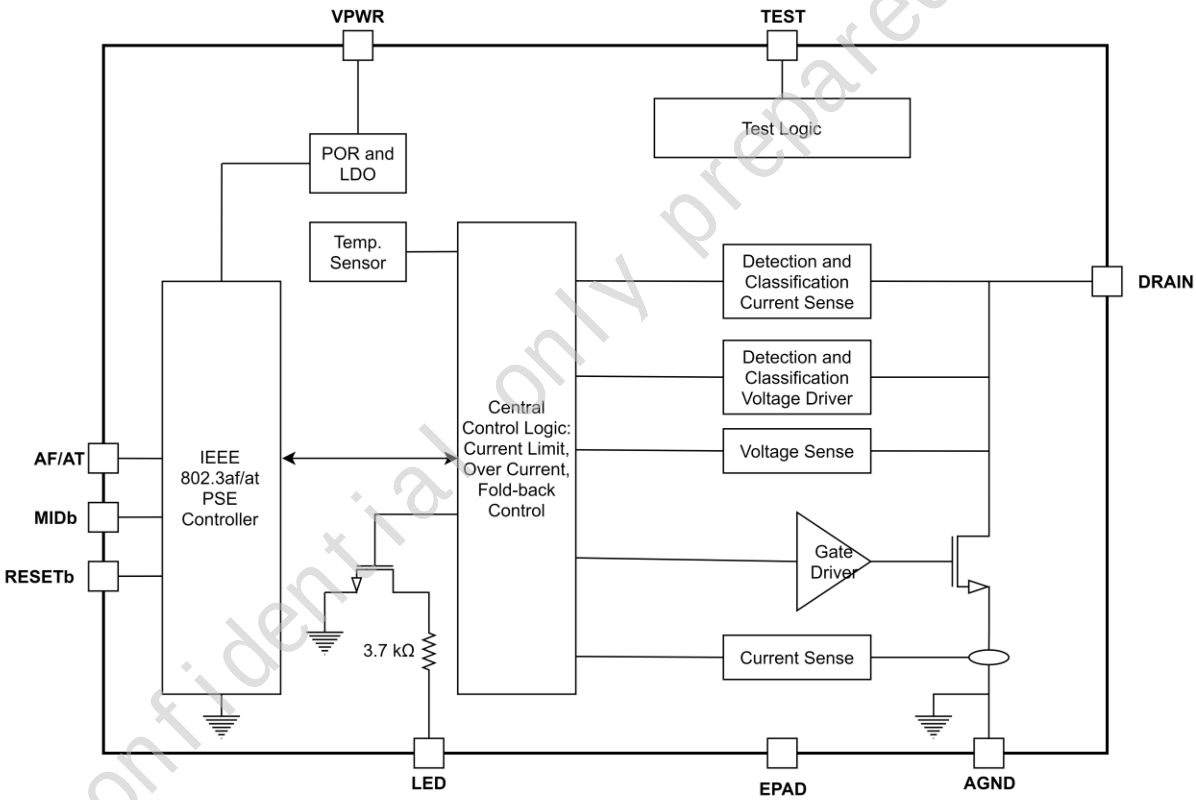


Figure 22. Block Diagram

8.3 Feature Description

8.3.1 Reset

The MK3614E is reset by power-up and hardware reset. Reset condition is cleared once V_{PWR} rises above the UVLO threshold. The MK3614E's RESETb pin is tied to internal VDD through a pull-up resistance. In a typical application, connect a 120kΩ to 200kΩ resister to AGND. However, if the RESETb pin is driven low (> 110us, typ), the MK3614E is reset. Once in the reset state, the port output and LED detection function are disabled. At the end of a reset event, the MK3614E latches in the state of AF/AT and MIDb input signals. During normal operation, changes of the AF/AT and MIDb inputs are ignored, and these inputs can only be changed at any time prior to the end of a reset state.

8.3.2 Midspan Mode

The MK3614E supports an Endpoint or Midspan PSE network configuration. In midspan mode, when failed detections occur, the device waits about 2.7s before attempting to detect again. Like the RESETb pin, MIDb pin is also tied to internal VDD through a pull-up resistance. The device is configured as Endpoint mode by default unless the MIDb pin is driven low.

8.3.3 PD Detection and Classification

Detection function of the MK3614E is the most important, which determines if the remote equipment
connected to a PSE is capable of receiving power. To avoid false detection in noisy environments, the MK3614E detects a PD by using a robust 4-point detection algorithm to reliably determine the signature resistance of the PD. During detection phase, the MK3614E keeps the internal MOSFET off and drives probe voltages with two different levels through the DRAIN pin. The device uses a specific algorithm to calculate the PD signature resistance by sampling the current injected into the port. Once the detection result is RGOOD, the MK3614E will perform Physical Layer classification by driving a class probe to determine the PD's class signature. The number of class events and mark events determines the PD requested power. Figure 23 shows a timing diagram of PD detection and classification for a Type 1 PSE powering a Type 1 PD. In this example, the MK3614E produces one class event to a Type 1 PD without any mark event. As shown in Figure 24 two class events and two mark events are driven by the MK3614E for a Type 2 PSE powering a Class 4 PD.

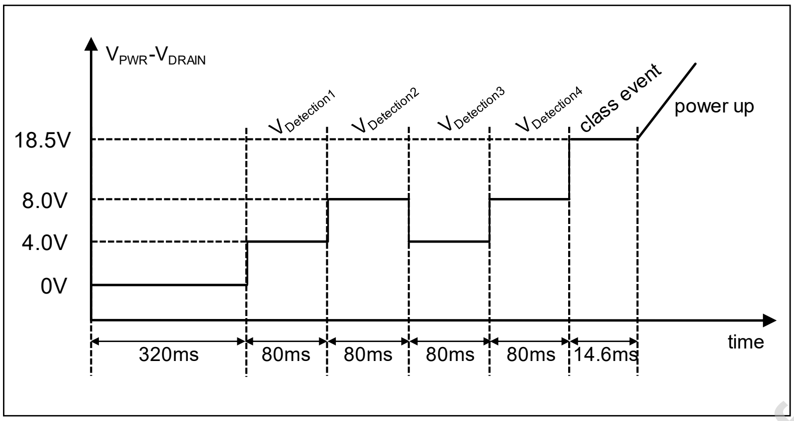


Figure 23. Type 1 Detection, Classification, and Port Power-Up Sequence

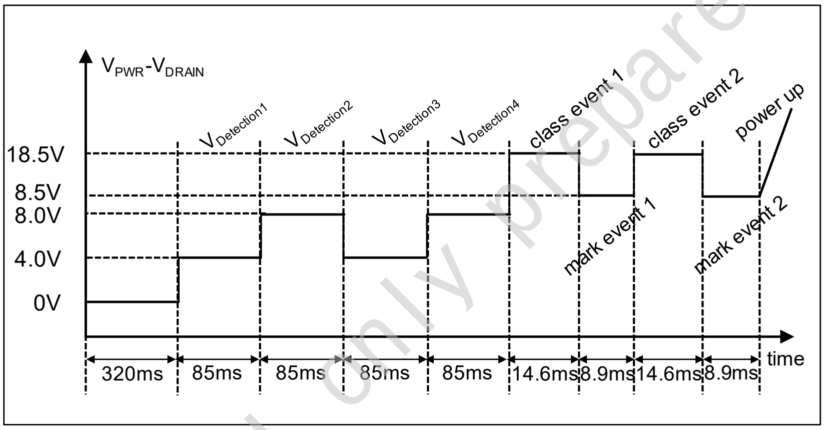


Figure 24. Type 2 Detection, Classification, and Port Power-Up Sequence

8.3.4 Inrush

After classification, if the MK3614E decides to power the PD, it will first go through the inrush phase. During inrush, the PSE limits the amount of current being delivered for at least 60ms. Between 1ms and 60ms after power-on, the inrush current of the MK3614E is limited to no more than 700mA

8.3.5 Operating Power

During a nominal powering state, the MK3614E checks for abnormal conditions, including overcurrent, PD disconnection, and short-circuits. Meanwhile, the MK3614E assigns the class required for PD to PD. The MK3614E achieves the purpose of distributing power by controlling the current called I_{CUT}. Once the current exceeds the I_{CUT} as least T_{CUT}, the MK3614E immediately cuts off the power and goes through detection phase.

8.3.6 Maintain Power Signature

When the MK3614E is supplying power to a PD, the MK3614E keeps on monitoring the current drawn in order to make sure that the PD is still connected. The minimum current that the PD must draw to avoid being disconnected is named the Maintain Power Signature (MPS). The MK3614E is designed to remove power when the MPS is absent for at least 350ms, ensuring that disconnected cables do not remain powered. In order to further reduce minimum standby power consumption for PoE systems, the MK3614E only requires that PD must draw a current above I_{PORT_DIS} for at least T_{MPS} with no more than T_{MPDO} between pulses.

8.3.7 Current Limit and Voltage Foldback

The MK3614E integrates a current-sensing resistor connected between the internal MOSFET and AGND to monitor the loop current. During normal operating conditions, the current running through the current-sensing resistor never exceeds the threshold ILIM. Otherwise, the internal feedback circuit regulates the driver voltage of the MOSFET to limit the current. Besides, the MK3614E senses the DRAIN voltage and regulates the current-limit value, which helps to reduce the internal MOSFET power dissipation.

8.3.8 LED Signals

The MK3614E's LED pin is open-drain output. The pin outputs FM signals with different duty ratios, which indicate various operating statuses and fault conditions. The LED pin can be directly connected to the VIN port through pull -up resistors, but an external pull-down resistor is required to reduce the voltage stress of the LED pin. As shown in Figure 22, the LED pin outputs various signals by controlling the internal MOSFET. Once the MOSFET is turned on, the current is injected to AGND through the internal integrated resistor, where its resistance value is approximately 3.7kΩ. Figure 25 shows the recommended LED connection circuit.

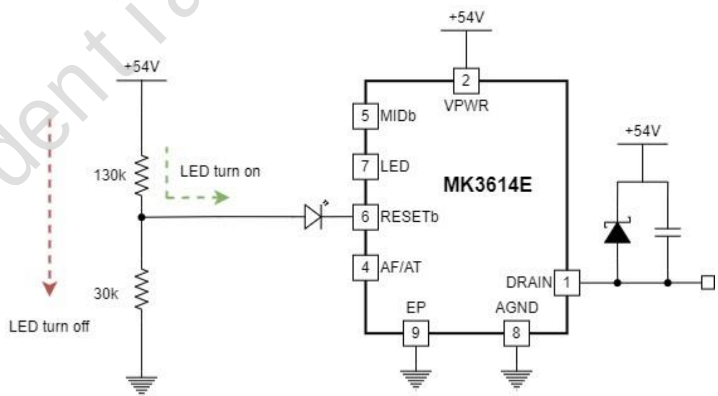


Figure 25. Recommended LED connection circuit

The following table lists LED pin states which indicate various operating statuses and fault conditions of the MK3614E.

Table 2. LED pin functions

LED Indication	Status	Note
LED on	Port successfully powered at requested power level	The MOSFET that controls the LED output is turned on.
LED off	Looking for a valid detection signature	The MOSFET that controls the LED output is turned off.
LED blinking only several times	Error condition, such as OCP, ICUT, port short fault, OTP	The MOSFET that controls the LED output is switched on and off several times, then off.

9. Application Examples

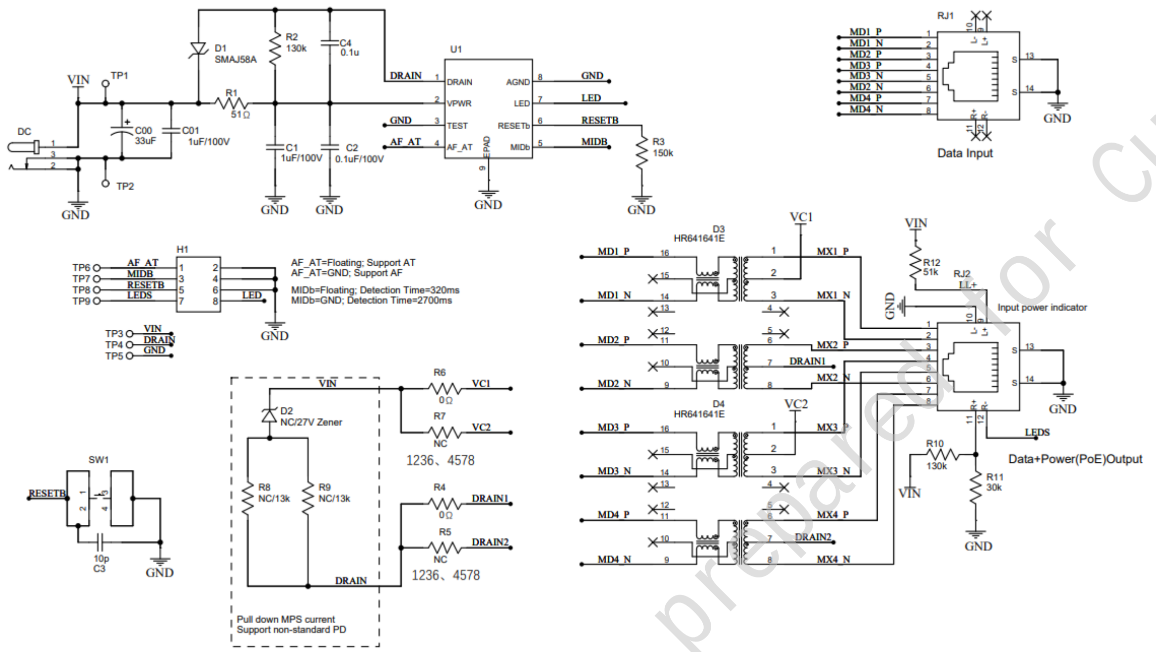


Figure 26. Application Schematic Example

10. Power Supply Recommendations

11. Layout

11.1 Layout Guidelines

To achieve high performance of the MK3614E, the following layout tips must be followed.

1. At least one low-ESR ceramic bypass capacitor for the VPWR pin must be used. Place the capacitor as close as possible to the MK3614E VPWR pin.
2. The unidirectional TVS connected between VPWR and DRAIN must be employed to prevent an external lightning strike and surge current from damaging the chip.
3. The recommended voltage of the LED pin is not higher than 30V and the current does not exceed 1mA, otherwise it may damage the pin. The pin voltage can be reduced by a pull-down resistor divider.
4. TEST pin is recommended to be tied to GND, and thermal pad is used for chip heat dissipation.
5. Use short, wide traces whenever possible for high power paths.

11.2 Layout Example

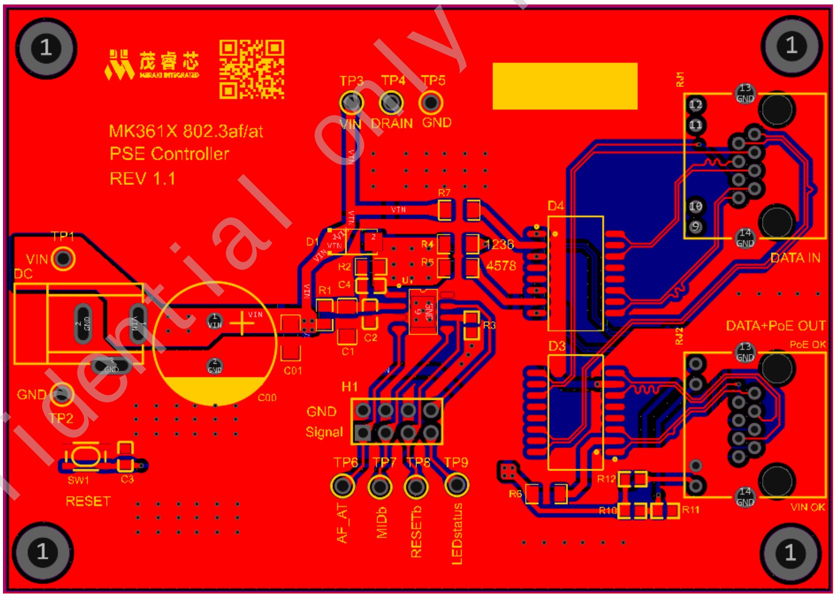


Figure 27. Evkit Layout (Tope Layer)

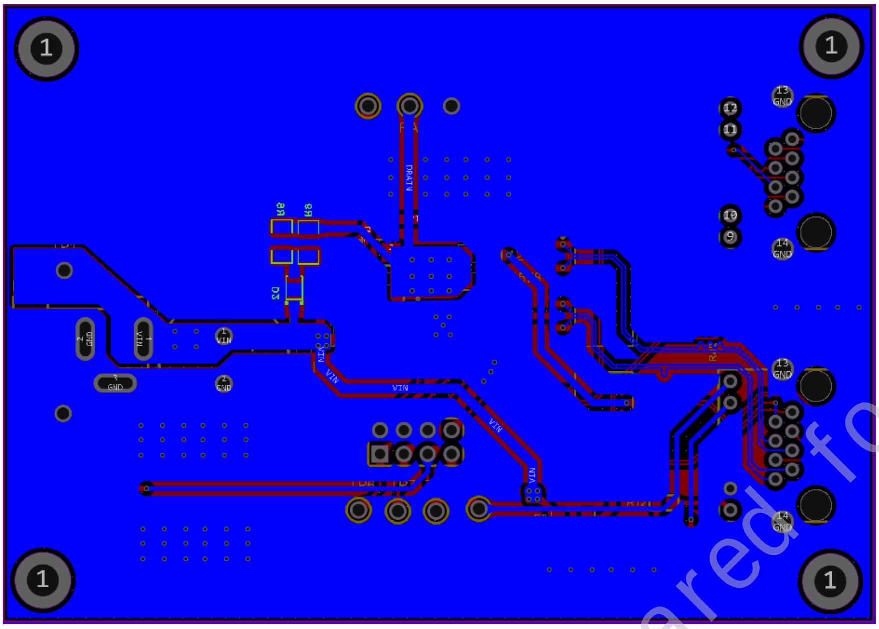


Figure 28. Evkit Layout (Bottom Layer)

12. Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device to not meet its published specifications.

13. Mechanical, Packaging

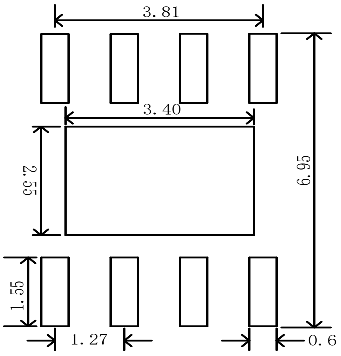


Figure 29. Recommended Land Pattern (mm)

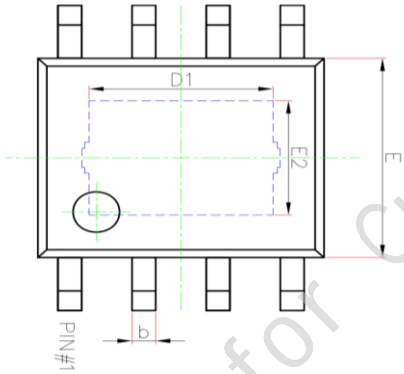


Figure 30. MK3614E Top View

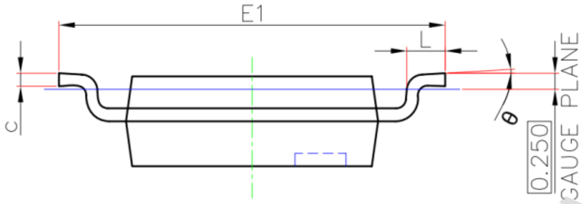


Figure 31. MK3614E Side View

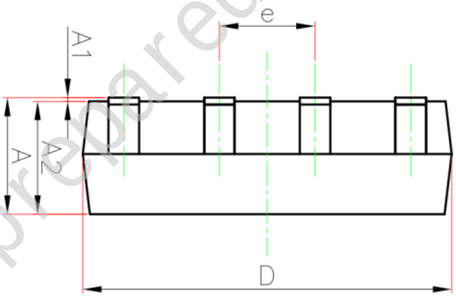
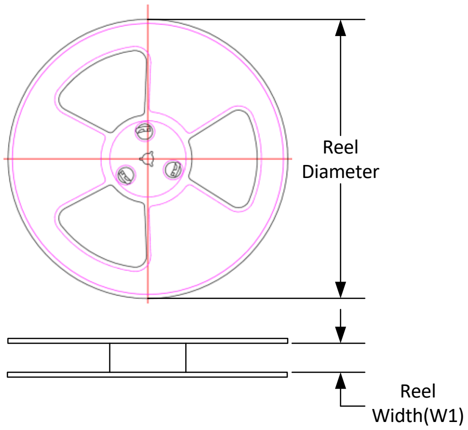


Figure 32. MK3614E Side View

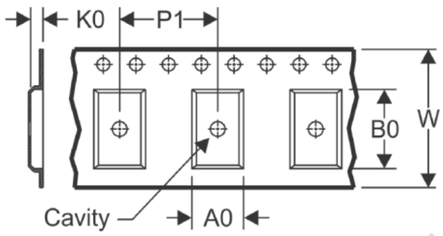
SYMBOL	Millimeter	
	MIN	NOM
A	1.300	1.700
A1	0.000	0.100
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
D1	3.050	3.250
E	3.800	4.000
E1	5.800	6.200
E2	2.160	2.360
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

14. Reel and Tape Information

REEL DIMENSIONS

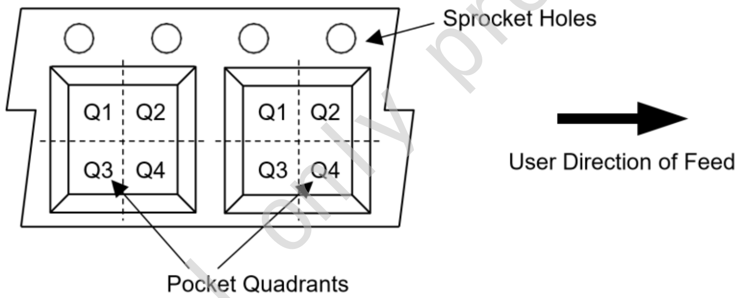


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Pins	Quantities	Reel Diameter (mm)	Reel Width W1(mm)
MK3614E	ESOP8	8	4000	330	12.4
A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
6.4	5.4	2.1	8.0	12.0	Q1

15. Tape and Reel Box Dimensions