Single-Port IEEE 802.3af/at PSE Controller

1. Description

The MK3616 family are high-density, integrated, autonomous, single Ethernet port power sourcing equipment (PSE) controller designed for use in IEEE 802.3af/at Power over Ethernet (PoE) systems. The device provides powered device (PD) detection, classification, current limit, load disconnect detection, and operating current levels. The device features intelligent protection circuitry and allows the deliverance of PD power up to 30W. The device integrates a 0.3Ω power MOSFET with an external 0.3Ω resistance R_{sns} which enables the non-PoE protocol adapter to be feasibly retrofitted into a PSE adapter with the PoE protocol only requiring a few external components.

The MK3616/3616T's LED pin is an open-drain output with simple digital logic signals to indicate operating statuses. According to the different status of LED indication, it is divided into MK3616 and MK3616T. The device supports Midspan or Endpoint mode. The Midspan mode function has a longer detection back-off time.

2. Applications

- IEEE 802.3af and 802.3at Power-Sourcing Equipment (PSE)
- Power over Ethernet Switches/Routers
- IP Phone Systems
- IP Camera Systems
- 5G Small Cells

3. Features

- IEEE 802.3af and 802.3at compatible
- Fully autonomous operation, no external controller required
- Up to 30W for PSE Applications
- Adjustable output power by R_{sns}
- 0.2mA standby current (Midspan mode)
- Integrated an 80V 0.3Ω power MOSFET
- Multi-point detection
- Support up to Class 3 (AF mode) and Class 4 (AT mode)
- Supports reset operation
- LED status indication
- Supports Midspan and Endpoint modes
- External current sense resistor
- 8-pin ESOP-8 package with thermal pad

4. Typical Application

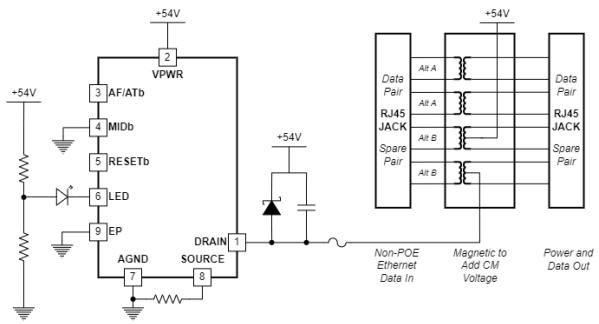
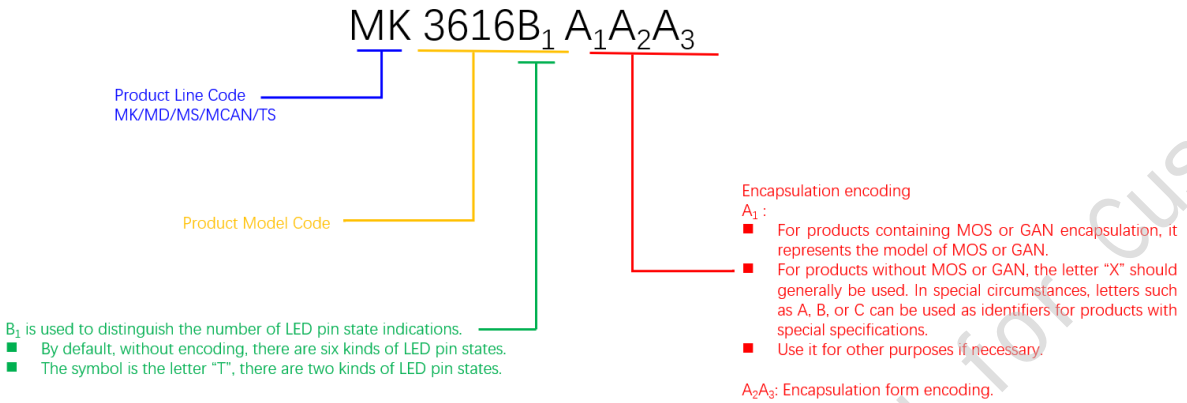


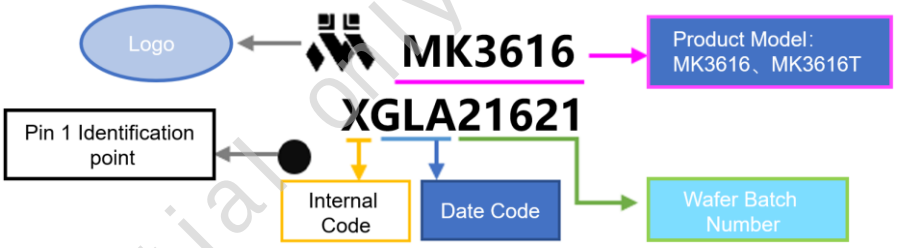
Figure 1. Typical Application Diagram for 802.3af Midspan Configuration

5. Order Information



Order Part Number	Package Type	Package Qty	Eco Plan	MSL	Single-Chip Weight	LED pin state
MK3616XAD	ESOP-8	4k/ reel	RoHS & Green	MSL-3	70mg	6
MK3616TXAD	ESOP-8	4k/ reel	RoHS & Green	MSL-3	70mg	2

6. Pin Configuration and Functions



(Please refer to MRX-DM-SCM-04 for detailed rules)

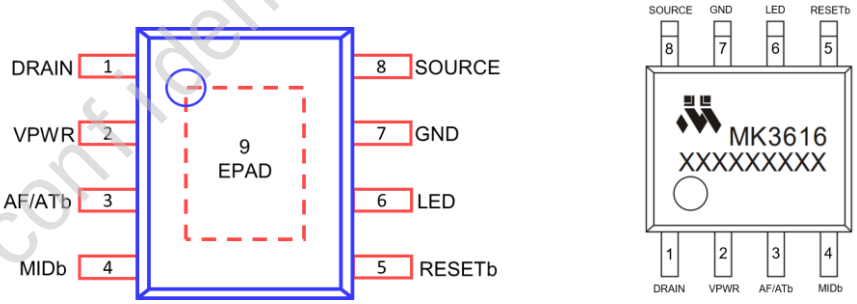


Figure 2. Pin Function (top view)

Table 1. Pin Functions

Pin		I/O	Description
NO.	Name		
1	DRAIN	Analog input	MOSFET drain output.
2	VPWR	Analog Power Input	Positive PoE voltage (+44V to 57V) relative to AGND.
3	AF/ATb	Digital Input	Pull up to internal VDD rail with 10μA current. Connect to AGND for AT configuration, leave floating for AF configuration.
4	MIDb	Digital Input	Pull up to internal VDD rail with 10μA current. Connect to AGND to set 2.7 seconds detection backoff time (Midspan)，leave floating for Endpoint configuration.
5	RESETb	Digital Input	Pull up to internal VDD rail with 20μA current. Active low device reset input.
6	LED	Digital Output	Open drain output pin, turn on an external LED when a PoE PD is connected and powered. Refer to LED section for more details.
7	AGND	Analog Ground	Analog ground.
8	SOURCE	Analog Output	MOSFET source output.
9	EPAD	—	Exposed pad, it should be connected to AGND, connect to power ground plane for better thermal performance.

7. Specifications

7.1 Absolute Maximum Ratings (1)

		MIN.	MAX.	Units
Input voltages	VCC VPWR, DRAIN to AGND	-0.3	80	V
	LED to AGND	-0.3	35	
	AF/ATb, SOURCE, RESETb, MIDb to AGND	-0.3	7	
Operating Junction Temperature, T_J		-40	150	℃
Storage Temperature, T_{stg}		-65	160	
Soldering Temperature (10 second), T_{sld}			260	

Note:

(1) Stresses beyond the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in "RECOMMENDED OPERATING CONDITIONS". Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 ESD Ratings

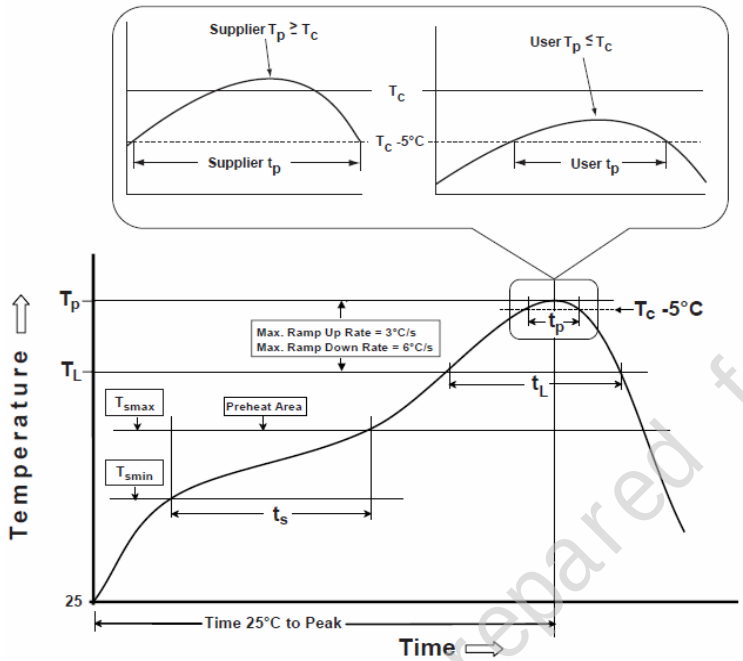
		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	1500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	2000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

7.3 Recommended Reflow Profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 ℃ 150℃ 60-120 seconds	 150 ℃ 200 ℃ 60-120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature (T_L) Time (t_L)maintained above T_L	183℃ 60-150 seconds	217℃ 60-150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the classification temp in Table2. For suppliers T_P must equal or exceed the classification temp in Table2	For users T_P must not exceed the classification temp in Table3. For suppliers T_P must equal or exceed the classification temp in Table3
Time (t_P) within 5℃ of the specified classification temperature (T_C)	20 seconds	30 seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8 minutes max
*Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum		

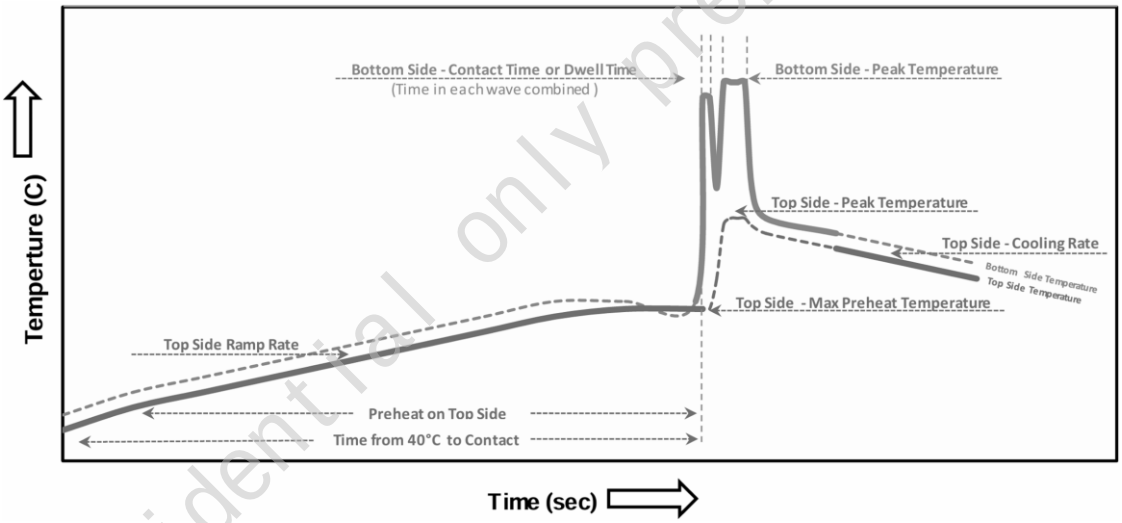
Table 2 SnPb Eutectic Process-Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5 mm	235 ℃	220 ℃
⩾2.5 mm	220 ℃	220 ℃

Table 3 Pb-Free Process-Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
<1.6 mm	260℃	260℃	260℃
1.6 mm-2.5 mm	260℃	250℃	245℃
>2.5 mm	250℃	245℃	245℃

7.4 Recommended Wave Soldering Profile



7.5 Recommended Hand Soldering and Desoldering Methods

Hand Soldering

Selection of soldering iron	Flux	Iron temperature	Welding time
Sharp tip or cutting head	Use rosin type or non-cleaning flux (with a small amount of auxiliary wetting)	Sn Pb solder: 300-350℃ Lead free solder: 350-400 ° C	2-4 seconds per solder joint (to avoid overheating and damaging components or PCBs)

skill and notes:

(1). Heat the solder pad first, then send the solder wire.

(2). Avoid forcefully pressing the soldering iron tip.

(3). Pay attention to hand soldering ESD.

Hand Desoldering

Selection of desoldering tool	Use solder suction cups and soldering irons	Use hot air gun	Skill and notes
Solder sucker and soldering iron or Hot air gun	Iron temperature: Sn Pb solder: 300-350℃; Lead free solder: 350-400 ° C; Operation: Quickly heat the solder joint and then tin suction	Temperature: 300-400℃ Airflow: medium to low (to avoid blowing small components off). Time: ≤10 seconds/solder joint. Preheating plate: 150-180 ° C (bottom heating). Hot air nozzle: 250-300 ° C (top heating).	(1). Clean the residual solder flux on the solder pads after desoldering. (2). Multilayer boards should be carefully avoided to prevent Pad detachment.

7.6 Recommended Operating Conditions

		MIN.	MAX.	Units
Recommended Operation Conditions	VPWR, DRAIN to AGND	32	60	V
	LED to AGND	0	30	
	AF/ATb, SOURCE, MIDb, RESETb, to AGND	0	5.5	
	Junction Temperature	-40	+125	℃

7.7 Thermal Information

		Value	Units
Package Thermal Resistance	θ_{JA} (Junction to ambient)	30	°C/W
	θ_{JC} (Junction to case)	10	

7.8 Electrical Characteristics

Conditions are –40°C < T_J < 125°C, V_{PWR} = 54V, Rsns = 0.3Ω unless otherwise noted. Typical values are at 25°C. All voltages are with respect to AGND unless otherwise noted.

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Power Supply Voltages						
V_{UVLO_ON}	V_{PWR} UVLO Input Voltage		25.5	28	—	V
V_{UVLO_OFF}	V_{PWR} UVLO Input Voltage		—	31	33.5	V
Power Supply Currents (1)						
I_{PWR}	V_{PWR} Supply Current	During normal operation (Detection + Idle), MIDb=Float	—	0.45	—	mA
		During normal operation (Detection + Idle), MIDb=GND	—	0.2	—	mA
Detection Specifications						
I_{DET_SC}	Detection Short Circuit Current	Measured when DRAIN is shorted to VPWR	—	1.5	5	mA
V_{PORT}	Detection Voltage When R_{DET} = 24 kΩ	V_{PWR} - V_{DRAIN}, primary detection voltage (V_{PORT_PDV})	2.8	4.2	—	V
		V_{PWR} - V_{DRAIN}, secondary detection voltage (V_{PORT_SDV})	—	8.2	10	V
T_{DET}	Detection Time		—	320	—	ms
T_{IDLE} (1)	Detection Idle Time	MIDb=Float ($V_{IDLE\_ENDPOINT}$)	—	315	—	ms
		MIDb=GND ($V_{IDLE\_MIDSPAN}$)	—	2700	—	ms

T_{DET1} (1)	Detection Time1		—	80	—	ms
T_{DET2} (1)	Detection Time2		—	80	—	ms
T_{DET3} (1)	Detection Time3		—	80	—	ms
T_{DET4} (1)	Detection Time4		—	80	—	ms
R_{GOOD} (1)	Signature Resistance		—	25	—	kΩ
R_{DET_MIN} (1)	Minimum Signature Resistance @ PD		15	17	19	kΩ
R_{DET_MAX} (1)	Maximum Signature Resistance @ PD		26.5	30	33	kΩ
C_{REJECT}	Reject Signature Capacitance		—	2.2	10	µF
Classification Specifications						
V_{CLASS}	Class Event Voltage	V_{PWR} - V_{DRAIN}, Class current between 0 and 51 mA ll,	15.5	—	20.5	V
I_{CLASS_LIM}	Class Event Current Limitation	Measured when DRAIN is shorted to VPWR	51	—	95	mA
T_{CLE}	Class Event Timing	Assigned PD Class 0, 1, 2, 3, 4	6	—	30	ms
I_{CLASS_REGION}	Classification Current Region	Class Signature 0	0	—	5	mA
		Threshold between Class Signature 0 or 1	5	—	8	mA
		Class Signature 1	8	—	13	mA
		Threshold between Class Signature 1 or 2	13	—	16	mA
		Class Signature 2	16	—	21	mA
		Threshold between Class Signature 2 or 3	21	—	25	mA

		Class Signature 3	25	—	31	mA
		Threshold between Class Signature 3 or 4	31	—	35	mA
		Class Signature 4	35	—	45	mA
		Threshold between Class Signature 4 or invalid Class	45	—	51	mA
Classification Mark Specifications						
V_{MARK}	Mark Event Voltage	V_{PWR} - V_{DRAIN}, Mark current between 0 and 5 mA	7	—	10	V
I_{MARK_LIM}	Mark Event Current Limitation	Measured when DRAIN is shorted to VPWR	51	—	95	mA
T_{ME}	Mark Event Timing	Assigned PD Class 4	6	—	12	ms
Current Limit and Overcurrent						
I_{CUT}	Overcurrent Threshold	TA=25℃, assigned PD Class 0, 1, 2, 3	—	375	—	mA
		TA=25℃, assigned PD Class 4	—	650	—	mA
T_{CUT}	Overcurrent Time Limit		50	—	75	ms
I_{INRUSH}	Output Current in POWER_UP State	TA=25℃, all assigned PD Classes, V_{PORT} > 30 V	—	425	—	mA
I_{LIM}	Current Limit	TA=25℃, Power-on, assigned PD Class 0, 1, 2, 3	—	460	—	mA
		TA=25℃, Power-on, assigned PD Class 4	—	780	—	mA
T_{LIM}	Short Circuit Time Limit	Power-on, assigned PD Class 0, 1, 2, 3	50	—	75	ms
		Power-on, assigned PD Class 4	10	—	75	ms
Load Disconnect						
I_{PORT_DIS}	DC MPS Current	Current per pairset	—	7.5	—	mA

T_{MPDO}	PD MPS Dropout Time Limit		300	—	400	ms
MOSFET On Resistance						
R_{DSON}	FET Resistance	100mA drain to source current	—	290	—	mΩ
Digital Pin Characteristics						
V_{IL}	Input Low Voltage	AF/ATb, RESETb, MIDb	—	—	1	V
V_{IH}	Input High Voltage	AF/ATb, RESETb, MIDb	2	—	—	V
I_{LK}	Input Leakage	AGND < VIN < VDD, AF/ATb, RESETb, MIDb	-1	—	1	μA
I_{PU}	Pullup Current to VDD	AF/ATb, MIDb = 0V	-13	-10	-7	μA
I_{PU}	Pullup Current to VDD	RESETb = 0V	-26	-20	-14	μA
Over Temperature Protection (1)						
T_{RISE}	Rising Threshold		—	180	—	℃
T_{FALL}	Recover Threshold		—	160	—	℃

Note:

(1) Values are verified by characterization on bench, not tested in production.

7.9 Typical Characteristics

Typical values are at V_{PWR} = 54V, TA = 25°C, Endpoint mode with a Class 0 PD, unless otherwise noted.

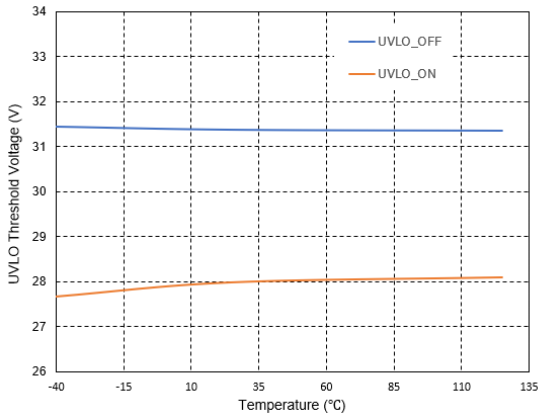


Figure 3. V_{PWR} UVLO Threshold Voltage vs. Temperature

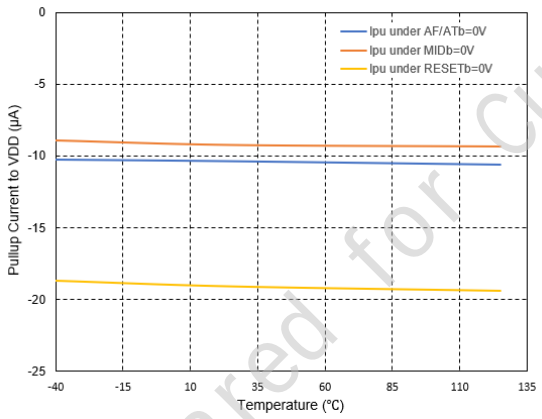


Figure 4. Digital Pin Pullup Current to VDD

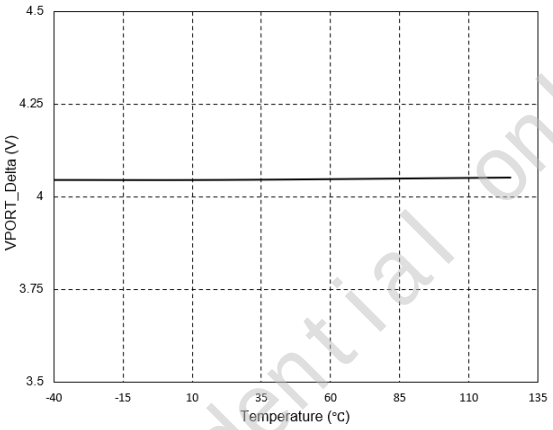


Figure 5. Voltage Difference Between Detection Points vs. Temperature

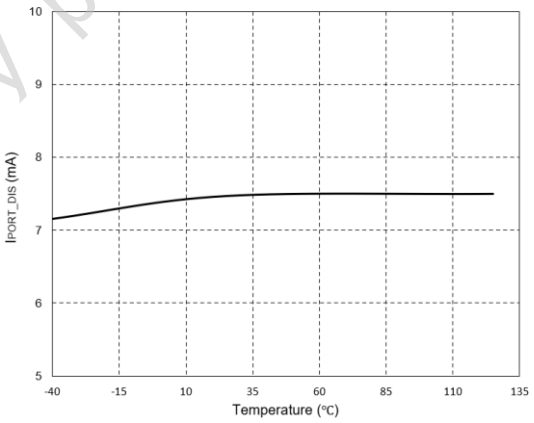


Figure 6. DC Maintain Power Signature

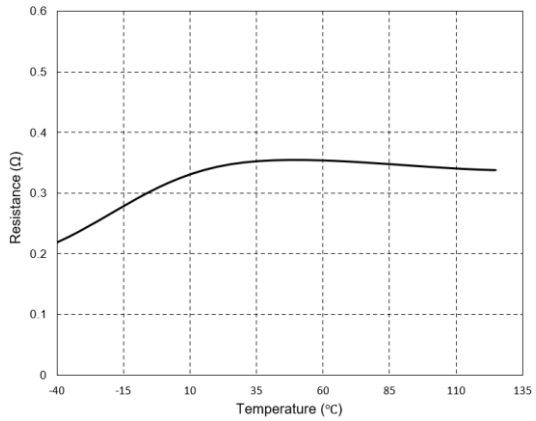


Figure 7. Internal FET Resistance vs. Temperature

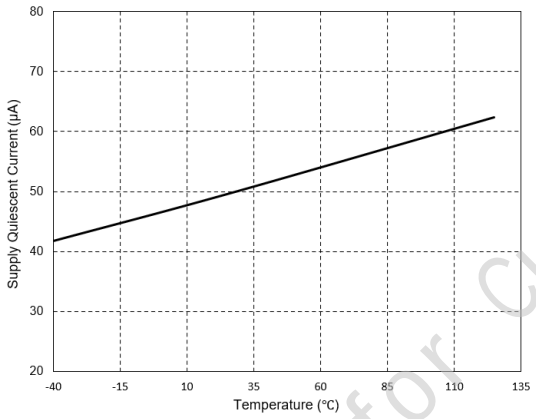


Figure 8. VPWR Current vs. Temperature (RESETb = 0V)

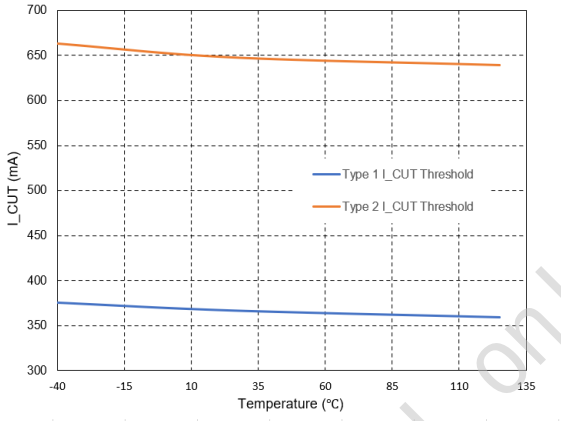
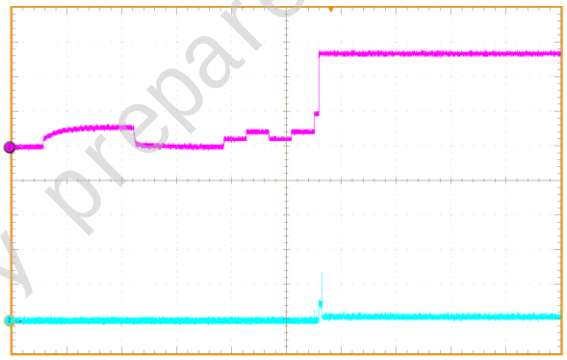
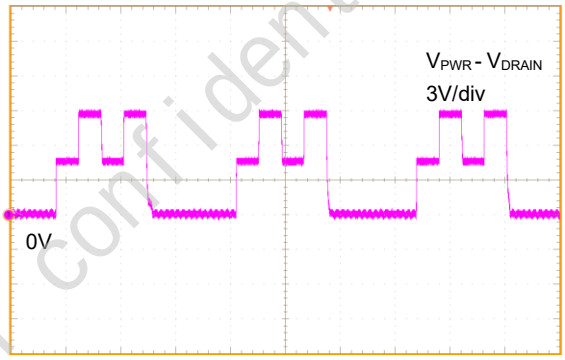


Figure 9. Overcurrent Threshold vs. Temperature



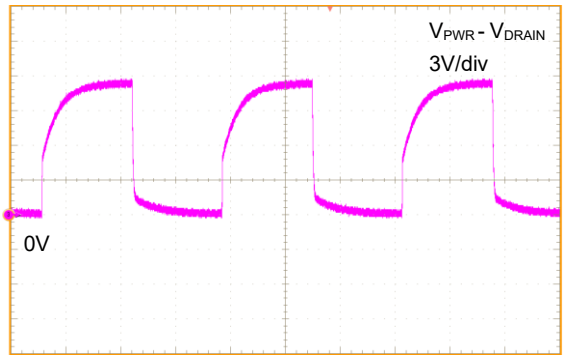
Time(200ms/div)

Figure 10. Startup with a valid PD



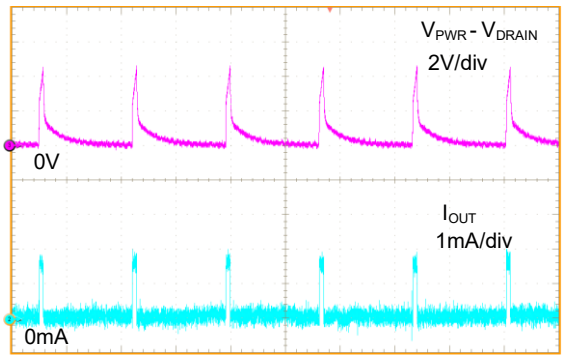
Time(200ms/div)

Figure 11. Detection with invalid PD (33kΩ)



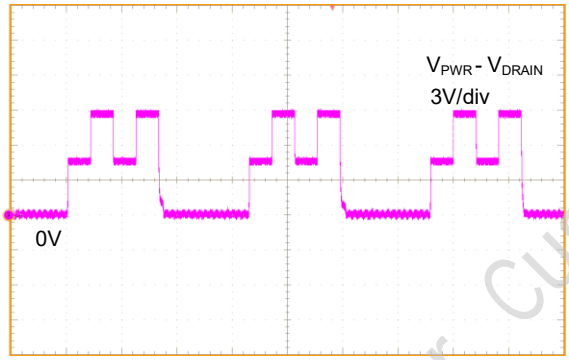
Time(200ms/div)

Figure 12. Detection with invalid PD (Open)



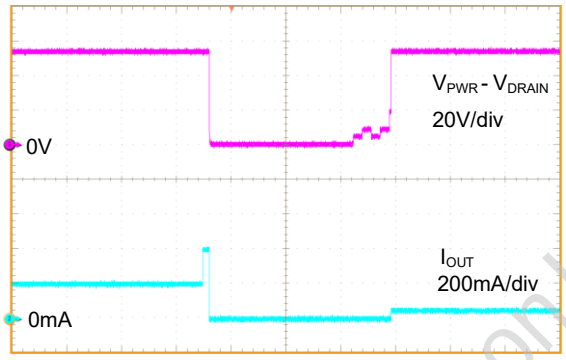
Time(200ms/div)

Figure 13. Detection with invalid PD (24kΩ and 10µF)



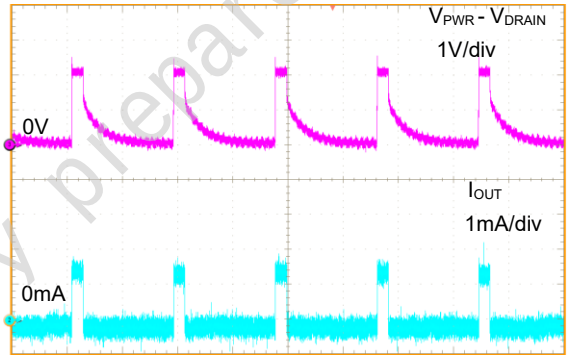
Time(200ms/div)

Figure 14. Detection with invalid PD (15kΩ)



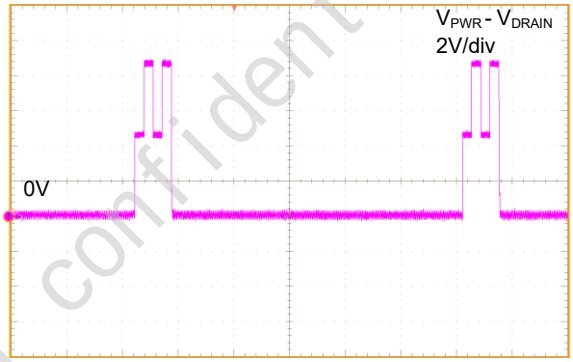
Time(500ms/div)

Figure 15. Overcurrent restart delay



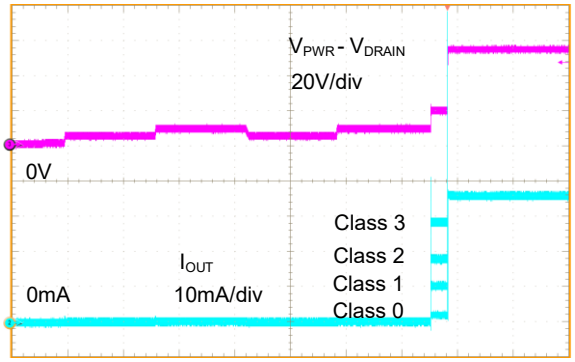
Time(200ms/div)

Figure 16. Detection with output shorted



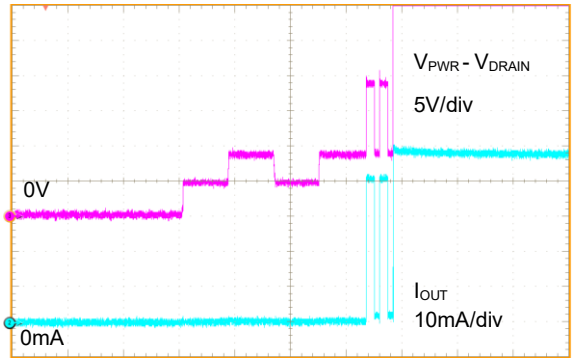
Time(500ms/div)

Figure 17. Detection in Midspan with invalid PD (15kΩ)



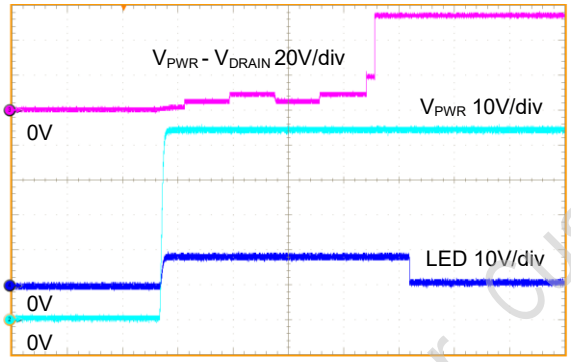
Time(50ms/div)

Figure 18. Classification with different PD classes (0 to 3)



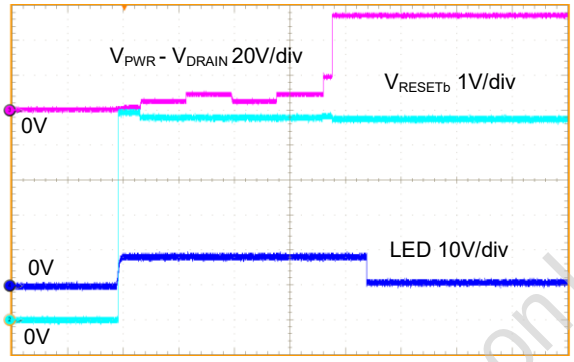
Time(100ms/div)

Figure 19. Classification with PD Class 4



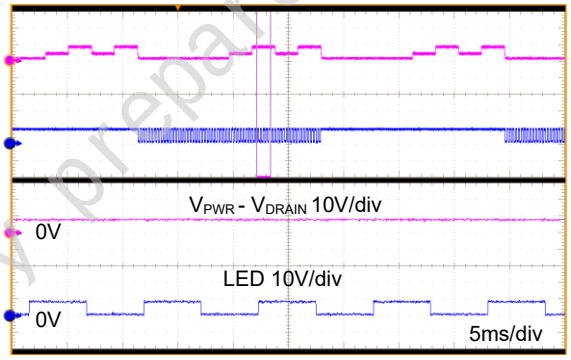
Time(100ms/div)

Figure 20. MK3616 LED function of the PD powered from V_{PWR}



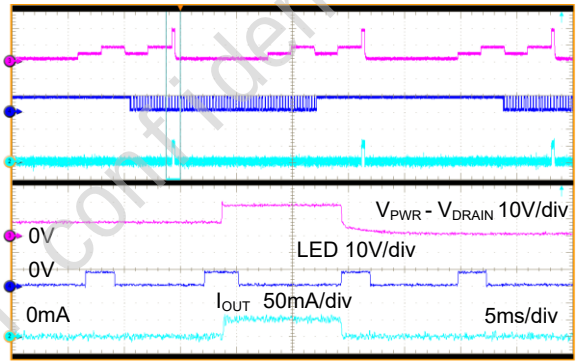
Time(100ms/div)

Figure 21. MK3616 LED function of the PD powered from V_{RESETb}



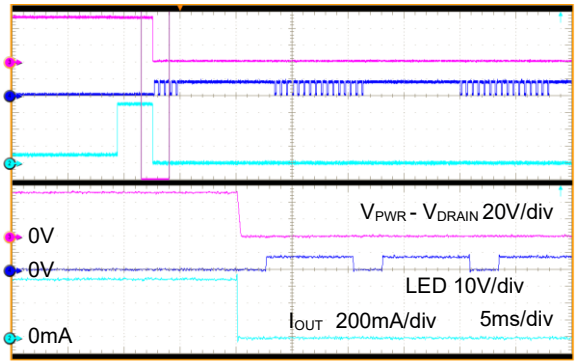
Time(200ms/div)

Figure 22. MK3616 LED function of detection error（R_{small}）



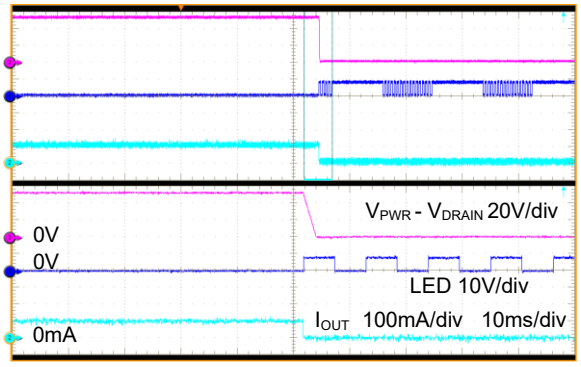
Time(200ms/div)

Figure 23. MK3616 LED function of classification error



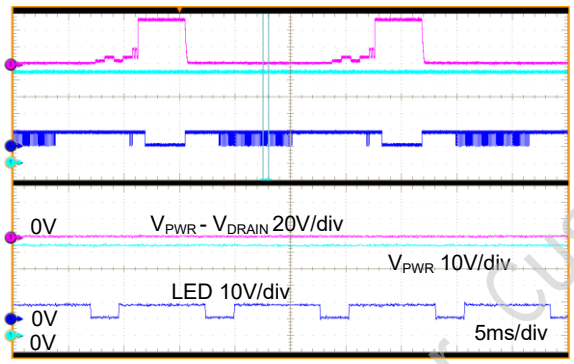
Time(200ms/div)

Figure 24. MK3616 LED function of Port Current Protection（I_{CUT}）



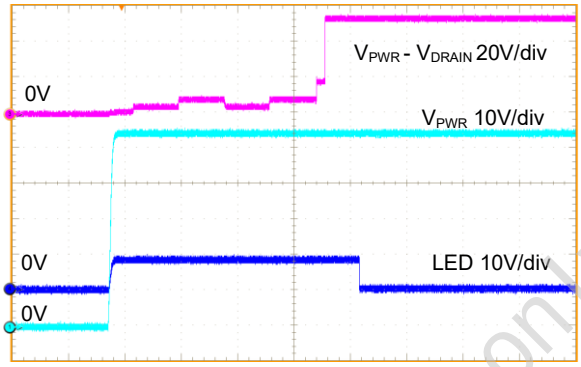
Time(200ms/div)

Figure 25. MK3616 LED function of Over Temperature Protection



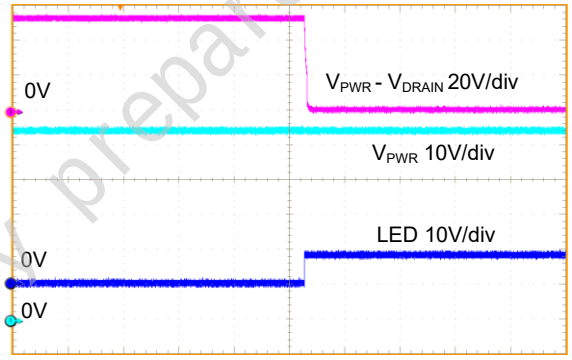
Time(500ms/div)

Figure 26. MK3616 LED function of Maintain Power Signature



Time(100ms/div)

Figure 27. MK3616T LED function of the PD powered from V_{PWR}



Time(100ms/div)

Figure 28. MK3616T LED function of Looking for a valid detection Signature

8. Detailed Description

8.1 Overview

The MK3616 family are high-density, integrated, autonomous, single Ethernet port power sourcing equipment (PSE) controller designed for use in IEEE 802.3af/at Power over Ethernet (PoE) systems. The device provides powered device (PD) detection, classification, current limit, load disconnect detection, and operating current levels. The device features intelligent protection circuitry and allows the deliverance of PD power up to 30W. The device integrates a 0.3Ω power MOSFET with an external 0.3Ω resistance R_{sns} which enables the non-PoE protocol adapter to be feasibly retrofitted into a PSE adapter with the PoE protocol only requiring a few external components. The MK3616/3616T's LED pin is an open-drain output with simple digital logic signals to indicate operating statuses. According to the different status of LED indication, it is divided into MK3616 and MK3616T. The device supports Midspan or Endpoint mode. The Midspan mode function has a longer detection back-off time.

8.2 Functional Block Diagram

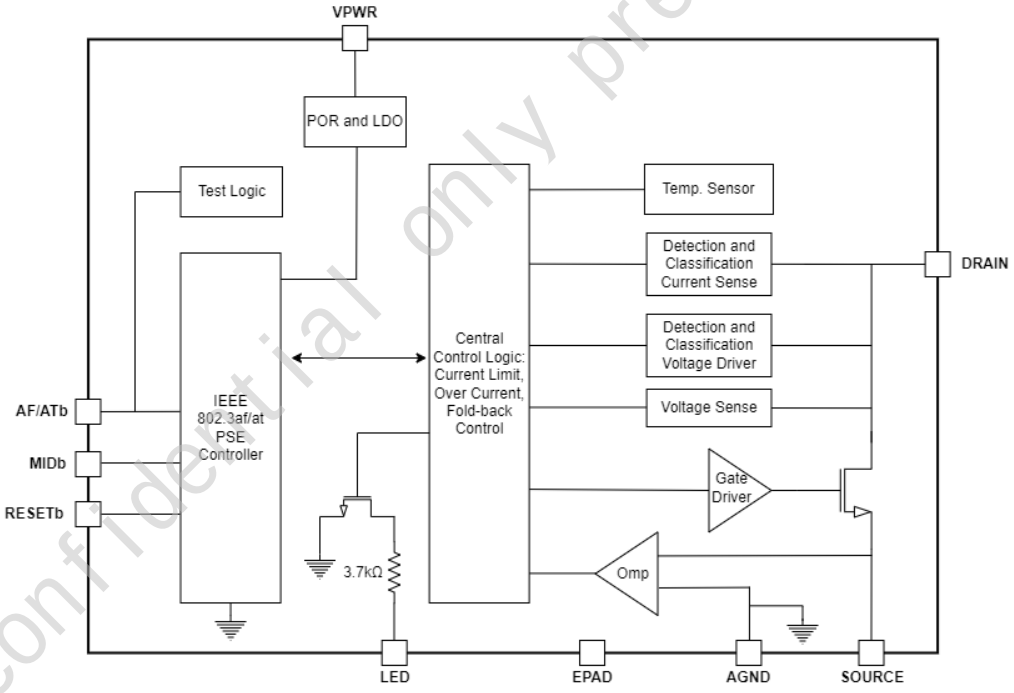


Figure 29. Block Diagram

8.3 Feature Description

8.3.1 RESET

The MK3616/3616T is reset by power-up and hardware reset. Reset condition is cleared once V_{PWR} rises above the UVLO threshold. The MK3616/3616T's RESETb pin is tied to internal VDD through a pull-up resistance. If the RESETb pin is driven low (> 110μs, typ.), the MK3616/3616T is reset. Once in the reset state, the port output and LED pull low function are disabled. At the end of a reset event, the MK3616/3616T latches in the status of AF/ATb and MIDb input signals. During normal operation, changes of the AF/ATb and MIDb inputs are ignored, and these inputs can only be changed at any time prior to the end of a reset state.

8.3.2 Midspan Mode

The MK3616/3616T supports Endpoint or Midspan PSE network configuration. In Midspan mode, when failed detections occur, the device waits about $V_{IDLE\_MIDSPAN}$ before attempting to detect again. Like the RESETb pin, MIDb pin is also tied to internal VDD through a pull-up resistance. The device is configured as Endpoint mode by default unless the MIDb pin is driven low.

8.3.3 PD Detection and Classification

The detection function of the MK3616/3616T is the most important, which determines whether the remote equipment connected to the PSE can receive power. To avoid false detection in noisy environments, the MK3616/3616T detects a PD by using a robust 4-point detection algorithm to reliably determine the signature resistance of the PD. During detection phase, the MK3616/3616T keeps the internal MOSFET off and drives probe voltages with two different levels through the DRAIN pin. The device uses a specific algorithm to calculate the PD signature resistance by sampling the current injected into the port. Once the detection result is RGOOD, the MK3616/3616T will perform Physical Layer classification by driving a class probe to determine the PD's class signature. The number of class events and mark events determines the PD requested power. Figure 30 shows a timing diagram of PD detection and classification for a Type 1 PSE powering a Type 1 PD. In this example, the MK3616/3616T produces one class event to a Type 1 PD without any mark event. As shown in Figure 31 two class events and two-mark events are driven by the MK3616/3616T for a Type 2 PSE powering a Class 4 PD.

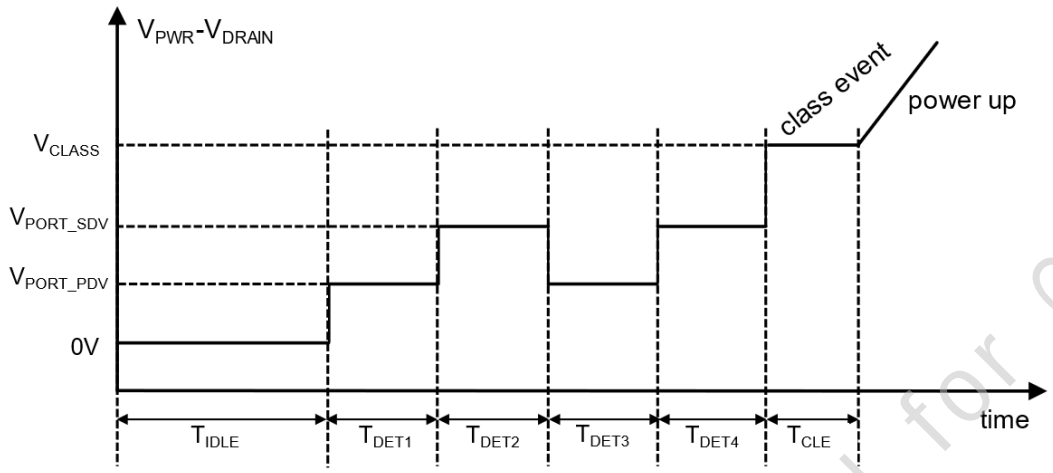


Figure 30. Type 1 Detection, Classification, and Port Power-Up Sequence

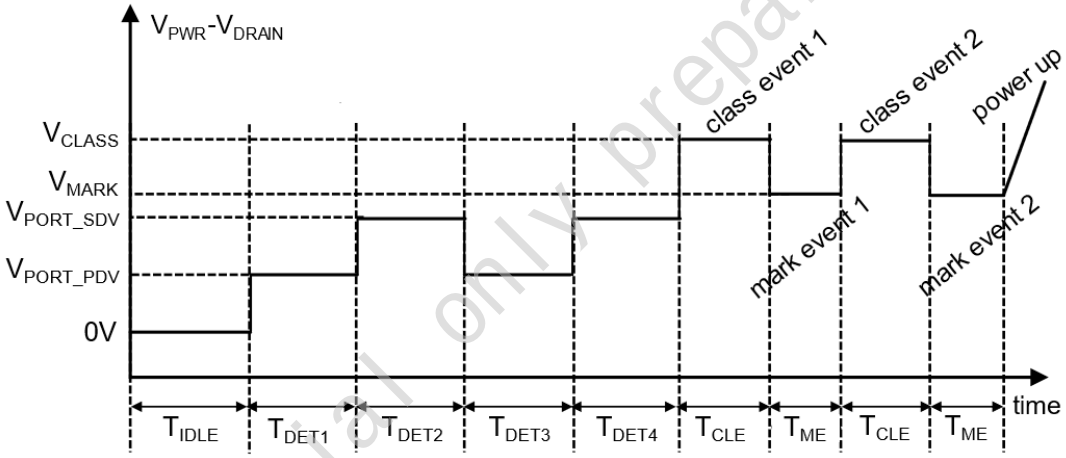


Figure 31. Type 2 Detection, Classification, and Port Power-Up Sequence

8.3.4 Inrush

After classification, if the MK3616/3616T decides to power the PD, it will first go through the inrush phase. During inrush, the PSE limits the amount of current being delivered for at least 60ms. Between 1ms and 60ms after power-on, the inrush current of the MK3616/3616T is limited to a typical value of 425mA.

8.3.5 Operating Power

During a nominal powering state, the MK3616/3616T checks abnormal conditions, including overcurrent, PD disconnection, and short-circuits. Meanwhile, the MK3616/3616T assigns the class required for PD to PD. The MK3616/3616T achieves the purpose of distributing power by controlling the current called I_{CUT}. Once the current exceeds the I_{CUT} at least T_{CUT}, the MK3616/3616T immediately cuts off the power and goes through detection phase.

8.3.6 Maintain Power Signature

When the MK3616/3616T is supplying power to a PD, the MK3616/3616T keeps monitoring the current drawn to make sure that the PD is still connected. The minimum current that the PD must draw to avoid being disconnected is named the Maintain Power Signature (MPS). The MK3616/3616T is designed to remove power when the MPS is absent for at least T_{MPDO}, ensuring that disconnected cables do not remain powered. To further reduce minimum standby power consumption for PoE systems, the MK3616/3616T only requires that PD must draw a current above I_{PORT_DIS} for at least T_{MPS} with no more than T_{MPDO} between pulses.

8.3.7 Current Limit and Voltage Foldback

The MK3616/3616T work with an external current-sensing resistor connected between the internal MOSFET and AGND to monitor the loop current. During normal operating conditions, the current running through the current-sensing resistor never exceeds the threshold ILIM. Otherwise, the internal feedback circuit regulates the driver voltage of the MOSFET to limit the current. Besides, the MK3616/3616T senses the DRAIN voltage and regulates the current-limit value, which helps to reduce the internal MOSFET power dissipation.

8.3.8 LED Signals

The LED pin is open-drain output. The pin outputs indicate operating statuses. The LED pin can't be directly connected to the VIN port through pull-up resistors, while an external pull-down resistor is required to reduce the voltage stress of the LED pin. As shown in Figure 29 the LED pin outputs various signals by controlling the internal MOSFET. Once the MOSFET is turned on, the current is injected to AGND through the internal integrated resistor, where its resistance value is approximately 3.7kΩ. Figure 32 shows the recommended LED connection circuit.

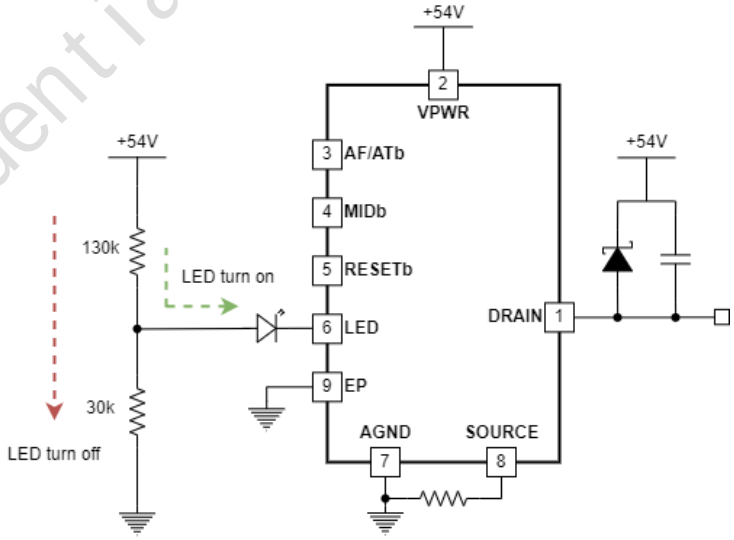


Figure 32. Recommended LED connection circuit

According to the different state of LED indication, it is divided into MK3616 and MK3616T. The following table lists LED pin states which indicate various operating statuses and fault conditions of the MK3616 and MK3616T.

Table 4. LED pin functions of MK3616

LED Indication	Status	Note
LED on	Port successfully powered at requested power level	The MOSFET that controls the LED output is turned on.
LED blinking slowly	Looking for a valid detection signature	≈1Hz with 100Hz modulation： 75% LED pin high duty：maintain power signature (MPS) 50% LED pin high duty：detection error (Rbig, Rsmall, Cbig) 25% LED pin high duty ：classification error
LED blinking quickly	Error condition, such as port overload	≈3Hz with 100Hz modulation： 75% LED pin high duty：OCP, port short fault, ICUT 50% LED pin high duty：OTP

Table 5. LED pin functions of MK3616T

LED Indication	Status	Note
LED on	Port successfully powered at requested power level	The MOSFET that controls the LED output is turned on.
LED off	Looking for a valid detection signature	The MOSFET that controls the LED output is turned off.

9. Application Examples

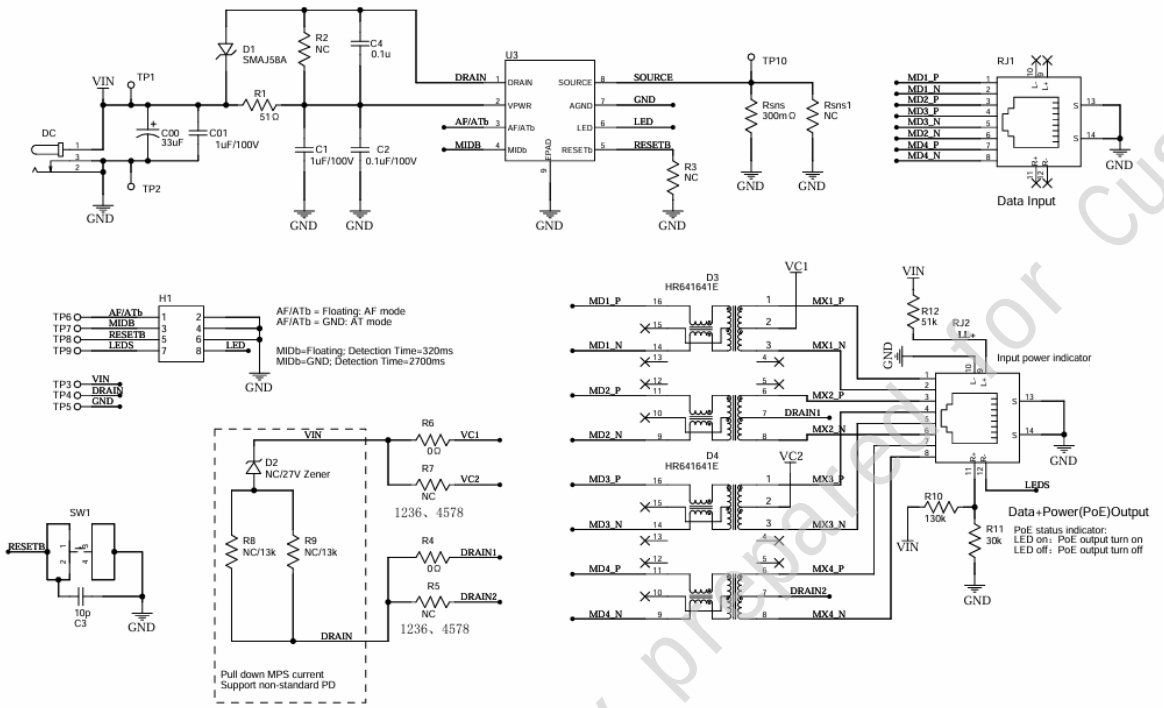


Figure 33. Application Schematic Example

10. Power Supply Recommendations

11. Layout

11.1 Layout Guidelines

To achieve high performance of the MK3616/3616T, the following layout tips must be followed.

1. At least one low-ESR ceramic bypass capacitor for the VPWR pin must be used. Place the capacitor as close as possible to the MK3616/3616T VPWR pin.
2. The unidirectional TVS connected between VPWR and DRAIN must be employed to prevent an external lightning strike and surge current from damaging the chip.
3. The recommended voltage of the LED pin is not higher than 30V and the current does not exceed 1mA, otherwise it may damage the pin. The pin voltage can be reduced by a pull-down resistor divider.
4. Try to maximize the copper laying area of the thermal pad to achieve better heat dissipation characteristics.
5. Use short, wide traces whenever possible for high power paths.

11.2 Layout Example

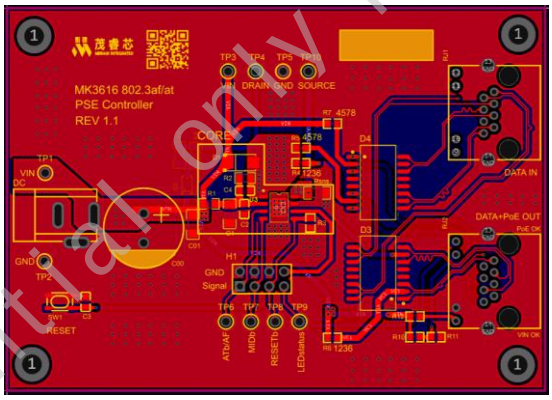


Figure 34. Evkit Layout (Top Layer)

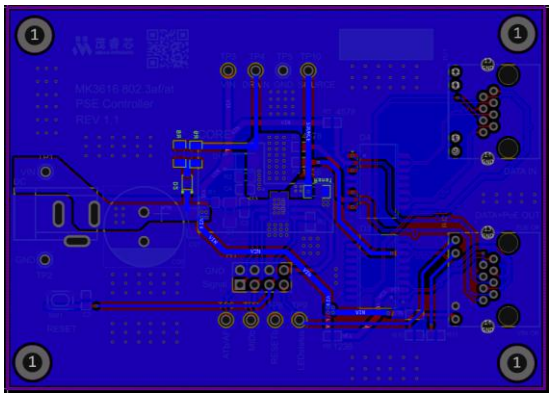


Figure 35. Evkit Layout (Bottom Layer)

12. Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device to not meet its published specifications.

13. Mechanical, Packaging

13.1 Package Size

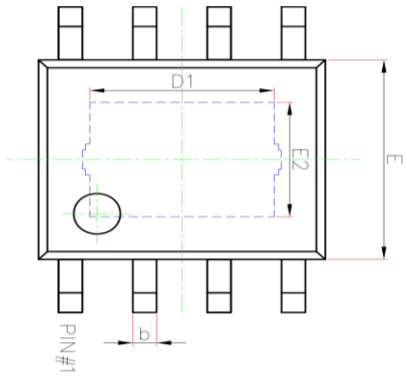


Figure 36. MK3616/3616T Top View

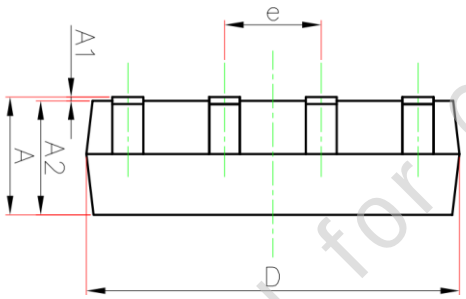


Figure 37. MK3616/3616T Side View

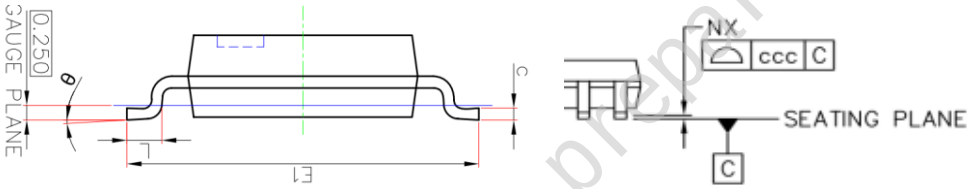


Figure 38. MK3616/3616T Side View and Coplanarity

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.30	1.50	1.70
A1	0.00	-	0.10
A2	1.35	1.45	1.55
b	0.33	-	0.51
c	0.17	-	0.25
D	4.70	4.90	5.10
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
D1	3.05	3.15	3.25
E2	2.16	2.26	2.36
e	1.27(BSC)		
L	0.4	-	1.27
θ	0°	-	8°
Coplanarity (ccc) ≤ 0.10mm			

Note:

(1) This drawing is subject to change without notice

13.2 Recommended Land Pattern

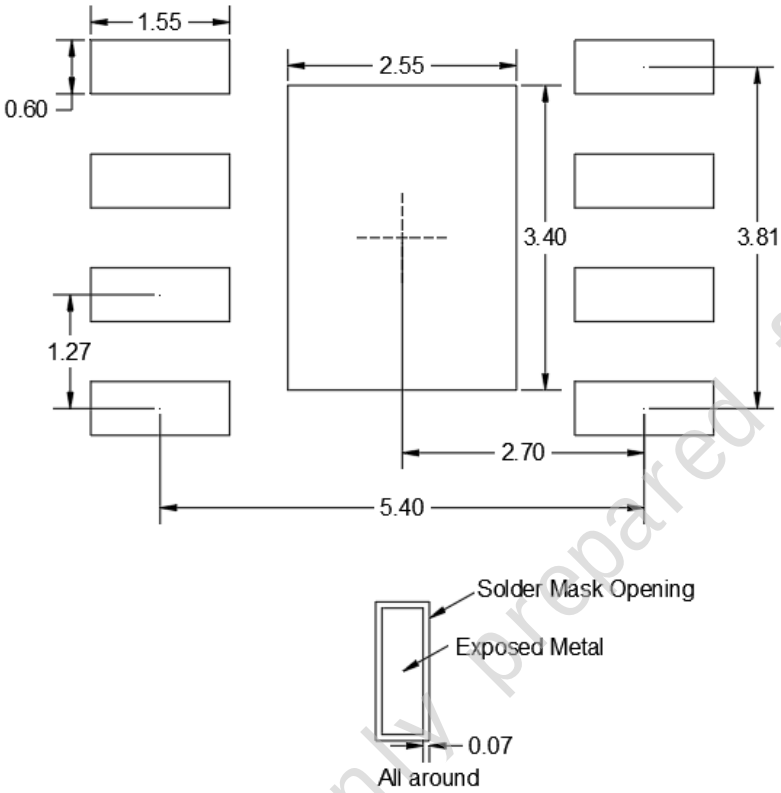


Figure 39. Recommended Land Pattern (mm)

Notes: (continued)

(1) All linear dimensions are in millimeters.

(2) It is recommended that vias under paste be filled, plugged or tented.

14. Reel and Tape Information

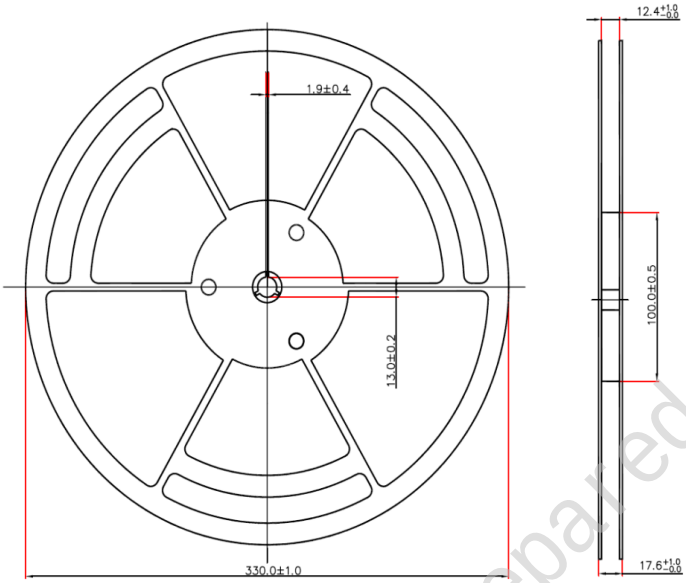
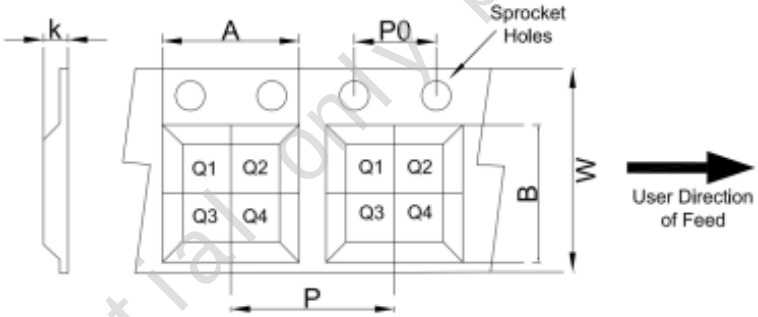


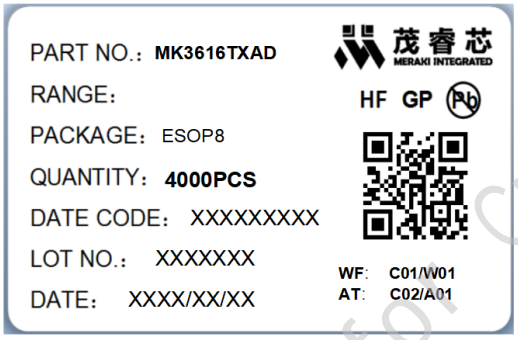
Figure 40. Reel Dimensions



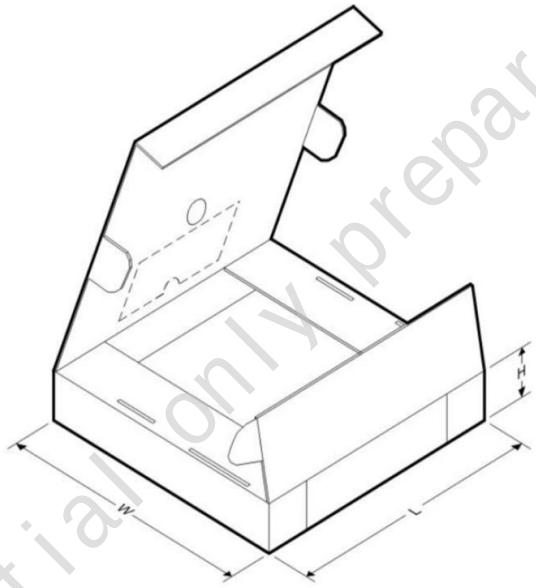
Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
MK3616/ 3616T	ESOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	12±0.1	Q1

Figure 41. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

15. Tape and Reel Box Dimensions



(Please refer to MRX-DM-QA-05 for detailed rules)



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MK3616/3616T	ESOP-8	8	8000	360	360	65

Figure 42. Box Dimensions