Dual Synchronous Rectifier Controller

1. Description

The MK1620 is a dual-channel synchronous rectifier (SR) controller for high performance switching power system. With the ultra-low quiescent current, appropriate gate drive method and independent sampling input, the MK1620 can achieve maximum efficiency under different load conditions. The MK1620 operates over a wide supply voltage range from 4.6V to 36V, which is suitable for a variety of applications. Dual-channel drivers with independent differential sampling, make it easy to use in a noisy switching system. The extremely low turn−off propagation delay time (10ns) and high sink current (~2.5A) capability of the driver reduce SR MOSFET VDS stress. The unique VG clamping circuit prevents VG from turning on by fast rising at VD pin under low VCC condition, that avoids the shoot through between primary side and secondary side during system startup.
The interlock logic with proper interlock time between two channels makes the system more reliable.

2. Applications

- AC/DC Adapters for Mobile Phone and Notebook
- Industrial Power Supplies
- Desktop All-in-one PC Power Supplies
- High Power Density Power Supplies

3. Features

- Wide VCC Voltage Range from 4.6V-36V
- Ultra-Low Quiescent Current <100uA
- Reduces the Chance of False Triggering in Discontinuous Conduction Mode (DCM)
- 10ns Fast Turn-off Delay
- VGA/VGB Clamping Circuit for Low Vth SR MOSFET
- -3V Drain Voltage Spike Tolerance
- True Differential Inputs for VDS Sensing of Each SR MOSFET
- Interlock Logic Between Two-Channel
- Adaptive Gate Drive for Maximum Efficiency
- Available in SOP-8 Package

4. Typical Application

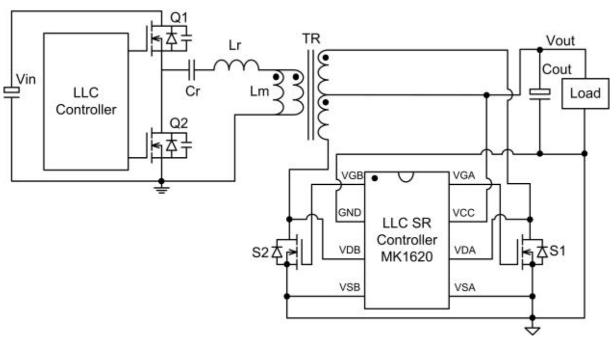
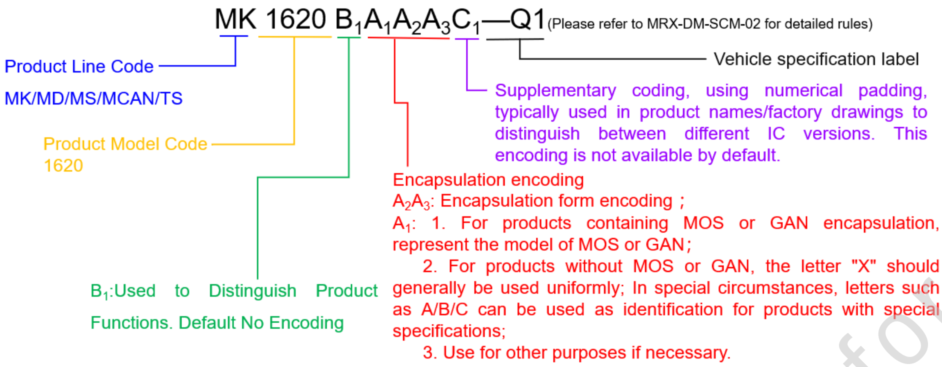


Figure 1. Typical Application Diagram

5. Order Information



Order Part Number	Package Type	Package Qty	Eco Plan	MSL	Single-Chip Weight
MK1620XAB	SOP-8	4k/ reel	RoHS & Green	MSL-3	88.6mg

6. Pin Configuration and Functions

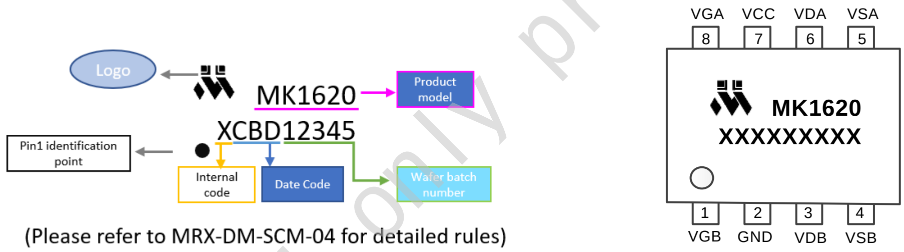


Figure 2. Pin Function (top view)

Table 1. Pin Functions

Pin		Description
NO.	Name	
1	VGB	B channel MOSFET gate drive output.
2	GND	Analog ground.
3	VDB	B channel MOSFET drain sense input.
4	VSB	B channel MOSFET source sense input.
5	VSA	A channel MOSFET source sense input.
6	VDA	A channel MOSFET drain sense input.
7	VCC	Supply voltage.
8	VGA	A channel MOSFET gate drive output.

7. Specifications

7.1 Absolute Maximum Ratings [1]

Symbol	Parameter	MIN	MAX	Units
VCC	supply voltage VCC	-0.3	38	
VGA/VGB [2]	voltage on pin VGA and VGB	-0.3	14	
VDA/VDB	drain sense voltage VDA and VDB	-1	105	V
VDA/VDB [3]	drain sense voltage VDA and VDB	-3	115	
VSA/VSB	source sense voltage VSA and VSB	-0.4	0.4	
T_J	operating junction temperature,	-40	150	
T_{stg}	storage temperature	-55	150	°C
T_{sld}	soldering temperature (10 second)		260	

Notes:

(1) Stresses beyond the “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in “RECOMMENED OPERATING CONDITIONS”. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Output pin not to be voltage driven.

(3) Repetitive Pulse<200ns.

7.2 ESD Ratings

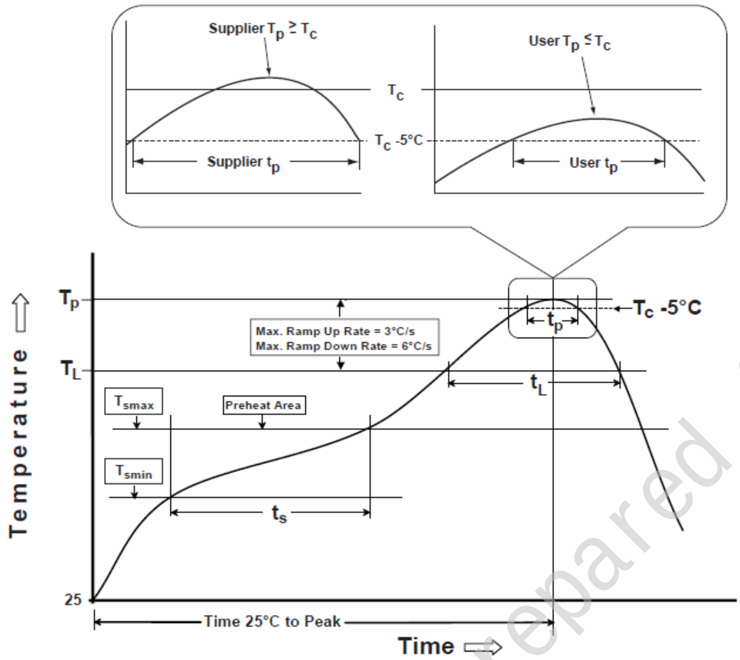
		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [2]	±2000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Reflow Profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 ℃ 150℃ 60-120 seconds	 150 ℃ 200 ℃ 60-120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature (T_L) Time (t_L)maintained above T_L	183℃ 60-150 seconds	217℃ 60-150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the classification temp in Table2 For suppliers T_P must equal or exceed the classification temp in Table2	For users T_P must not exceed the classification temp in Table3 For suppliers T_P must equal or exceed the classification temp in Table3
Time (t_P) within 5℃ of the specified classification temperature (T_C)	20 seconds	30 seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8 minutes max
*Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum		

Table 2. SnPb Eutectic Process-Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 ℃	220 ℃
⩾2.5 mm	220 ℃	220 ℃

Table 3. Pb-Free Process-Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260℃	260℃	260℃
1.6 mm-2.5 mm	260℃	250℃	245℃
>2.5 mm	250℃	245℃	245℃

7.4 Recommended Wave Soldering Profile

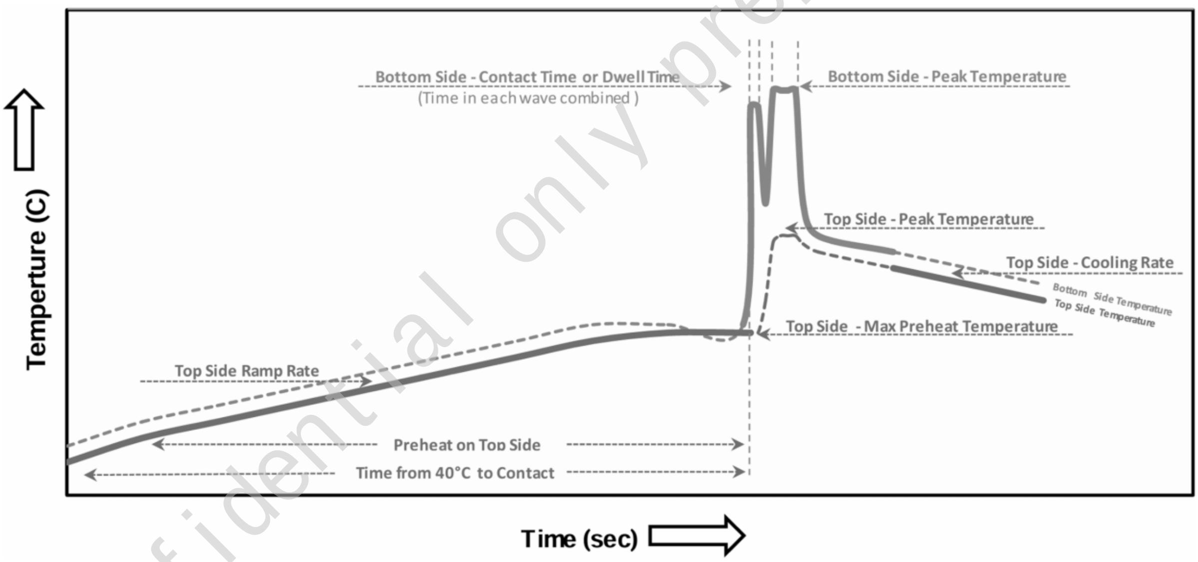


Table 4. Recommended Parameters for Solder Pot Temperatures

Profile Feature	General Profile IPC/JEDEC[1]	AIM (Recommended starting point)[2]
Tin-Lead Alloys	230 – 260 °C	230 – 260 °C
Lead-Free Alloys	260 – 290 °C	255 – 300 °C *

*Temperatures can start as low as 240°C depending on the application and alloy being used.

Table 5. Recommended Parameters for IPA-Based Fluxes – Medium to High Solids > 3.5% Typical *

Profile Feature	General Profile IPC/JEDEC[1]	Tin–Lead Alloys (Recommended starting point)[2]	Lead-Free Alloys (Recommended starting point)[3]
Top Side Ramp Up Rate	< 3 °C/ Sec.	1 - 3 °C/ Sec.	1 - 3 °C/ Sec.
Top Side Max Preheat Temperature	< 150 °C	75 – 130 °C	80 – 140 °C
Bottom Side Contact Time	< 10 Sec.	< 5 Sec.	< 8 Sec.
Top Side Cooling Rate	< 3 °C / Sec.	< 3 °C / Sec.	< 3 °C / Sec.
Time from 40°C to Contact	60 – 180 Sec.	60 – 180 Sec.	60 – 180 Sec.

* Modern low-solid fluxes including AIM “FX” series may be used with medium to high solids parameters for improved performance.

Table 6. Recommended Parameters for IPA-Based Fluxes – Low Solids < 3.5% Typical

Profile Feature	General Profile IPC/JEDEC[1]	Tin–Lead Alloys (Recommended starting point)[2]	Lead-Free Alloys (Recommended starting point)[3]
Top Side Ramp Up Rate	< 3 °C/ Sec.	1 - 3 °C/ Sec.	1 - 3 °C/ Sec.
Top Side Max Preheat Temperature	< 150 °C	75 – 110 °C	80 – 120 °C
Bottom Side Contact Time	< 10 Sec.	< 5 Sec.	< 8 Sec.
Top Side Cooling Rate	< 3 °C / Sec.	< 3 °C / Sec.	< 3 °C / Sec.
Time from 40°C to Contact	60 – 180 Sec.	60 – 90 Sec.	60 – 90 Sec.

* Most low-solid fluxes may be used with low-solids parameters for optimal performance.

Table 7. Recommended Parameters for VOC - Free

Profile Feature	General Profile IPC/JEDEC[1]	Tin–Lead Alloys (Recommended starting point)[2]	Lead-Free Alloys (Recommended starting point)[3]
Top Side Ramp Up Rate	< 3 °C/ Sec.	1 - 3 °C/ Sec.	1 - 3 °C/ Sec.
Top Side Max Preheat Temperature	< 150 °C	90 – 120 °C	90 – 140 °C
Bottom Side Contact Time	< 10 Sec.	< 5 Sec.	< 8 Sec.
Top Side Cooling Rate	< 3 °C / Sec.	< 3 °C / Sec.	< 3 °C / Sec.
Time from 40°C to Contact	60 – 240 Sec.	60 – 180 Sec.	60 – 180 Sec.

(1) The general profile data are the parameters allowable by IPC/JEDEC, and are added only as a reference.

(2) This data guideline applies to common tin-lead alloys (i.e. Sn63/Pb37, Sn62/Pb36/Ag2).

(3) This data guideline applies to common lead-free alloys (i.e. AIM REL Alloys, SAC, SN100C et.al.).

7.5 Recommended Hand Soldering and Desoldering Methods

Hand Soldering

Selection of soldering iron	Flux	Iron temperature	Welding time
Sharp tip or cutting head	Use rosin type or non-cleaning flux (with a small amount of auxiliary wetting)	Sn Pb solder: 300-350℃ Lead free solder: 350-400 ° C	2-4 seconds per solder joint (to avoid overheating and damaging components or PCBs)

skill and notes:

(1) Heat the solder pad first, then send the solder wire.

(2) Avoid forcefully pressing the soldering iron tip.

(3) Pay attention to hand soldering ESD.

Hand Desoldering

Selection of desoldering tool	Use solder suction cups and soldering irons	Use hot air gun	Skill and notes
Solder sucker and soldering iron or Hot air gun	Iron temperature: Sn Pb solder: 300-350℃; Lead free solder: 350-400 ° C; Operation: Quickly heat the solder joint and then tin suction	Temperature: 300-400℃ Airflow: medium to low (to avoid blowing small components off). Time:⩽10 seconds/solder joint. Preheating plate: 150-180 ° C (bottom heating). Hot air nozzle: 250-300 ° C (top heating).	(1). Clean the residual solder flux on the solder pads after desoldering. (2). Multilayer boards should be carefully avoided to prevent Pad detachment.

7.6 Recommended Operating Conditions

		MIN	MAX	Units
Recommended Operation Conditions	VCC supply voltage	4.6	36	V
	drain sense voltage VDA and VDB	-0.7	100	
	operating junction temperature. (T_J)	-40	125	°C

7.7 Thermal Information

		Value	Units
Package Thermal Resistance (1)	θ_{JA} (Junction to ambient)	146	°C/W
	θ_{JC} (Junction to case)	70	

Note:

(1) Measured on JESD51-7, 4-layer PCB.

7.8 Electrical Characteristics

T_A=25°C. All Voltages are measured with respect to ground (pin 2). Currents are positive when flowing into the IC, unless otherwise specified.

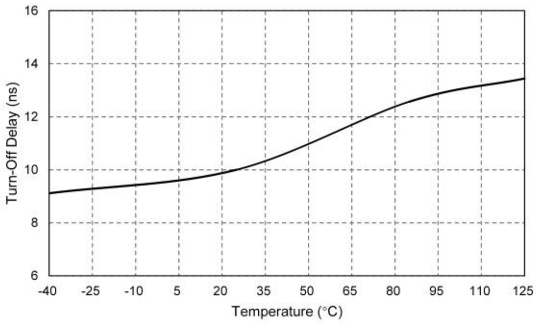
Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Supply voltage Management						
$V_{CC\text{-}ON}$	VCC UVLO rising		4.25	4.40	4.55	V
$V_{CC\text{-}OFF}$	VCC UVLO falling		4.05	4.20	4.35	V
$V_{CC\text{-}HYST}$	VCC UVLO hysteresis			0.2		V
I_{CC}	Operating supply current	VCC=12V, VDA=VDB=10V		75	100	µA
		VCC=12V VDA=VDB=0V		0.85	1.05	mA
t_{act}	Sleep-mode activation time		80	110	160	µs
Synchronous rectification sense input						
$V_{DS\text{-}reg}$	$V_{DA(B)}$ – $V_{SA(B)}$ Adjusting voltage	VCC=8V	-45	-25		mV
$V_{ON\text{-}th}$	$V_{DA(B)}$ – $V_{SA(B)}$ Turn-on threshold voltage	VCC=12V	-450	-300	-150	mV
$V_{OFF\text{-}th}$	$V_{DA(B)}$ – $V_{SA(B)}$ Turn-off threshold voltage	VCC=13V	110	150	190	mV
$T_{D\text{-}on}$	Turn-on propagation delay time	C_{LOAD} = 0nF, VD step down from 3V to -0.3V, measure VG rising to 1V	50	60	75	ns
$T_{D\text{-}off}$	Turn-off propagation delay time	C_{LOAD} = 0nF, VD step up from -0.3V to 3V, measure VG falling to 90% of $V_{G\text{-}H}$	5	10	15	ns
$T_{B\text{-}on}$	Turn-on blanking time (1)	C_{LOAD} = 0nF, VCC=12V		0.8		µs
$T_{B\text{-}off}$	Turn-off blanking time	C_{LOAD} = 0nF, VCC=12V	0.7	0.8		µs
T_d	Two-channel interlock time	C_{LOAD} = 0nF, VCC=12V	50	65	80	ns
$V_{B\text{-}off}$	$V_{DA(B)}$ – $V_{SA(B)}$Turn-off threshold during turn-on blanking time (1)			0.5		V
Gate Driver						
$V_{G\text{-}H}$(high)	Maximum gate voltage	VGA/VGB at VCC=5V	4.85	4.99	5	V
		VGA/VGB at VCC=12V	9.5	10.5	11.5	V
		VGA/VGB at VCC=24V	9.5	10.5	11.5	V

I_{VG-H}	Maximum source current (1)			-0.25		A
I_{VG-L}	Maximum sink current (1)			2.5		A
R_{sink}	Pull-down impedance (1)	I_{LOAD}= 100mA		0.9		Ω

Note:

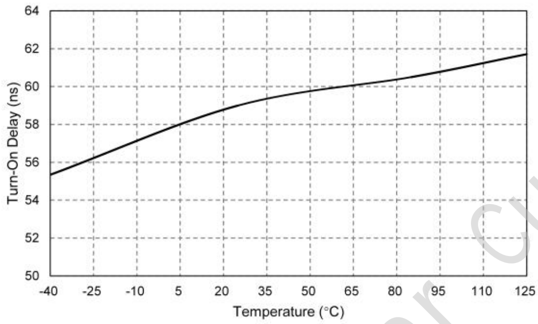
(1) Values are verified by characterization on bench, not tested in production.

7.9 Typical Characteristics



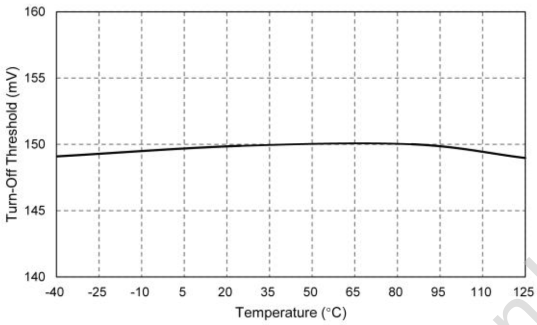
VCC=12V, C_{LOAD}=0nF

Figure 3. Turn-Off Delay vs Temperature



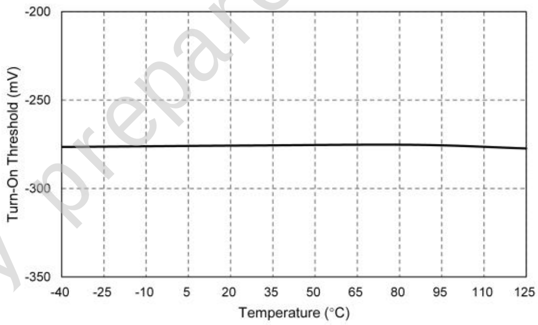
VCC=12V, C_{LOAD}=0nF

Figure 4. Turn-On Delay vs Temperature



VCC=12V, C_{LOAD}=0nF

Figure 5. Turn-Off Threshold vs Temperature



VCC=12V, C_{LOAD}=0nF

Figure 6. Turn-On Threshold vs Temperature

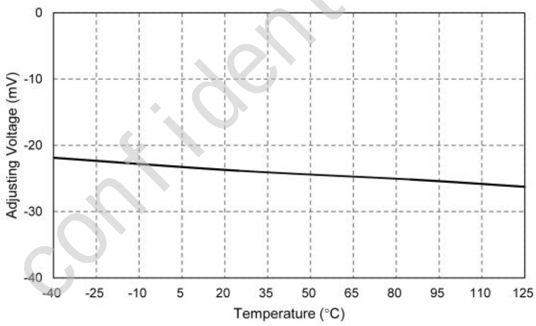


Figure 7. Adjusting Voltage vs Temperature

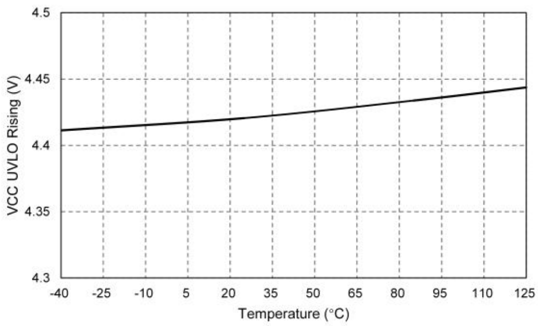


Figure 8. VCC UVLO Rising vs Temperature

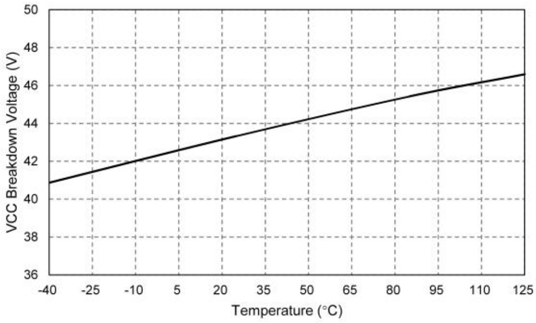


Figure 9. VCC Breakdown Voltage vs Temperature

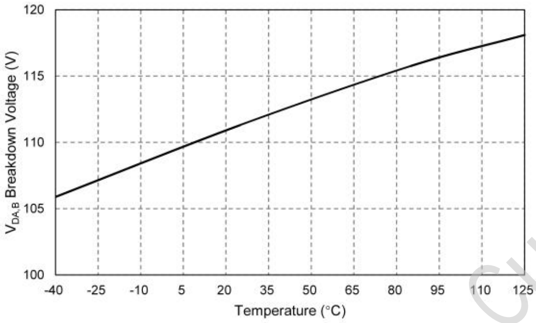
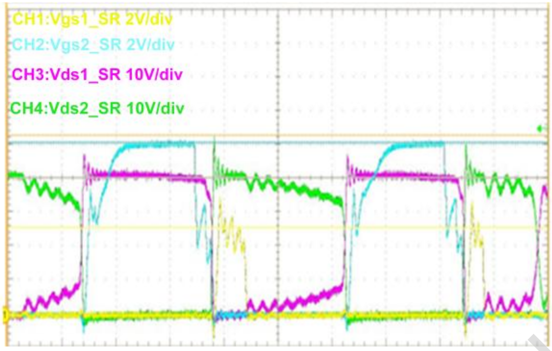
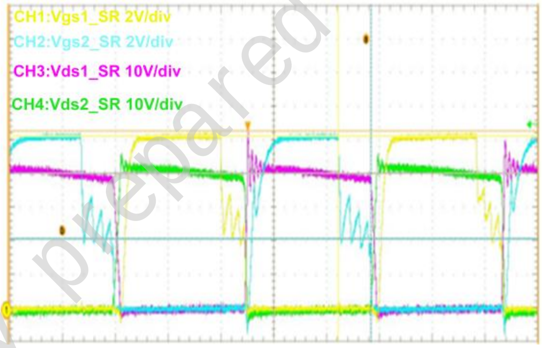


Figure 10. VDA/B Breakdown Voltage vs Temperature



Vin=230VAC, Vout=20V, Iout=0.1A

Figure 11. Operation in 300W LLC Converter

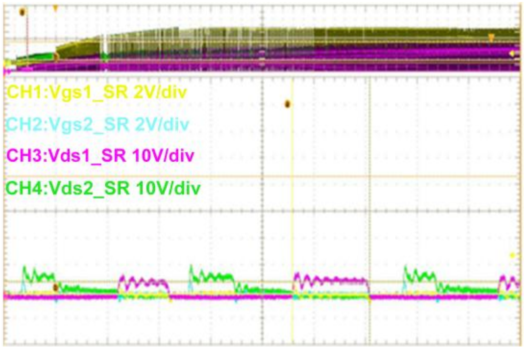


Vin=230VAC, Vout=20V, Iout=15A

Figure 12. Operation in 300W LLC Converter

Vin=230VAC, Vout=20V, Iout=1A Turn-Off

Figure 13. Operation in 300W LLC Converter



Vin=230VAC, Vout=20V, Iout=0.1A Turn-On

Figure 14. Operation in 300W LLC Converter

8. Detailed Description

8.1 Overview

The MK1620 is a dual-channel synchronous rectifier controller capable of driving two N-Channel power MOSFETs in resonant converter applications. This controller has dual differential sampling inputs to detect the voltage difference between the drain and source of each SR MOSFET.

The gate voltage is adjusted consistently with the VDS voltage. The control strategy of the chip is easy to implement and straight-forward.

The unique VG clamping circuit works well to prevent VG from turning on by quickly rising at the VD pin with no VCC. Extremely low turn−off propagation delay time (10ns) and high sink current (~2.5A) capability of the driver reduce SR MOSFET VDS stress. Internal two-channel interlock logic with proper interlock time makes the system more reliable.

8.2 Functional Block Diagram

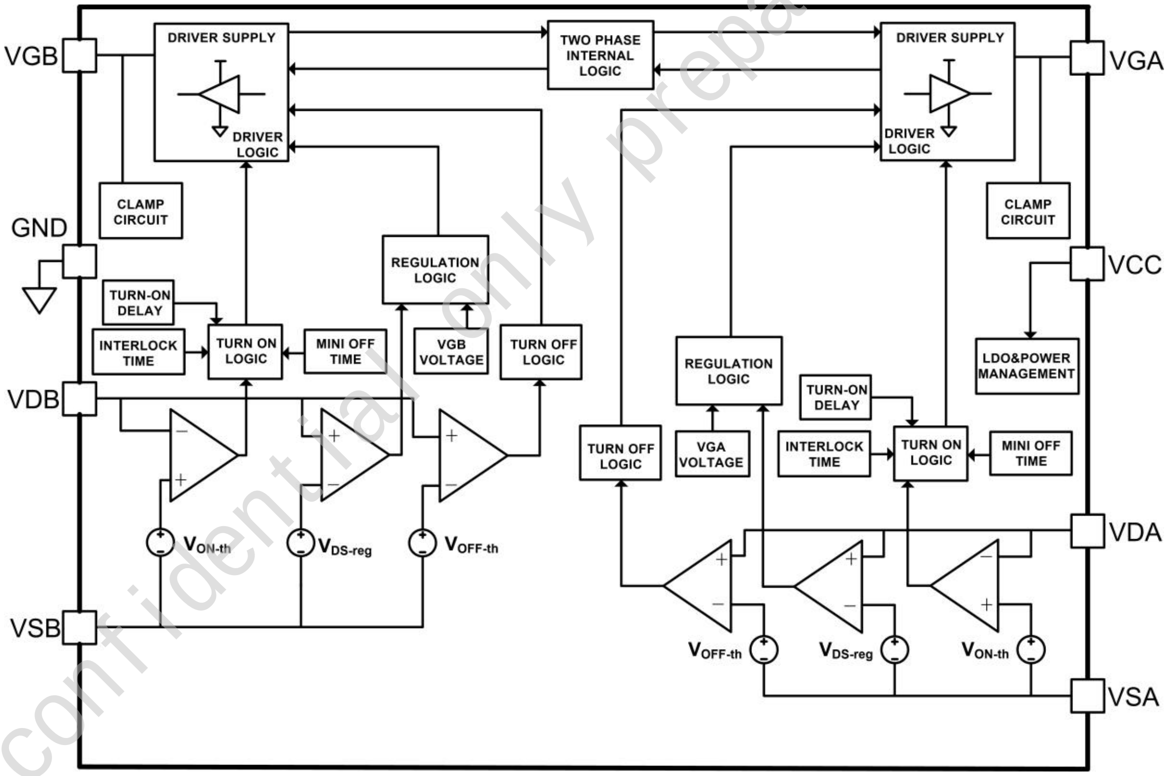


Figure 15. Block Diagram

8.3 Feature Description

8.3.1 VCC Power Supply and Undervoltage Lockout

The MK1620 operates from a supply voltage of 4.6V to 36V. This feature makes MK1620 suitable for a variety of application scenarios. For the best performance, use a typical 0.1uF decoupling capacitor as close as possible between the VCC and GND pins of MK1620. A VCC bypass capacitor (1uF to 10uF) in parallel to the decoupling capacitor is also recommended to reduce noise ripple during switching.

MK1620 has an internal undervoltage lockout (UVLO) protection feature in the VCC supply circuit blocks. When the voltage on the VCC pin exceeds $V_{CC\text{-}ON}$, the controller leaves the UVLO state and activates the SR circuitry. When VCC voltage drops to below $V_{CC\text{-}OFF}$, the controller re-enters the UVLO state.

8.3.2 Conduction Phase

When the absolute voltage difference of VDS increases from zero to above $V_{ON\text{-}th}$, the corresponding gate driver output turns on the external SR MOSFET.

After SR MOSFET turns on, a turn-on blanking time $T_{B\text{-}on}$ is required to prevent the parasitic ringing from falsely turning off SR MOSFET. During the turn-on blanking time, the turn-off threshold increases to $V_{B\text{-}off}$.

After this, the MK1620 goes into regulation mode. In this phase, MK1620 adjusts the VDS of SR MOSFET to be around $V_{DS\text{-}reg}$ by the high level of VGA/VGB voltage until the current through SR MOSFET drops to zero. See Section 9.3.2 for further description on regulation mode.

8.3.3 Turn-Off Phase

After the turn-on blanking time $T_{B\text{-}on}$, the turn-off threshold is around $V_{OFF\text{-}th}$. With a suitable regulation and turn-off strategy, the MK1620 will not turn-off prematurely, which will not cause the current to conduct for a long time through the body diode of the SR MOSFET.

With an extremely fast 10ns turn-off propagation delay and 2.5A pull-down (sink) current, the MK1620 is rapidly turned off when the current through the external SR MOSFET reaches zero.

After SR MOSFET turns off, a minimum turn-off blanking time $T_{B\text{-}off}$ is required, which helps to reduce the chance of false triggering-on in DCM.

8.3.4 Interlock Function

The MK1620 incorporates an internal interlock logic between the two drivers, which prevents the SR MOSFETs from cross conduction due to both drivers turned on at the same time.

The control diagram is shown on Figure 16. When either VGA or VGB is turned on, the other channel gate driver is blanked until channel VGA or VGB is turned off.

After either VGA or VGB is unlocked, the other channel gate driver has to be locked until the end of the interlock time (T_d).

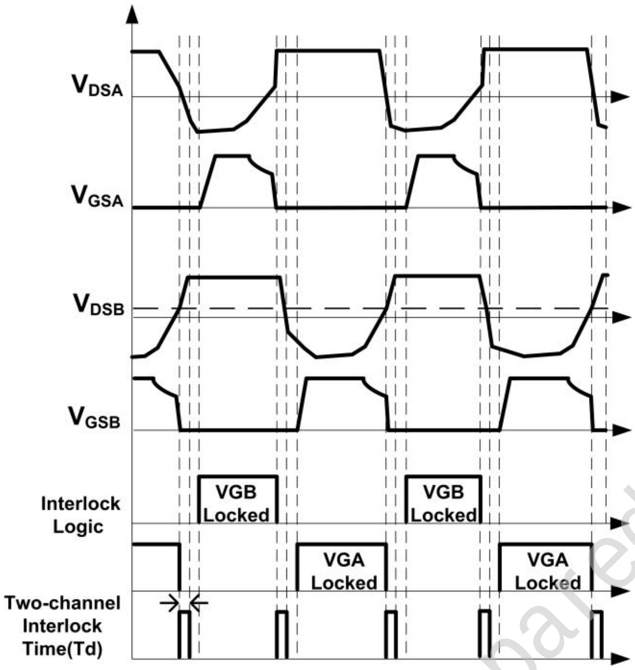


Figure16. Internal Interlock Logic Control Diagram

9. Application and Implementation

9.1 Typical Applications

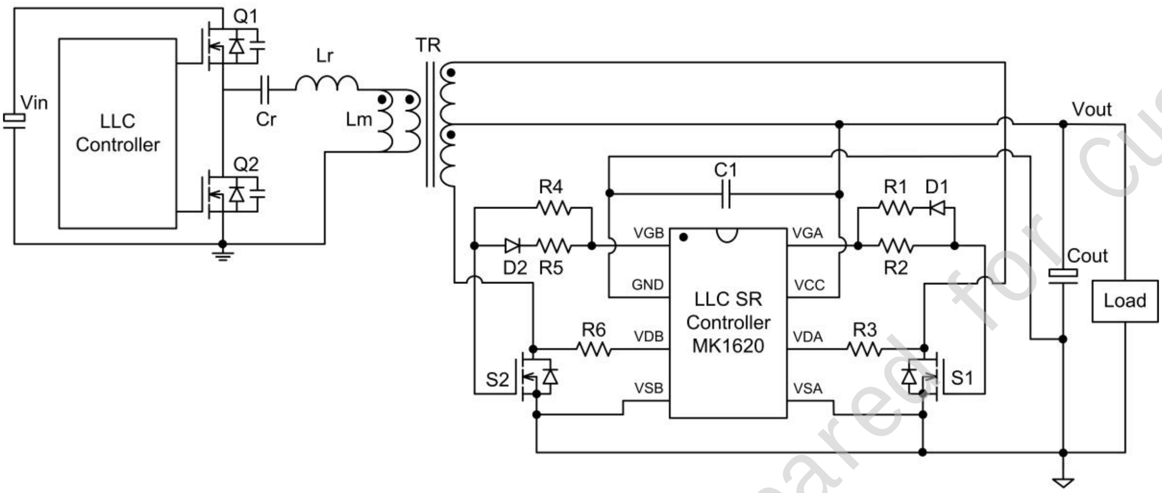


Figure 17. MK1620 Reference Design Circuit

9.2 Design Procedure

9.2.1 Supply Voltage

The supply voltage applied to the controller VCC pin should never exceed the absolute maximum ratings. Higher supply voltages require consideration of chip power dissipation and junction temperature (See Section 9.2.4). In some scenarios where the output bus voltage is high (for example, applications with outputs greater than 36V), a high voltage LDO must be used so that the VCC pin does not exceed the absolute maximum ratings and reduces the power dissipation of the internal LDO.

MK1620 reference design circuit is shown in Figure 17. Connect a low-ESR ceramic decoupling capacitor (C1) between 100 nF and 1 μF from VCC to GND for stability. The choice of decoupling capacitor voltage rating should also depend on the VCC voltage. Place the capacitor (C1) as close as possible to the MK1620 VCC and GND pins.

9.2.2 Peak Source and Sink Current

In order to reduce the switching losses and stress of the MOSFET, the switching speed of the MOSFET during turn-on and turn-off should be considered. The chip should be able to provide the required peak current for achieving the targeted switching speeds with the chosen power MOSFET. The maximum source and sink currents of the MK1620 have been provided.

For system applications, adding resistors R2 and R4 (such as 1Ω or 2Ω) between the gate of MOSFET and the VGA/VGB controls the switching speed of the MOSFET. Add diodes D1 and D2 as well as resistors R1 and R5. Keep the values of the resistors at 0Ω to achieve the fastest turn-off time.

9.2.3 Adjusting Voltage Setup

During regulation mode, MK1620 adjusts the VDS of SR MOSFET to be around $V_{DS\text{-}reg}$ until the current through the SR MOSFET drops to zero.

In different application systems, $V_{DS\text{-}reg}$ is one of the important parameters, which determines the output high level of the gate driver. When the current of the MOSFET rises to a higher value, the VDS voltage is less than the $V_{DS\text{-}reg}$ voltage. The gate driver charges the gate of the MOSFET until the MOSFET is fully turned on. Therefore, the value of $V_{DS\text{-}reg}$ is related to system efficiency.

Since the VDS voltage and $V_{DS\text{-}reg}$ determines the high level of VGA/VGB voltage, which further impacts the system efficiency, the external resistor in series with VDA/VDB used for filtering switching noise and limiting current when VDA/VDB is negative, should limit its value for no more than 100 ohms. The optimal control scheme and VDA/VDB negative voltage handling capability makes MK1620 working robustly and reliably even with no external filtering resistor at VDA/VDB pins.

If really needed, the value of $V_{DS\text{-}reg}$ may be slightly fine-tuned by adding resistors R3 and R6 (R_{set}) between the drain of the MOSFET and VDA/VDB. It is approximately calculated based on the below formula. The default value of R3 and R6 is zero ohm.

$$V_{DS\_regnew} \approx V_{DS\_reg} - (40uA \times R_{\mathrm{set}})$$

9.2.4 Power Dissipation

The chip power consumption and junction temperature must be considered. The chip will be damaged, if these two parameters are too large. The total power consumption (P_{DIS}) is estimated by the following formula:

$$P_{DIS} = P_{DRV} + P_P$$

The gate power (P_{DRV}) needs to be calculated first. It is calculated based on the formula:

$$P_{DRV} = 2 \times (Q_g - Q_{gd}) \times f_{smax} \times V_{CC}$$

Where (Q_g-Q_{gd}) is the total gate charge for SR MOSFET, f_{smax} is the maximum switching frequency, and V_{CC} is the supply voltage. The power consumption P_p (without gate charge) must also be considered.

$$P_P = I_{CC} \times V_{CC}$$

I_{CC} is the normal operating supply current without gate charging. The operating junction temperature (T_{JOP}) at a given ambient temperature (T_A) can be estimated according to the formula:

$$T_{JOP} = \theta_{JA} \times P_{DIS} + T_A$$

θ_{JA} is the junction-to-ambient thermal resistance.

9.2.5 MOSFET Selection

The SR MOSFET voltage stress, without considering the ringing voltages, must be twice of the output voltage. However, due to the switching noises at MOSFET turn off, there is always extra voltage stress. To ensure enough design margin, the selection of VDS voltage rating for MOSFEET is important. It is recommended to ensure a margin of at least 3 times the output voltage.

Due to the adjusting voltage threshold and driver ability of the synchronous rectifier controller, the selection of the power MOSFETs is a trade-off between RDS(ON) and Qg. Choosing the appropriate Qg value is also very important. A larger Qg will reduce the opening/closing speed and result in greater switching loss. Therefore, it is necessary to consider the opening/closing speed and switching loss.

MOSFETs with smaller RDS (ON) will touch the adjusting voltage threshold in advance, so that the power MOSFET cannot be fully turned on, so the advantage of the lower RDS (ON) MOSFET is not obvious. It is recommended to calculate the appropriate Rdson using the following formula:

$$Rdson = \frac{Vdsreg * \Pi}{2\sqrt{2} * Ioutmax}$$

For example, the typical value Vdsreg of MK1620 is 25mV. In applications where the maximum output current Ioutmax is 5A, Rdson can be calculated:

$$Rdson = \frac{25mV * \Pi}{2\sqrt{2} * 5A} \approx 5.55m\Omega$$

the RDS(ON) of the MOSFET is recommended to be no lower than 5.6mΩ.

10. Power Supply Recommendations

11. Layout

11.1 Layout Guidelines

To achieve high performance of the MK1620, the following layout tips must be followed.

1. Use separate clean traces for VCC and GND pins.
2. At least one low-ESR ceramic bypass capacitor(100nF) must be used. Place the capacitor as close as possible to the MK1620 VCC and GND pins.
3. The GND pin on the ground plane needs to route with a short and wide trace, or use a GND plane underneath the IC connected to the GND pin as well. It results in better heat dissipation.
4. Use separate traces for each source sense pin (VSA/VSB), and keep the ground and source sense traces separated.
5. Keep the two-channel differential sampling inputs (VDA/VSA, VDB/VSB) to each of the corresponding MOSFET drain/source pins as short as possible.
6. Keep the loop area of the two-channel differential sampling inputs (VDA/VSA, VDB/VSB) to each corresponding MOSFET drain/source pins as small as possible.
7. Avoid placing the VDA, VSA, VDB, and VSB traces close to any other high dV/dT traces that would induce significant noise into the high impedance leads.
8. The trace from the VGA/VGB pin to the gate of the SR MOSFET needs to be as short as possible.

11.2 Layout Example

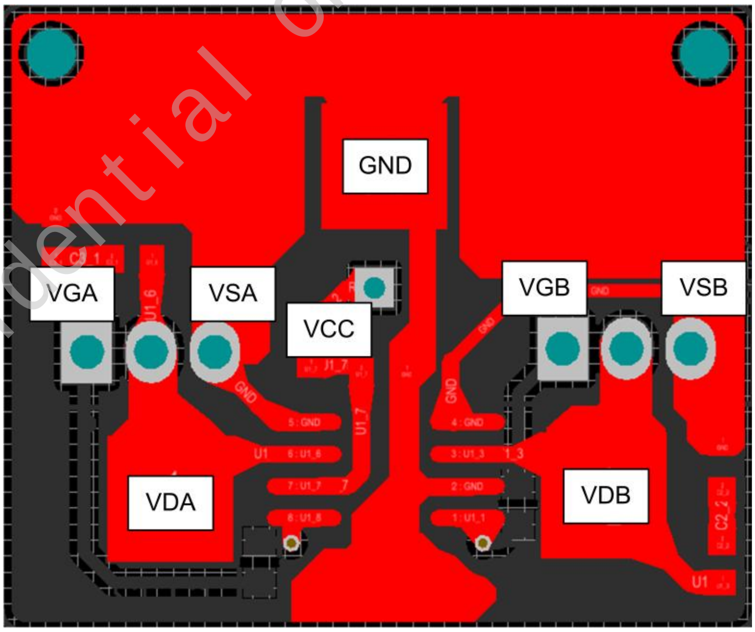


Figure 18. MK1620 Demo Board Layout (Top Layer)

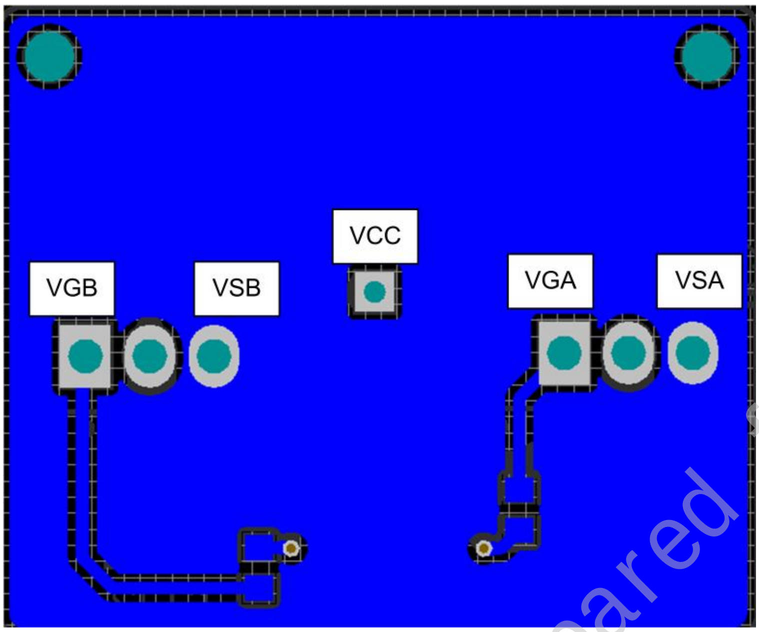


Figure 19. MK1620 Demo Board Layout (Bottom Layer)

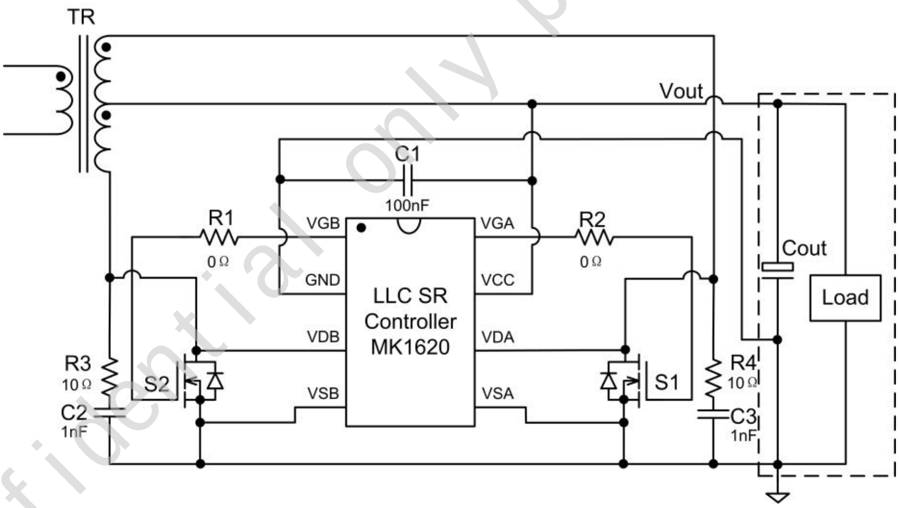


Figure 20. MK1620 Demo Board Schematic

12. Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13. Mechanical, Packaging

13.1 Package Size

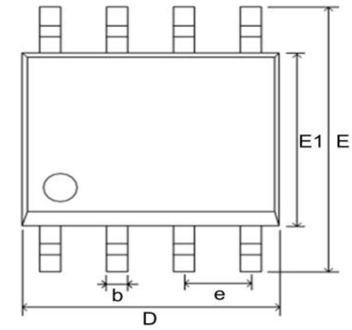


Figure 21. SOP-8 Top View

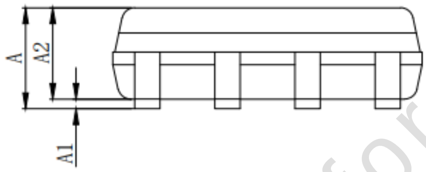


Figure 22. SOP-8 Side View

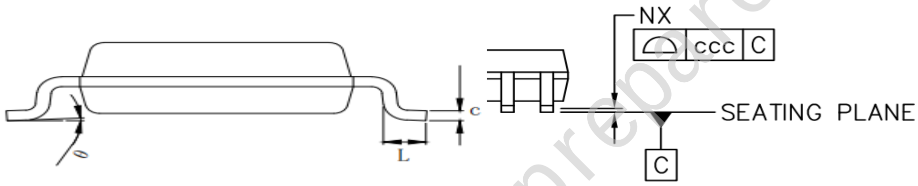


Figure 23. SOP-8 Side View and Coplanarity

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.30	1.55	1.75
A1	0.05	-	0.25
A2	1.25	1.40	1.65
b	0.33	-	0.51
c	0.20	-	0.25
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27(BSC)		
L	0.4	-	1.27
θ	0°	-	8°
Coplanarity (ccc) ≤ 0.10mm			

Notes:

(1) This drawing is subject to change without notice

13.2 Recommended Land Pattern

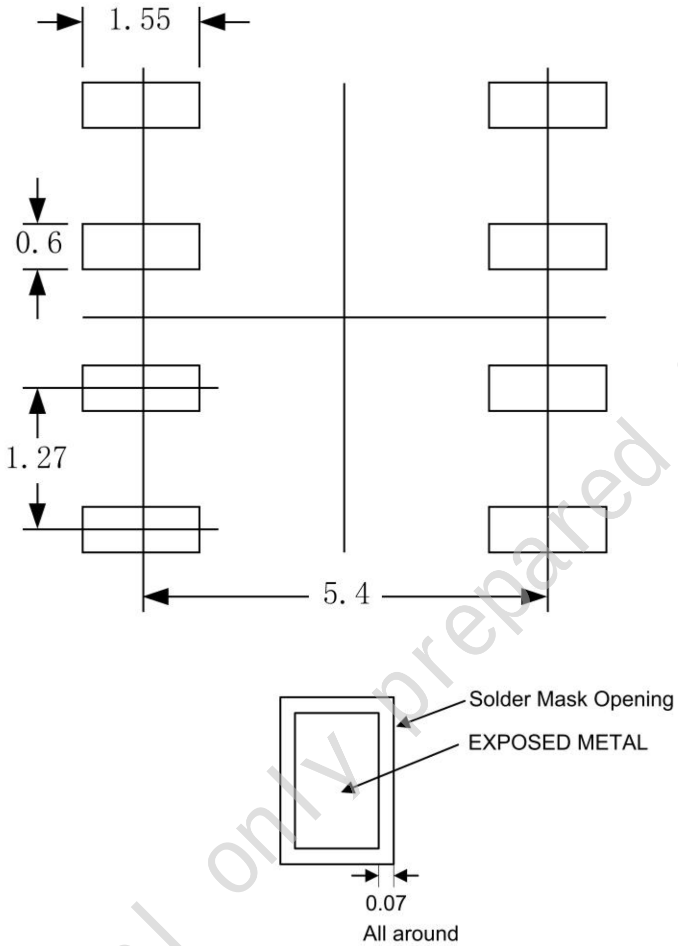


Figure 24. Recommended Land Pattern

Notes: (continued)

(1) All linear dimensions are in millimeters.

(2) It is recommended that vias under paste be filled, plugged or tented.

14. Reel and Tape Information

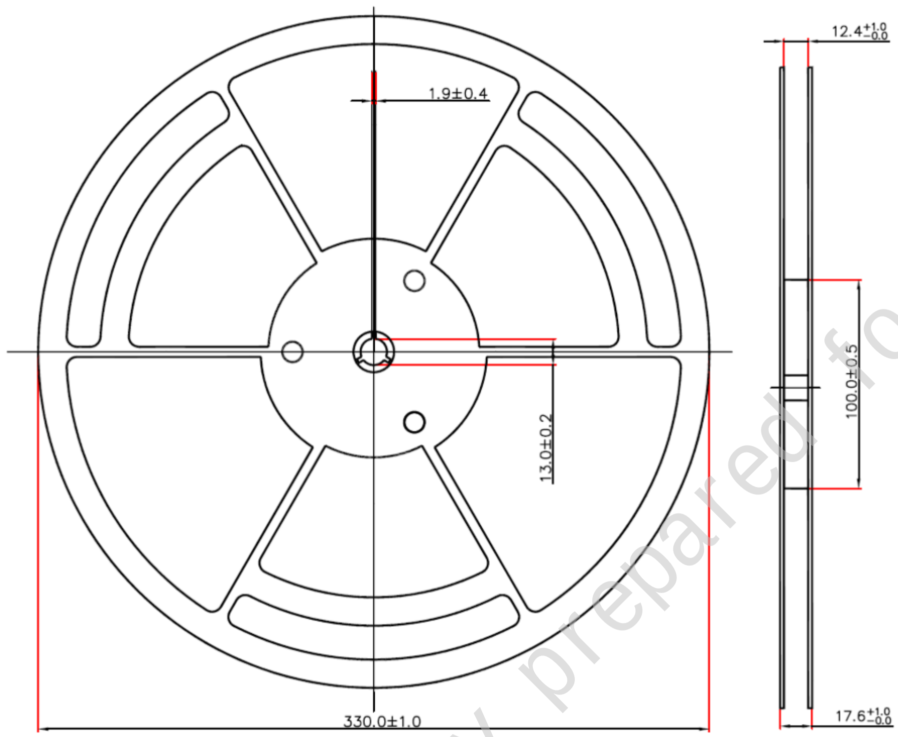
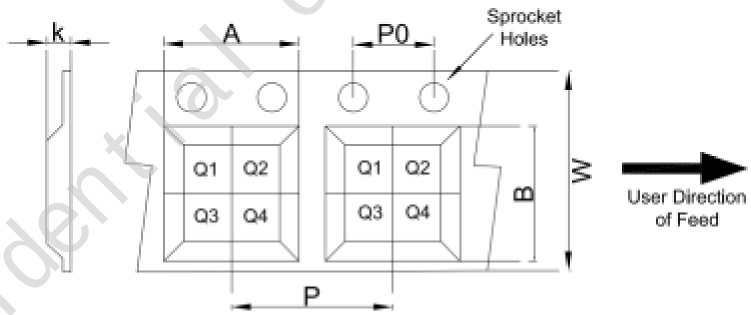


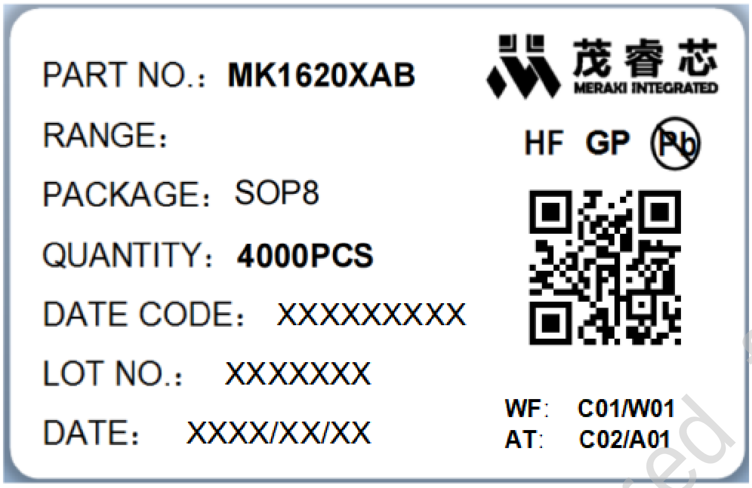
Figure 25. Reel Dimensions



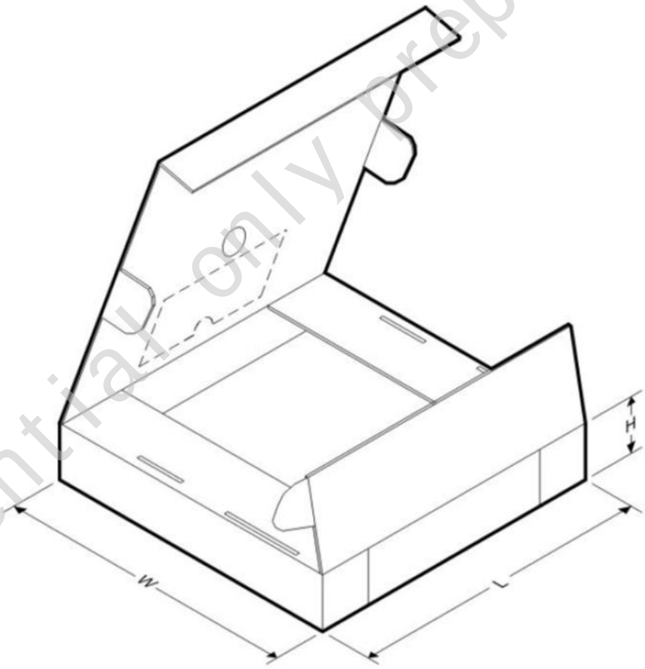
Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
MK1620XAB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	12.0±0.1	Q1

Figure 26. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

15. Tape and Reel Box Dimensions



(Please refer to MRX-DM-QA-05 for detailed rules)



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MK1620XAB	SOP-8	8	8000	360	360	65

Figure 27. Tape and Box Dimensions