MK2554A Continuous Conduction Mode PFC Controller

1. Description

The MK2554A family are continuous conduction mode (CCM) power factor correction (PFC) controllers for high performance AC/DC power systems. With multimode control strategy, the MK2554A can achieve ultralow THD and near unity power factor under different operation conditions. The switching frequency is fixed internally. Frequency dithering for better EMI performance is provided.

The MK2554A operates over a wide supply voltage range from 11V to 28V, which is suitable for various application scenarios. MK2554A integrates open/short protection functions for feedback and sense pin to reduce system damages risk. The MK2554A also features other system-level protections including peak current limit, input brown-out detection, output over-voltage and under-voltage detection. An accurate reference voltage for providing precise and reliable protection thresholds. The internal clamp circuitry limits the gate drive voltage less than 15.5 V.

2. Applications

- Boost PFC Power Converters
- Industrial Power Supplies
- Server and Desktop Power Supplies
- High Power LED Power Supplies

3. Features

- Wide VCC Voltage Range from 11V - 28V
- Ultra-Low Startup Current < 55uA
- Accurate Fully Integrated 65kHz / 130kHz / 200kHz Oscillator
- Dynamic Load Enhancer
- Frequency Dithering
- Soft-Start for Smoothly Startup Operation
- ±1% Voltage Reference
- Multimode Operation for Optimized Operation over the Line/Load Range
- Feedback and Sense Pin Open/Short Protection
- Available in SOP-8 Package

4. Typical Application

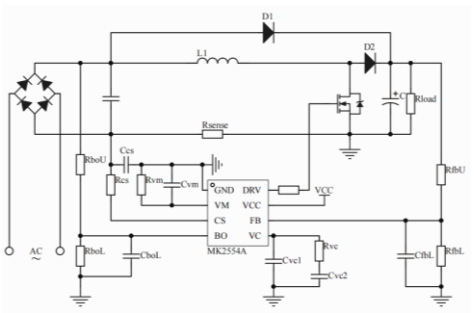

Figure 1. Typical Application Diagram

5. Order Information

Order Part Number	Descriptions
MK2554AX65AB	SOP-8, tape, 4000 pcs/reel
MK2554AX130AB	SOP-8, tape, 4000 pcs/reel
MK2554AX200AB	SOP-8, tape, 4000 pcs/reel

6. Pin Configuration and Functions

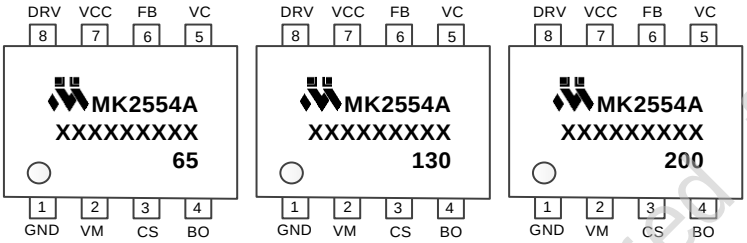

Figure 2. Pin Connection (top view)

Table 1. Pin Functions

Pin		Descriptions
NO.	Name	
1	GND	Device ground reference.
2	VM	This pin provides a voltage VM for the PFC duty cycle modulation, with open/short protection. Connect a resistor R_{VM} to GND, which is proportional to the input impedance of the PFC circuits to adjust the maximum delivered power by the PFC stage. The device operates in average current mode if an external capacitor C_{VM} is further connected between this pin and GND. Otherwise, it operates in peak current mode.
3	CS	This pin sources a current I_{CS} which is proportional to the inductor current. The sensed current I_{CS} is for duty cycle modulations, also for protections: inrush current detection, overcurrent protection (OCP) and zero current crossing detection (ZCD).
4	BO	This pin is connected to the rectified main input voltage via a resistor divider with a capacitor connected between BO pin and ground.BO pin detects a voltage signal proportional to the average input voltage. It is used for input brown out protection and overpower limitation (OPL).
5	VC	This pin is the output of the transconductance error amplifier. V_C pin is connected to external type−2 compensation components to limit the V_C bandwidth typically below 20Hz to achieve near unity power factor. This pin also has open/short protection.
6	FB	Negative input of the transconductance error amplifier. The information on the output voltage of the PFC converter is fed into the pin through a resistor divider.
7	VCC	This pin is the positive supply of the IC. The device starts to operate when V_{CC} exceeds $V_{CC\text{-}ON}$ and turns off when VCC goes below $V_{CC\text{-}OFF}$. After start−up, the operating range is 11V to 28V.
8	DRV	Integrated push-pull gate driver for one or more external power MOSFETs, with 1.5A sink and 1.5A source capability. Output voltage is clamped at 15.5 V.

7. Specifications

7.1 Absolute Maximum Ratings (1)

Symbol	Parameter	Min	Max	Unit
VCC	supply voltage VCC	-0.3	30	V
DRV (2)	output gate driver	-0.3	20	
FB/VC/BO/VM (2)	voltage on pin FB, VC, BO, VM	-0.3	8	
CS	voltage on pin CS	-3	8	
T_J	operating junction temperature,	-40	150	°C
T_{stg}	storage temperature	-55	150	
T_{sld}	soldering temperature (10 second)		260	

Notes:

(1) Stresses beyond the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in "RECOMMENED OPERATING CONDITIONS". Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Output pin not to be voltage driven.

7.2 ESD Ratings

		Value	Unit
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±2000	

Note:

（1） JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

（2） JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Moisture Sensitivity Level

Moisture Sensitivity Level	SOP-8	MSL1

7.4 Recommended Operating Conditions

		Min	Max	Unit
Recommended Operation Conditions	VCC supply voltage	11	28	V
	operating junction temperature (T_J)	-40	125	°C

7.5 Thermal Information

			Value	Unit
Package Thermal Resistance (1)	SOP-8	θ_{JA} (Junction to ambient)	128	°C/W
		θ_{JC} (Junction to case)	75	

Note:

（1） Measured on JESD51-7, 4-layer PCB.

7.6 Electrical Characteristics

-40°C ≤ T_A = T_J ≤ 125°C. V_{CC} = 15V_{DC}, 1µF from VCC to GND. All voltages are measured with respect to ground (pin 1). Currents are positive when flowing into the IC, unless otherwise specified.

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Supply Voltage Management						
V_{CC_ON}	V_{CC} UVLO Rising		9.50	10.70	11.50	V
V_{CC_OFF}	V_{CC} UVLO Falling		8.25	9.10	9.75	V
V_{CC_HYST}	V_{CC} UVLO Hysteresis			1.6		V
I_{ST}	Start-up Current	Before turn-on, V_{CC}=9V			55	µA
I_{OP}	Operating Current	V_{CC}=15V, no load, no switching, T_J=25℃		0.8	1.5	mA
I_{STDN}	Shutdown Mode Current	V_{CC}=15V, V_{FB}=0V		156	260	uA
Regulation Block						
V_{REF}	Voltage Reference	V_{CC}=15 V	2.43	2.50	2.57	V
V_{REF}	Voltage Reference	V_{CC}=15 V; T_J=25℃	2.475	2.500	2.525	V
I_{EA}	Error Amplifier Current Capability (1)	V_{CC}=15 V		±28		µA
G_{EA}	Error Amplifier Gain (1)	V_{CC}=15 V		230		µS
I_{FB}	Pin 6 Bias Current	V_{FB} = V_{REF}	-500		800	nA
V_{C_MAX}	Maximum Control Voltage	V_{FB} = 2 V		3.6		V
V_{C_MIN}	Minimum Control Voltage	V_{FB} = 3 V		0.6		V
ΔV_C	ΔV_C = V_{C_MAX} – V_{C_MIN}		2.8	3.0	3.2	V
V_{FB_ODE} /V_{REF}	V_{OUT} Low Detect Threshold/V_{REF}		92.0	94.7	98.0	%
V_{FB_ODE} $_{(HYS)}$ /V_{REF}	V_{OUT} Low Detect Hysteresis/V_{REF}			2		%
Current Sense Block						
I_S	Overcurrent Protection Threshold	T_J=25℃	190	200	210	µA
Power Limitation Block						
I_{OPL}	Overpower Limitation Threshold	I_{OPL} = I_{CS} *V_{BO}		200		µVA

$I_{CS\ (OPL1)}$	Overpower Current Threshold	V_{BO} = 0.9 V, V_M = 3 V	175	210	245	μA
$I_{CS\ (OPL2)}$	Overpower Current Threshold	V_{BO} = 2.7 V, V_M = 3 V	60	75	90	μA
PWM Block						
D_{CYCLE}	Duty Cycle Range (1)			0-97		%
T_{LEB}	Leading Edge Blanking Time (1)			300		ns
Oscillator Block						
F_{SW}	Switching Frequency	MK2554AX65AB, T_J=25℃	60	65	70	kHz
F_{SW}	Switching Frequency	MK2554AX130AB, T_J=25℃	120	130	140	kHz
F_{SW}	Switching Frequency	MK2554AX200AB, T_J=25℃	184	200	216	kHz
Brown-out Detection Block						
V_{BOH}	Brown-out Voltage Threshold (rising)		1.23	1.30	1.37	V
V_{BOL}	Brown-out Voltage Threshold (falling)		0.65	0.70	0.75	V
I_{BO}	Pin 4 Input Bias Current	V_{BO} = 1 V	-300		300	nA
Current Modulation Block						
I_{M1}	Multiplier Output Current	C_{VC} = 30 nF, V_{BO} = 0.9 V, I_{CS} = 25 μA, V_{FB} = 2 V		1.9		μA
I_{M2}	Multiplier Output Current	C_{VC} = 30 nF, V_{BO} = 0.9 V, I_{CS} = 75 μA, V_{FB} = 2 V		5.8		μA
I_{M3}	Multiplier Output Current	C_{VC} = 30 nF, V_{BO} = 1.5 V, I_{CS} = 75 μA, V_{FB} = 2 V	7.5	10.0	12.5	μA
I_{M4}	Multiplier Output Current	V_C = 0.8 V, V_{BO} = 0.9 V, I_{CS} = 25 μA, V_{FB} = 2 V		28		μA
I_{M5}	Multiplier Output Current	V_C = 0.8 V, V_{BO} = 0.9 V, I_{CS} = 75 μA, V_{FB} = 2 V		80		μA
Overvoltage Protection						
V_{OVP}/V_{REF}	Ratio (Overvoltage Threshold/ V_{REF})		102	105	108	%
$V_{OVP(HYS)}$ /V_{REF}	Ratio (Overvoltage Threshold Hysteresis / V_{REF})			3		%

Undervoltage Protection						
$V_{UVP(ON)}$ /V_{REF}	UVP Activate Threshold Ratio		5	8	11	%
$V_{UVP(OFF)}$ /V_{REF}	UVP Deactivate Threshold Ratio		10	12	14	%
$V_{UVP(H)}$ /V_{REF}	UVP Lockout Hysteresis			4		%
Thermal Shutdown						
T_{SD}	Thermal Shutdown Threshold (1)		150			°C
H_{SD}	Thermal Shutdown Hysteresis (1)			30		°C
Gate Driver						
T_{RR}	Gate Drive Voltage Rise Time from 1 V to 11V	C_{LOAD} = 2.2nF R_{GS} = 10kΩ V_{CC} = 12V		58		ns
T_{RF}	Gate Drive Voltage Fall Time from 11 V to 1 V	C_{LOAD} = 2.2nF R_{GS} = 10kΩ V_{CC} = 12V		30		ns
I_{VG_H}	Maximum Source Current (1)			1.5		A
I_{VG_L}	Maximum Sink Current (1)			1.5		A
R_{sink}	Pull-down Impedance	I_{LOAD}= 100mA		1		Ω
V_{VG_H}	Pin 8 Clamp Voltage	V_{CC} = 18V		15.5		V

Note:

(1) Values are guaranteed by design and verified by characterization on bench, not tested in production.

7.7 Typical Characteristics

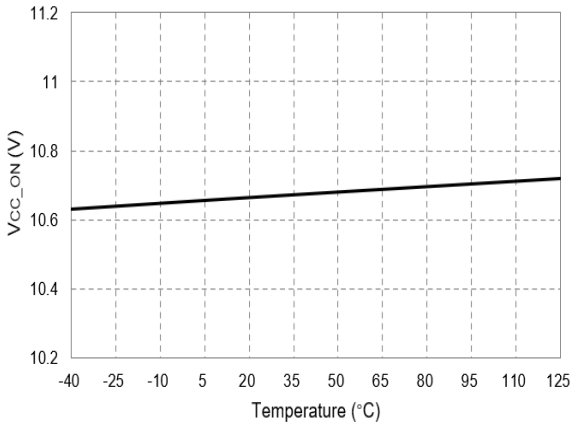

Figure 3. VCC UVLO Rising vs. Temperature

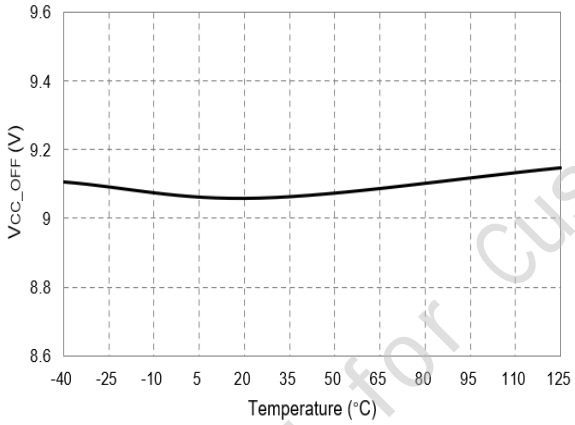

Figure 4. VCC UVLO Falling vs. Temperature

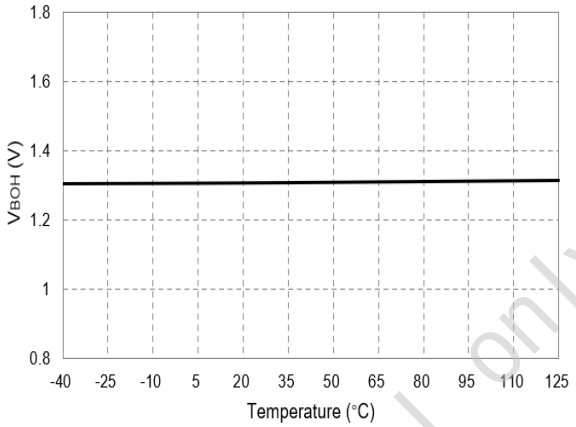

Figure 5. Brown-out Voltage (Rising) vs. Temperature

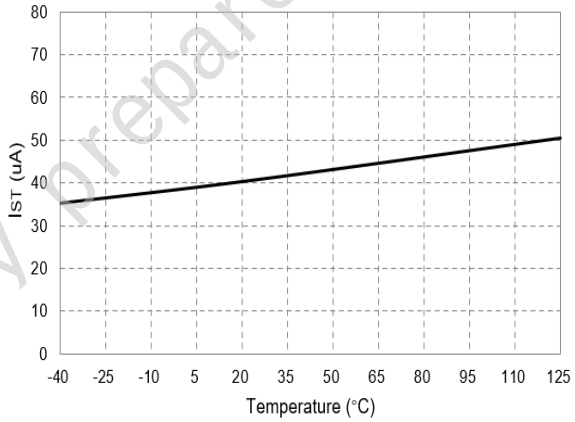

Figure 6. Start-Up Current (Before Turn-On) vs. Temperature

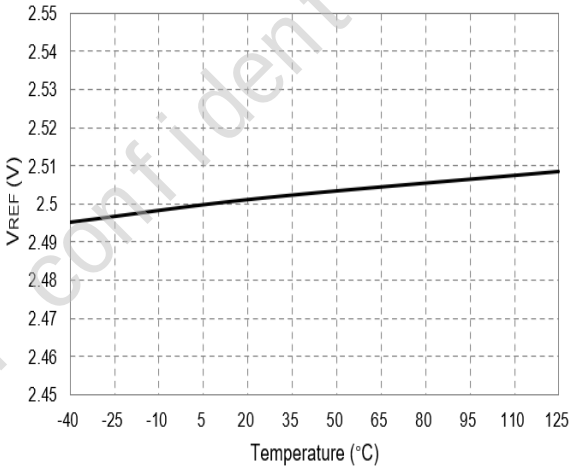

Figure 7. Reference Voltage vs. Temperature

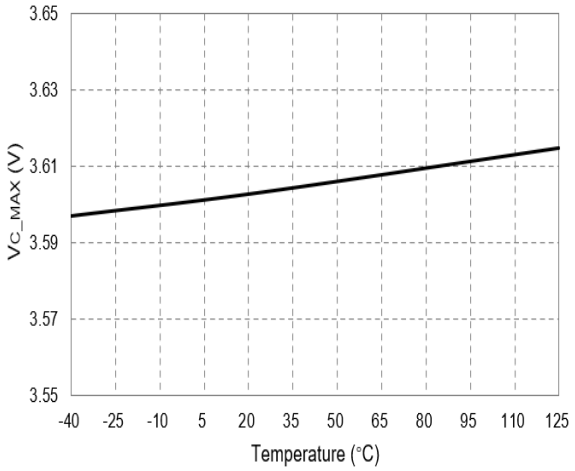

Figure 8. Maximum Control Voltage vs. Temperature

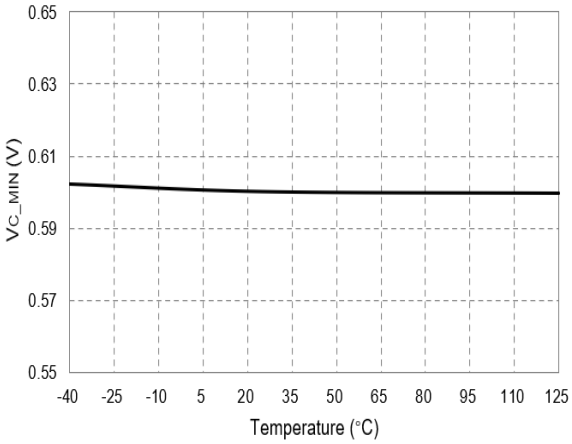

Figure 9. Minimum Control Voltage vs. Temperature

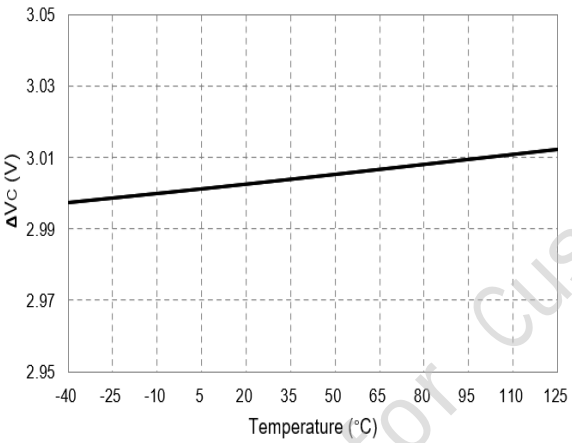

Figure 10. ΔVc vs. Temperature

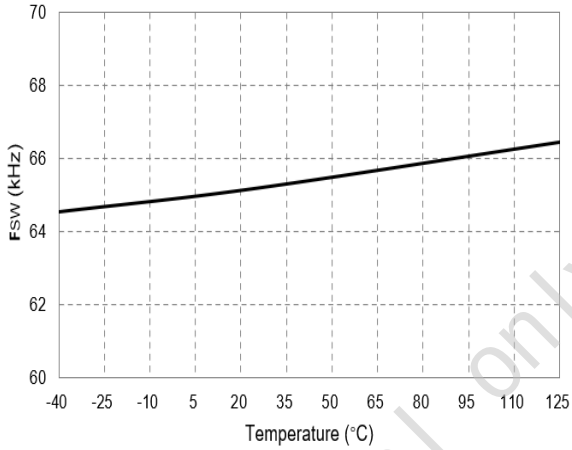

Figure 11. Switching Frequency (Based on 65 kHz) vs. Temperature

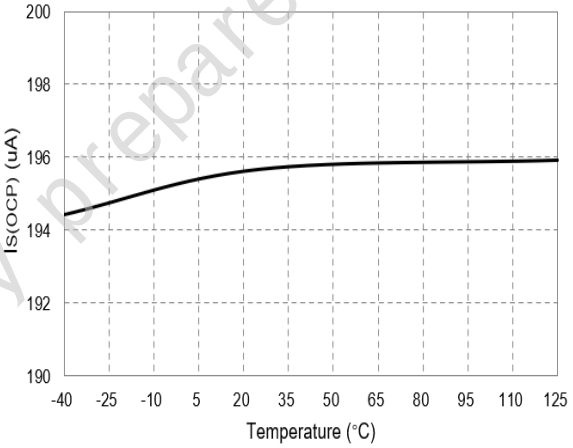

Figure 12. Overcurrent Protection Threshold vs. Temperature

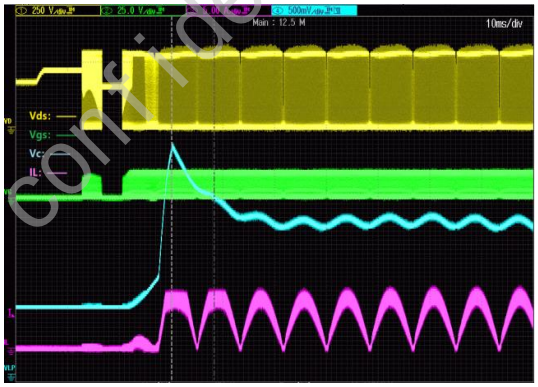

Figure 13. Dynamic Load Enhancer

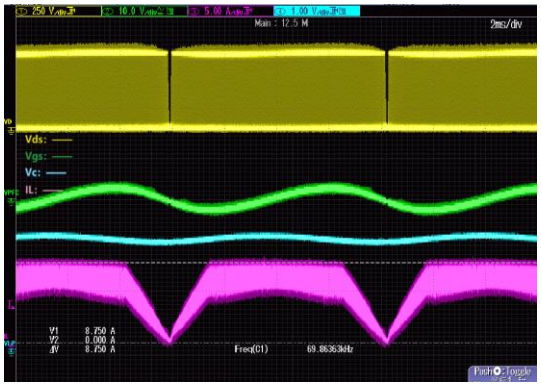

Figure 14. Overcurrent Protection

8. Detailed Description

8.1 Overview

The MK2554A family are continuous conduction mode PFC controllers designed to operate in fixed frequency. With multimode control strategy, the MK2554A can achieve ultralow THD and near unity power factor under different operation conditions. At the same time, the frequency dithering is provided for spreading the noise spectrum and reducing the possible radiated noise.
In continuous conduction mode, the lower peak current and di/dt value reduce power loss and improve system efficiency. The reliability of internal logic and protection is guaranteed by the accurate reference voltage. The MK2554A simplifies PFC surrounding circuit, so that the design time of production can be saved.
The MK2554A is pin compatible with other industrial controllers providing similar functions, while richer enhancement features have been implemented to reduce bill of materials (BOM) cost. The system performance is improved by increasing the operating voltage range and optimizing the startup strategy, which makes the controller easier to start in the high-power systems. The device also features an innovative dynamic output voltage protection enhancement circuit, which improves the performance of the system under dynamic load. The soft start function and optimized operating currents of the device result in low current stress and low power consumption. The intelligent protection functions and strategies of MK2554A can greatly improve system reliability, such as driver output voltage clamp, feedback pin open or short protection, brown in and brown out protection, output overvoltage protection (OVP), output undervoltage protection (UVP), overcurrent protection (OCP), and smart overpower limitation (OPL).

8.2 Functional Block Diagram

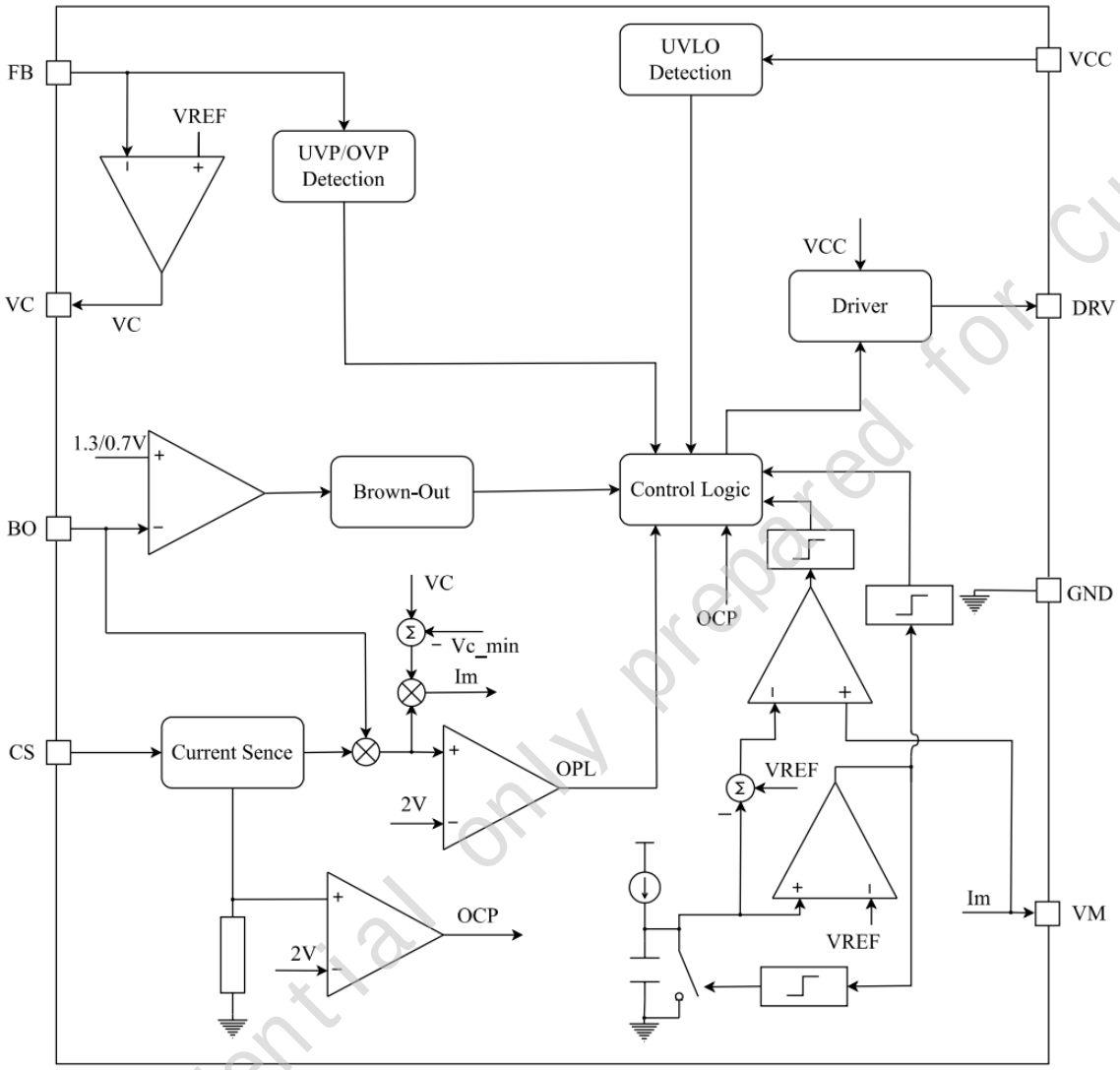

Figure 15. Block Diagram

8.3 Feature Description

8.3.1 VCC Power Supply and Undervoltage Lockout (UVLO)

The VCC operation voltage is between 11V to 28V, which makes MK2554A suitable for a variety of application scenarios. For the best performance, use a typical 0.1uF decoupling capacitor as close as possible between the VCC and GND pins of MK2554A. A VCC bypass capacitor (1uF to 10uF) in parallel to the decoupling capacitor is also recommended to reduce noise ripple during switching.

MK2554A has an internal undervoltage lockout (UVLO) protection feature in the VCC supply circuit blocks. When the voltage on the VCC pin exceeds $V_{CC\text{-}ON}$, the controller exits the UVLO state and activates the circuitry. When VCC voltage drops to below $V_{CC\text{-}OFF}$, the controller re-enters the UVLO state.

When the VCC supply voltage of MK2554A is higher than 18V, in order to avoid the damage of power MOSFETs due to high driver voltage, the voltage of MK2554A DRV (Pin 8) is clamped to V_{VG_H}.

8.3.2 Brown−In and Brown−Out Protection

As the power line voltage decreases, the input current must increase to maintain a constant output voltage for any specific load. Brownout protection helps prevent excess system thermal stress (due to the higher RMS input current) from exceeding a safe operating level.

The MK2554A detects the input voltage after rectification by V_{BO} (Pin 4) for input undervoltage protection. The rms value of input voltage is converted into the average value because of the existence of the capacitance C_{BO}. The C_{BO} typically uses a typical 0.47uF filter capacitor. Figure 16 and Figure 17 show the V_{BO} waveforms before and after filtering, respectively. The V_{AC} is the rms value of input voltage. V_{BO} voltage can be described in Equation 1.

$$V_{BO} = \frac{2\sqrt{2}}{\pi} V_{AC} \times \frac{R_{BOL}}{R_{BOL} + R_{BOU}} \quad (1)$$

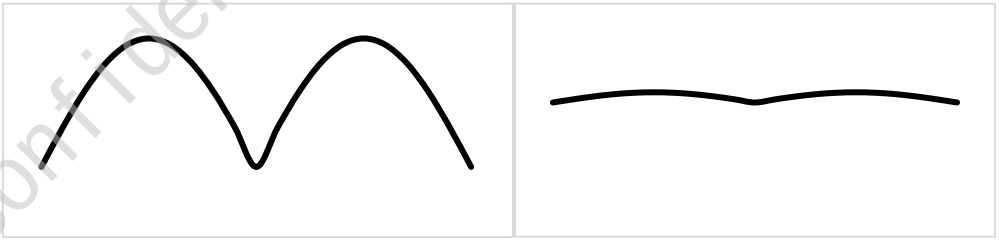

Figure 16. Before Average **Figure 17. After Average**

When V_{BO} exceeds V_{BOH} (1.3V, the typical value), and the VCC pin exceeds $V_{CC\text{-}ON}$, the power stage soft starts as VC pin rises with controlled voltage. If the BO pin voltage V_{BO} falls below V_{BOL} (0.7 V, the typical value), a brown-out condition is detected, and gate driver output will not immediately turn off until the end of deglitch time. Thanks to a larger hysteresis between the brown out and brown in, the MK2554A can operate stably under critical input voltage conditions.

8.3.3 Overcurrent Protection (OCP) and Overpower Limitation (OPL)

Under certain conditions such as inrush, brown-out recovery, and output over-load, the PFC power stage experiences large currents. It is critical that the power devices are protected from switching during these conditions.

In order to achieve real-time sampling of inductance current, the resistors R_{sense} and R_{CS} are needed. R_{sense} is a low value resistor in the return path of input rectifier, the other side of the resistor is tied to the system ground. The voltage is sensed on the rectifier side of the sense resistor and is always negative. The MK2554A controller maintains the voltage at CS pin to be zero voltage by sourcing an I_{CS} current. The sensing current I_{CS} represents the inductor current I_L, so that, the current value I_{CS} can be calculated in Equation 2. The current I_{CS} is used in the PFC duty modulation to generate the multiplier voltage VM, overcurrent protection (OCP) and overpower limitation (OPL).

$$I_{cs} = \frac{R_{sense}}{R_{cs}} I_L \quad (2)$$

Once I_{CS} exceeds overcurrent protection threshold (I_S) or I_{CS}* V_{BO} exceeds overpower limitation threshold, the MOSFET is turned off, the MK2554A triggers overcurrent protection or overpower limitation, the MOSFET stays in OFF-state until the PWM latch-off is reset by the clock signal.

8.3.4 Overvoltage Protection (OVP) and Undervoltage Protection (UVP)

The accuracy of the MK2554A internal reference voltage (V_{REF}) used for the output regulation, which is less than ±3% over the temperature range. In particular, the accuracy can be less than ±1% at room temperature. The output voltage V_{out} of the PFC circuits is sensed at FB pin via the resistor divider (R_{FBL} and R_{FBU}). The output voltage (V_{out}) can be obtained in Equation 3.

$$V_{out} = \frac{R_{FBL} + R_{FBU}}{R_{FBL}} V_{REF} \quad (3)$$

In a similar way, the FB pin voltage (V_{FB}) can be calculated in Equation 4.

$$V_{FB} = \frac{R_{FBL}}{R_{FBL} + R_{FBU}} V_{out} \quad (4)$$

The MK2554A monitors the voltage on the FB pin in real time. When the output voltage is higher than the overvoltage protection threshold, the OVP is triggered and the driver signal will be stopped. The MK2554A will not release protection until V_{FB} drops below the OVP voltage threshold with a hysteresis.

When FB pin voltage is below the UVP threshold, the MK2554A is shut down and reduces its power consumption to a lower value. To restart the IC, the FB pin voltage must exceed UVP threshold with a hysteresis. Using this function, the user can flexibly control the operating state of the MK2554A.

The MK2554A also provides a certain degree of additional security. When the lower resistor of the output resistor divider is shorted to ground or the upper resistor is missing, the MK2554A enters the off-protection state. The MK2554A VC and VM pin also has similar functions.

8.3.5 Dynamic Load Enhancer (DLE)

The output voltage of PFC stages may exhibit excessive over or under shoots because of load steps or input voltage changes. During large changes in load or input voltage, dynamic load enhancer acts to speed up the slow response of the low-bandwidth voltage loop. As shown in Figure 18, if the output voltage is out of regulation, the MK2554A dynamic load enhancer maintains fast and stable regulation of the output voltage.

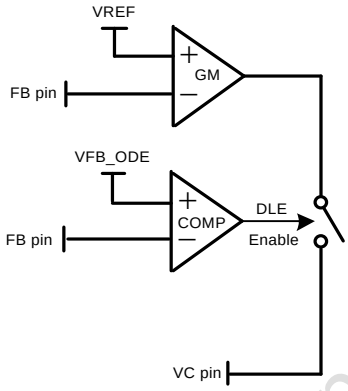

Figure 18. Dynamic Load Enhancer

When the output voltage is below V_{FB_ODE}, the comparator COMP is set high, dynamic load enhancer is activated with an extra current source (current value associated with the V_{FB}-V_{REF}) raising VC pin voltage rapidly. Therefore, the PFC output is prevented from dropping too low, and the transient response is improved.

8.3.6 Multiplier Voltage

The multiplier serves two main purposes, with the first one is for power protection. Multipliers generate I_{CS}* V_{BO}, when I_{CS}* V_{BO} is greater than I_{OPL}, the MOSFET is turned off. The second purpose is to generate I_M for loop control. The multiplier outputs a current I_M, flows out of the VM pin and generates voltage on the VM pin after passing through a resistor R_{VM}. With an external capacitor C_{VM} connected to the multiplier voltage VM pin to bypass the high−frequency component of VM. MK2554A operates in average current control mode. Otherwise, it operates in peak current control mode. The current I_M can be calculated in Equation 5, k is the current gain.

$$I_M = k\frac{I_{CS}*V_{BO}}{V_C - V_{C\_\min}} \quad (5)$$

Where, the V_{BO} is the input voltage signal on the BO pin, which is proportional to the rms input voltage. I_{CS} is the sense current proportional to the inductor current I_L as described in 9.3.3. The V_C is the control voltage signal, the output voltage of operational trans−conductance amplifier (OTA). The V_{C_min} can be regarded as a constant, equal to V_{C_MIN}.

The PFC modulation and timing diagram is shown in Figure 19. The MOSFET on time is generated by the reference voltage V_{REF}, multiplier voltage VM and ramp voltage V_{RAMP}.

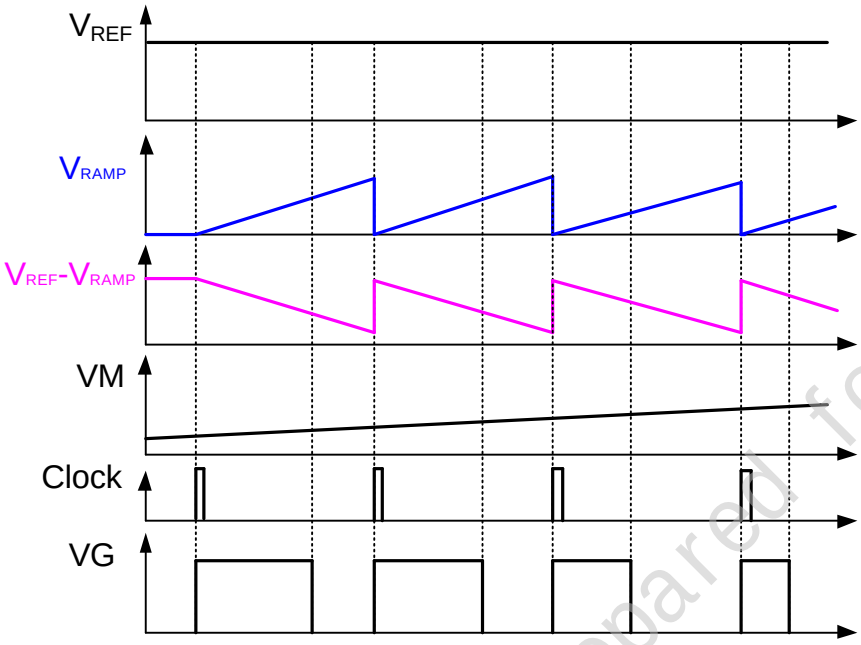

Figure 19. MK2554A Modulation and Timing Diagram

9. Application and Implementation

9.1 Typical Applications

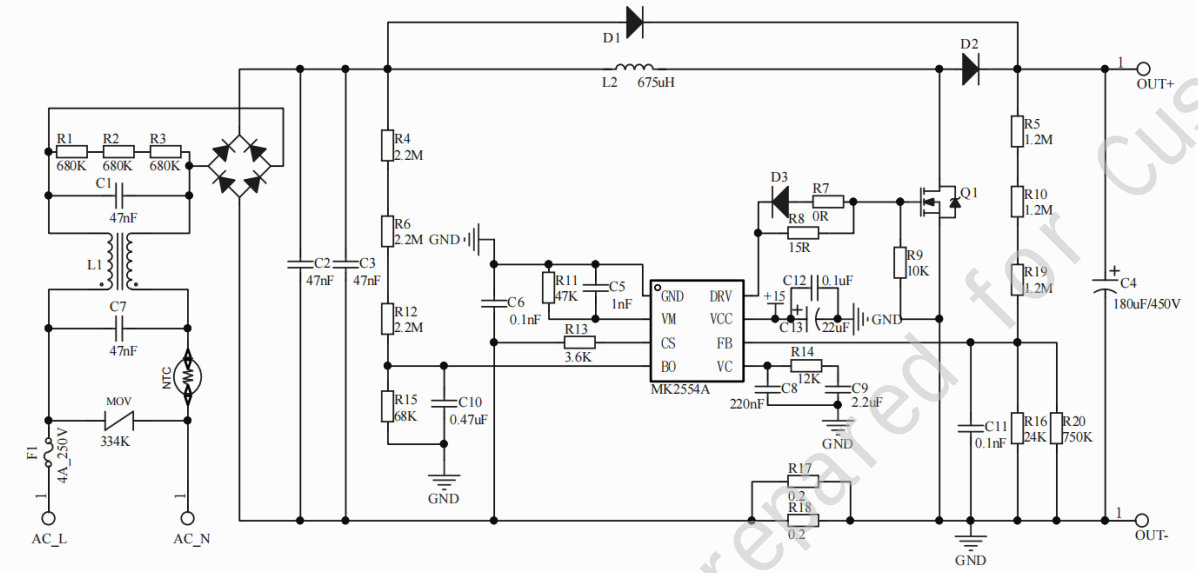

Figure 20. Reference Design Circuit

10. Power Supply Recommendations

11. Layout

11.1 Layout Guidelines

To achieve high performance of the MK2554A, the following layout tips must be followed:

1. Use separate clean traces for VCC and GND pins.
2. At least one low-ESR ceramic bypass capacitor(100nF) must be used. Place the capacitor as close as possible to the MK2554A VCC and GND pins.
3. The GND pin on the ground plane needs to route with a short and wide trace, or use a GND plane underneath the IC connected to the GND pin as well.
4. The effectiveness of the filter capacitors on the signal pins (BO, VC, VM) depends upon the integrity of the ground return.
5. The pinout of the MK2554A is ideally suited for separating the high di/dt induced noise on the power ground from the low current quiet signal ground required for adequate noise immunity.
6. A star point ground connection at the GND pin of the device can be achieved with a simple cut out in the ground plane.
7. The capacitors on CS and FB must all be returned directly to the quiet portion of the ground plane.
8. The trace from the DRV pin to the gate of the MOSFET needs to be as short as possible.

11.2 Layout Example

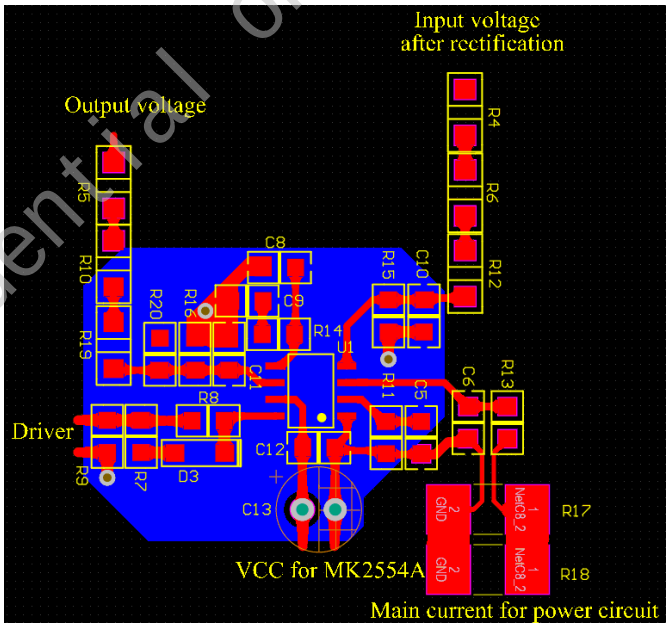

Figure 21. MK2554A Layout Example

12. Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13. Mechanical, Packaging

13.1 Package Size

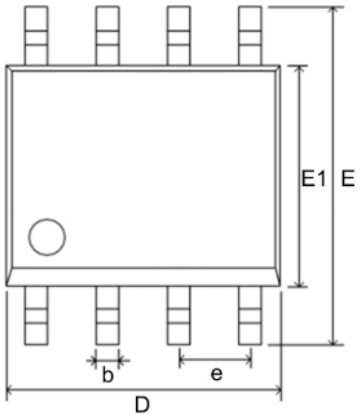

Figure 22. SOP-8 Top View

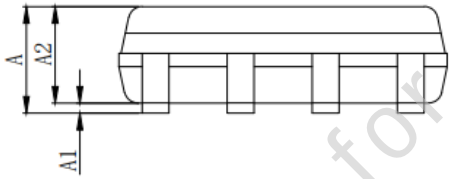

Figure 23. SOP-8 Side View

Figure 24. SOP-8 Side View

SYMBOL	Dimensions In Millimeters	
	MIN	MAX
A	1.30	1.75
A1	0.05	0.25
A2	1.25	1.65
b	0.33	0.51
c	0.20	0.25
D	4.7	5.1
E	5.8	6.2
E1	3.8	4.0
e	1.270(BSC)	
L	0.40	1.27
θ	0°	8°

Note:

（1）This drawing is subject to change without notice

13.2 Recommended Land Pattern

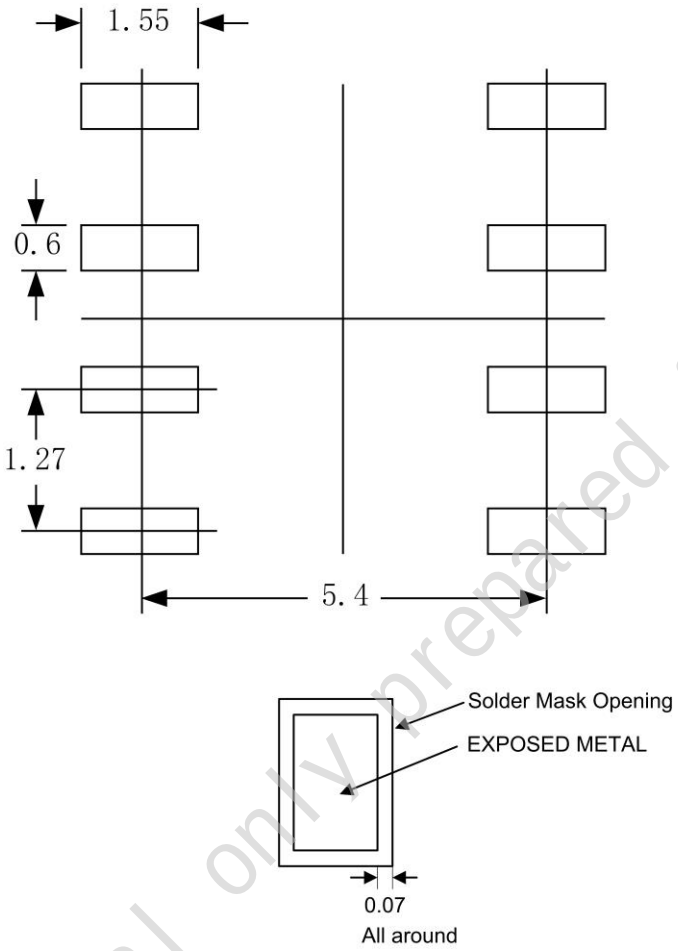

Figure 25. Recommended Land Pattern

Notes: (continued)

（1） All linear dimensions are in millimeters.

（2） It is recommended that vias under paste be filled, plugged or tented.

14. Reel and Tape Information

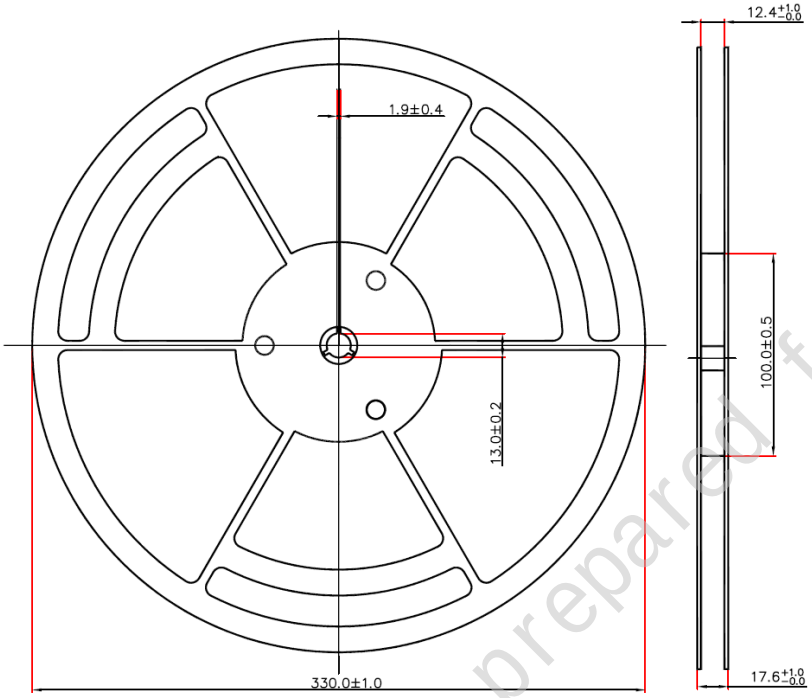

Figure 26. Reel Dimensions

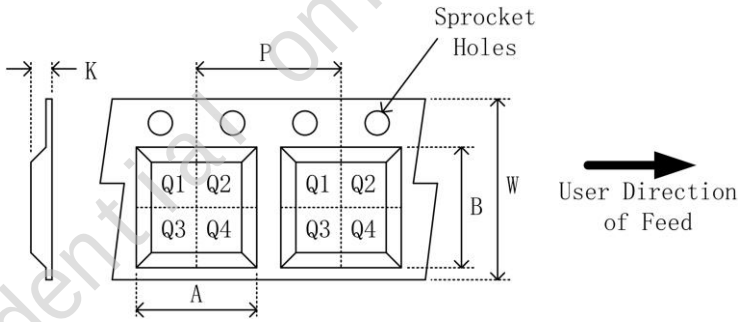

Figure 27. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	W (mm)	Pin1 Quadrant
MK2554AX65AB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8±0.1	12±0.1	Q1
MK2554AX130AB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8±0.1	12±0.1	Q1
MK2554AX200AB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8±0.1	12±0.1	Q1

15. Tape and Reel Box Dimensions

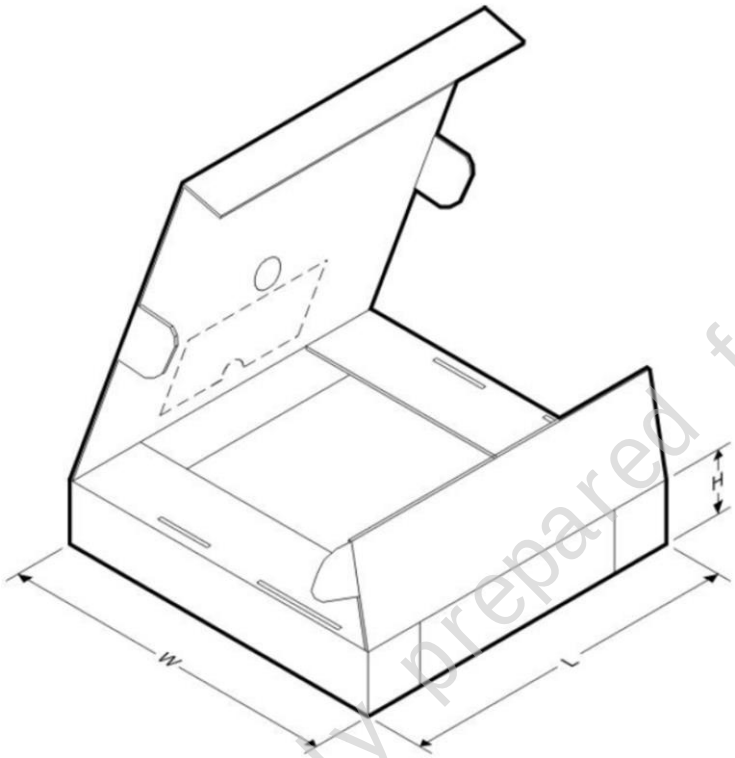

Figure 28. Box Dimensions

Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MK2554AX65AB	SOP-8	8	8000	360	360	65
MK2554AX130AB	SOP-8	8	8000	360	360	65
MK2554AX200AB	SOP-8	8	8000	360	360	65