MCAN1463B CAN FD Signal Improvement Transceiver with Sleep Mode

1 Descriptions

The MCAN1463B meets the ISO11898-2(2016) High Speed CAN (Controller Area Network) physical layer standard. All devices are designed for use in CAN FD (flexible data rate) networks up to 8Mbps (megabits per second).

The MCAN1463B supports CAN Signal Improvement Capability (SIC), as defined in CiA 601-4:2019. CAN SIC reduces signal ringing at the dominant-to-recessive edge and enables higher throughput in complex network topologies.

2 Features

- AEC-Q100 Grade 1
- Meets the ISO 11898-2:2016 physical layer standards
- Implements Signal Improvement Capability (SIC) as defined in CiA 601-4
- Support classic CAN and 8Mbps CAN FD
- I/O Voltage range supports 1.71 V to 5.5 V
- Ideal passive behavior when unpowered
- Local wake up via the WAKE pin
- Operating modes
  - Normal mode
  - Listen mode
  - Standby mode
  - Sleep mode
- Remote wake up via WUP (Wake Up Pattern)
- INH output for system power reduction
- Protection and diagnosis features
  - Bus Fault protection: ±58 V
  - V_{BAT} Absolute Max. Voltage: ±58 V
  - V_{BAT}, V_{CC}, V_{IO} Under-voltage protection
  - TXD-to-RXD short-circuit fault diagnosis
  - Thermal shutdown protection (TSD)
- Receiver common mode input voltage: ±30V
- Suitable for 12V and 24V systems
- Typical loop delay: 110 ns
- Available in SOP14 and DFN14 package

3 Application

- Automotive and Transportation
- Body electronics and lighting
- Advanced driver assistance systems (ADAS)
- Hybrid, electric & power train systems

4 Typical Application

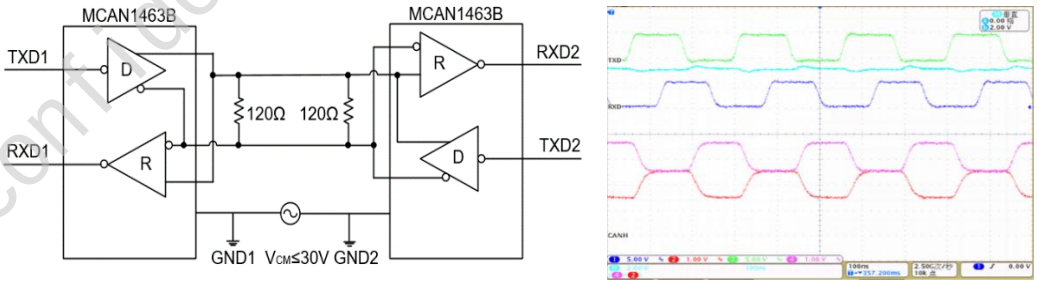


Figure 1. Typical Application Diagram and Performance

5 Order Information

Part Number	Package Type	Package Qty	Eco Plan	MSL	Description
MCAN1463BXAK-Q1	SOP14	4000pcs	RoHS & Green	MSL2	VCM=±30V
MCAN1463BXDH-Q1	DFN14	3000pcs	RoHS & Green	MSL2	VCM=±30V

6 Pin Configuration and Marking Information

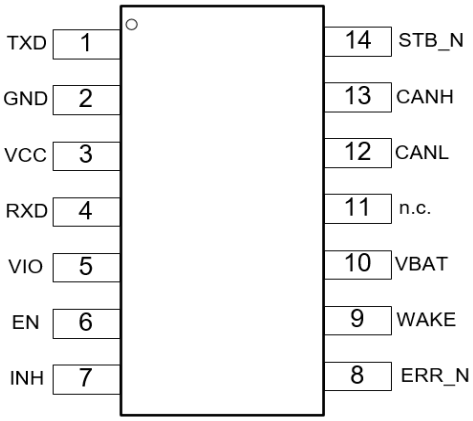


Figure 2. SOP Package,14 pin (top view)

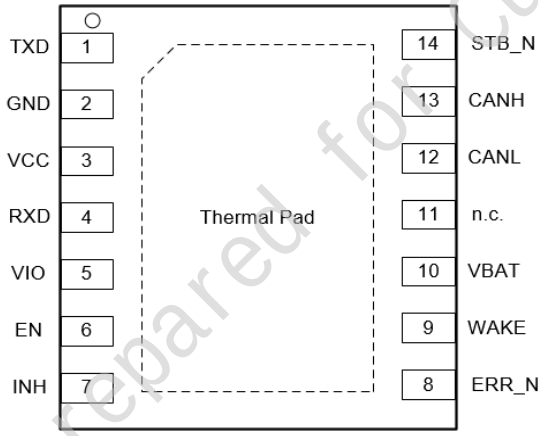
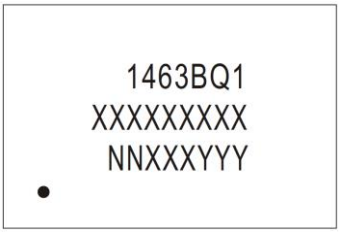


Figure 3. DFN Package,14 pin (top view)

SOP14



DFN14

Figure 4. Marking Information (XXXXXXXXX: Date Code)

Table 1. Pin Functions

Pin		I/O (1)	Description
Number	Name		
1	TXD	I	CAN transmit data input, integrated pull-up
2	GND	GND	Ground
3	VCC	P	5V transceiver supply
4	RXD	O	CAN receive data output
5	VIO	P	I/O supply voltage
6	EN	I	Enable input for mode control, integrated pull-down
7	INH	O	INH output for controlling system voltage regulators (High to enable and High-Z to disable the system voltage regulators)
8	ERR_N	O	Fault indication output (active low)
9	WAKE	I	Local wake-up input
10	VBAT	P	Battery supply input
11	n.c.	-	No connect (not internally connected)
12	CANL	I/O	Low-level CAN bus input/output line
13	CANH	I/O	High-level CAN bus input/output line
14	STB_N	I	Standby mode control input (active Low), integrated pull-down
Thermal Pad		-	Exposed PAD, Solder the EP to the GND pin and connect to a large copper plane to reduce thermal

Note:

(1) GND = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings (1)

		MIN	MAX	UNIT
V_{BAT}	Battery supply voltage	-0.3	58	V
V_{CC}	CAN transceiver supply voltage	–0.3	6	V
V_{IO}	I/O supply voltage	–0.3	6	V
V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)	–58	58	V
V_{DIFF}	Max differential voltage between CANH and CANL	–58	58	V
V_{WAKE}	WAKE input voltage	-0.3	58 and ≤V_{BAT}+0.3	V
V_{INH}	INH pin voltage	-0.3	58 and ≤V_{BAT}+0.3	V
V_{LOGIC}	Logic pin voltage	–0.3	6	V
$I_{O(LOGIC)}$	Logic output current (RXD, ERR_N)		8	mA
$I_{O(INH)}$	INH pin output current		6	mA
$I_{O(WAKE)}$	WAKE pin output current		3	mA
T_J (2)	Junction temperature	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C

Notes:

(1) Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in “Recommended Operating Conditions”. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C

7.2 ESD Ratings

			MIN	UNIT
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	ESD Resistivity to GND, CANH, CANL	±8000	V
		ESD Resistivity to GND, TXD, VCC, RXD, VIO, EN, ERR_N, n.c., STB_N	±5000	V
		On pin WAKE	±4000	V
		On pin INH	±2000	V
		ESD Resistivity to GND, BAT	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±2000	V
	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) (3)	ESD Resistivity to GND, CANH, CANL with PESD2CANFD27L and ACT45B-2P-TL003	±30	kV
		ESD Resistivity to GND, CANH, CANL (Unpowered Contac Discharge)	±4000	V
		ESD Resistivity to GND, VBAT with 100nF capacitor (Unpowered Contact Discharge)	±25	kV
		ESD Resistivity to GND, WAKE with 33kΩ resistor (Unpowered Contact Discharge)	±2	kV

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

(3) Testing performed by OEM-approved independent 3rd part, EMC report available upon request

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{BAT}	Battery supply voltage	4.5	45	V
V_{CC}	CAN transceiver supply voltage	4.5	5.5	V
V_{IO}	I/O supply voltage	1.71	5.5	V
$I_{OH(DO)}$	Digital output high-level current	–2		mA
$I_{OL(DO)}$	Digital output low-level current		2	
$I_{O(INH)}$	INH output current		4	mA
T_A	Operating temperature	-40	125	°C

7.4 Thermal Information

Thermal Metric		MCAN1463BXXX-Q1		UNIT
		SOP14	DFN14	
$R_{\theta JA}$	Junction-to-air thermal resistance	59.3	40	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	-	5.4	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	18.4	-	°C/W
T_{TSD}	Thermal shutdown temperature	180	180	°C
T_{TSD_HYS}	Thermal shutdown hysteresis	20	20	°C

7.5 Electrical Characteristics

V_{BAT}=12V, V_{CC}=V_{IO}=5V, R_L=60Ω, Typical values correspond to T_A=25°C, Minimum and Maximum limits apply over -40°C to 125°C operating temperature range unless otherwise indicated.

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Power supply characteristics						
I_{BAT_NORMAL}	V_{BAT} supply current	Normal mode		28	56	μA
I_{BAT_STBY}		Standby mode		15	30	μA
I_{BAT_SLEEP}		Sleep mode		13	26	μA
$UV_{BAT(R)}$	Under-voltage V_{BAT} threshold rising	V_{BAT} rising	3.6	4	4.4	V
$UV_{BAT(F)}$	Under-voltage V_{BAT} threshold falling	V_{BAT} falling	3.4	3.8	4.2	V
$V_{HYS(UVBAT)}$	Hysteresis voltage on UV_{BAT}			200		mV
I_{CC_NORMAL}	Normal mode Dominant	R_L=60Ω, TXD=0V, CL=open See Figure 11		38	65	mA
		R_L=50Ω, TXD=0V, CL=open See Figure 11		42	70	
	Normal mode Dominant with bus fault	R_L=C_L=open, TXD=0V V_{CANH}=-25V, See Figure 11			115	mA
	Normal mode Recessive	R_L=60Ω, TXD=V_{IO}, C_L=open See Figure 11		1.4	3	mA
I_{CC_STBY}	Standby mode	TXD=V_{IO}, EN=STB_N=0V See Figure 11		0.8	2	mA
I_{CC_SLEEP}	Sleep mode	TXD=EN=V_{IO}, STB_N=0V See Figure 11		0.8	2	mA
$UV_{CC(R)}$	Under-voltage V_{CC} threshold rising	V_{CC} rising		4.2	4.5	V
$UV_{CC(F)}$	Under-voltage V_{CC} threshold falling	V_{CC} falling	3.5	4		V
$V_{HYS(UVCC)}$	Hysteresis voltage on UV_{CC}			200		mV
I_{IO_NORMAL}	Normal mode Dominant	TXD=0V, RXD floating		17	30	μA
	Normal mode Recessive	TXD=V_{IO}, RXD floating		0.45	5	μA
I_{IO_STBY}	Standby mode	TXD=V_{IO}, EN=STB_N=0V		0.45	2	μA
I_{IO_SLEEP}	Sleep mode	TXD=EN=V_{IO}, STB_N=0V		0.48	2	μA
$U_{VIO(R)}$	Under-voltage V_{IO} threshold rising	V_{IO} rising		1.5	1.7	V
$U_{VIO(F)}$	Under-voltage V_{IO} threshold falling	V_{IO} falling	1.1	1.3		V
$V_{HYS(UVIO)}$	Hysteresis Voltage on UV_{IO}			150		mV

INH Characteristics						
ΔV_H	High-level voltage drop from V_{BAT} to INH(V_{BAT}-V_{INH})	I_{INH}= –2mA		0.5	1	V
R_{PD}	Pull-down resistance	Sleep Mode, INH=1V	7	10	12	MΩ
WAKE Characteristics						
V_{IH}	High-level input voltage	Sleep mode	4			V
V_{IL}	Low-level input voltage				2	V
I_{IL}	Low-level input leakage current	WAKE=1V		1	3	μA
TXD Characteristics (3)						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	TXD=V_{CC}=V_{IO}=5V	-1		1	μA
I_{IL}	Low-level input leakage current	TXD=0V, V_{IO}=5V	-30		-2.5	μA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD=5V, V_{BAT}=V_{CC}=V_{IO}=0V	-1		1	μA
C_I (1)	Input capacitance			2.5		pF
STB_N Characteristics (3)						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	STB_N=V_{CC}=V_{IO}=5V	3		7	μA
I_{IL}	Low-level input leakage current	STB_N =0V, V_{CC}=V_{IO}=5V	-1		-1	μA
$I_{LKG(OFF)}$	Unpowered leakage current	STB_N =5V, V_{BAT}=V_{CC}=V_{IO}=0V	-1		1	μA
EN Characteristics (3)						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	STB_N=V_{CC}=V_{IO}=5V	3		7	μA
I_{IL}	Low-level input leakage current	STB_N =0V, V_{CC}=V_{IO}=5V	-1		-1	μA
$I_{LKG(OFF)}$	Unpowered leakage current	STB_N =5V, V_{BAT}=V_{CC}=V_{IO}=0V	-1		1	μA
RXD Characteristics						
V_{OH}	High-level output voltage	I_O=-2mA	0.8			V_{IO}
V_{OL}	Low-level output voltage	I_O=-2mA			0.2	V_{IO}
$I_{LKG(OFF)}$	Unpowered leakage	RXD=5V, V_{BAT}=V_{CC}=V_{IO}=0V	-1		1	μA
ERR_N Characteristics						
V_{OH}	High-level output voltage	I_O=-2mA	0.8			V_{IO}
V_{OL}	Low-level output voltage	I_O=-2mA			0.2	V_{IO}
$I_{LKG(OFF)}$	Unpowered leakage	RXD=5V, V_{BAT}=V_{CC}=V_{IO}=0V	-1		1	μA
CAN Driver Characteristics						
$V_{O(DOM)}$	Dominant output voltage	CANH	TXD=0V, 50Ω≤R_L≤65 Ω, C_L=open, R_{CM}=open, See Figure 12 and Figure 13	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage		TXD=V_{IO}, R_L=open, R_{CM}=open, See Figure 12 and Figure 13	2		3	V
							V
$V_{O(STB)}$	Standby mode output voltage	CANH	TXD= V_{IO}, STB_N=0V, R_L=open, C_L= open, R_{CM}=open, See Figure 12 and Figure 13	-0.1	0	0.1	V
		CANL		-0.1	0	0.1	V
		CANH-CANL		-0.2	0	0.2	V

$V_{OD(DOM)}$	Differential output voltage Dominant	CANH-CANL	TXD=0V, STB_N=V_{IO}, 45Ω≤R_L≤70Ω, C_L=open, R_{CM}=open, See Figure 12 and Figure 13	1.4		3	V
			TXD=0V, STB_N=V_{IO}, 50Ω ≤R_L≤65 Ω, C_L=open R_{CM}=open, See Figure 12 and Figure 13	1.5		3	V
			TXD=0V, STB_N=V_{IO}, R_L=2240Ω, C_L =open R_{CM}=open, See Figure 12 and Figure 13	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Recessive	CANH-CANL	TXD=STB_N=V_{IO}, R_L=60Ω, C_L=open, R_{CM}=open, See Figure 12 and Figure 13	-12		12	mV
			TXD=STB_N=V_{IO}, R_L=open, C_L=open R_{CM}=open, See Figure 12 and Figure 13	-50		50	mV
V_{SYM}	Output symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{CC}		STB_N=V_{IO}, R_L=60Ω, C_{SPLIT}=4.7nF, C_L =open, R_{CM}=open, TXD=250kHz,1 MHz, 2.5MHz, See Figure 12 and Figure 13	0.9		1.1	V
V_{SYM_DC}	DC output symmetry V_{CC}-($V_{O(CANH)}$ + $V_{O(CANL)}$)		STB_N=V_{IO}, R_L=60 Ω, C_L=open, R_{CM}= open, See Figure 12 and Figure 13	-0.4		0.4	V
$I_{OS(SS\_DOM)}$	Short-circuit output current, Dominant, Normal mode		TXD=0, STB_N=V_{IO}, $V_{(CANH)}$= -15V to 27V, CANL=open, See Figure 20	-115			mA
			TXD=0, STB_N=V_{IO}, $V_{(CANL)}$= -15V to 27V, CANH=open, See Figure 20			115	mA
$I_{OS(SS\_REC)}$	Short-circuit output current, Recessive, Normal mode		TXD=STB_N=V_{IO}, V_{BUS}= -27V to 32V, V_{BUS} = V_{CANH} = V_{CANL} See Figure 20	-3		3	mA
CAN Receiver Characteristics							
V_{CM}	Common mode range Normal mode		STB_N=V_{IO}, See Figure 15, Figure 16 and Table 5	-30		30	V
V_{IT+}	Positive-going input threshold voltage, Normal mode.		TXD=STB_N=V_{IO} -30V ≤ V_{CM} ≤ +30V See Figure 15, Figure 16 and Table 5	900			mV
V_{IT-}	Negative-going input threshold voltage, Normal mode.					500	mV
V_{HYS}	Hysteresis voltage				120		mV
V_{CM_STB}	Common mode range		STB_N=0V, See Figure 15, Figure 16 and Table 5	-12		12	V

	Standby mode					
$V_{IT(STB)}$	Input threshold voltage Standby mode	STB_N=0V, -12V ≤ V_{CM} ≤ +12V See Figure 15, Figure 16 and Table 5	400		1150	mV
$V_{REC(RX)}$	Receiver recessive voltage Normal mode	STB_N=VIO -30V ≤ VCANH ≤ +30 V, -30V ≤ VCANL ≤ +30 V	-3		0.5	V
	Receiver recessive voltage Standby mode	STB_N=0V -12V ≤ VCANH ≤ +12 V, -12V ≤ VCANL ≤ +12 V	-3		0.4	V
$V_{DOM(RX)}$	Receiver dominant voltage Normal mode	STB_N=VIO -30V ≤ VCANH ≤ +30 V, -30V ≤ VCANL ≤ +30 V	0.9		9	V
	Receiver dominant voltage Standby mode	STB_N=0V -12V ≤ VCANH ≤ +12 V, -12V ≤ VCANL ≤ +12 V	1.15		9	V
$I_{LKG(OFF)}$	Unpowered bus input leakage current	CANH = CANL = 5V, V_{CC} = V_{IO}=V_{BAT}=0V			1	μA
C_I (1)	Input capacitance to ground (CANH or CANL)	TXD=V_{CC}=V_{IO}		21		pF
C_{ID} (1)	Differential input capacitance			10.5		pF
R_{ID}	Differential input resistance	TXD=V_{CC}=V_{IO}=5V, STB_N=5V, –30V≤V_{CM} ≤30V	40		90	KΩ
R_{IN}	Input resistance (CANH or CANL)		20		45	KΩ
$R_{IN(M)}$	Input resistance matching [1 – $R_{IN(CANH)}$ / $RIN_{(CANL)}$] × 100%	V_{CANH}=V_{CANL}=5 V	-2		2	%
Undervoltage Detection Characteristics (1)						
$t_{DET(UV)}$	Undervoltage recovery time on V_{CC} and V_{IO}	V_{CC} ≤ UV_{CC} or V_{IO} ≤ UV_{IO}			50	us
$t_{DET(UV)\ long}$	Long undervoltage detection time on V_{CC} and V_{IO}	V_{CC} ≤ UV_{CC} or V_{IO} ≤ UV_{IO}		300		ms
$t_{REC\ (UV)}$	Undervoltage recovery time on V_{CC} and V_{IO}	Time for device to return to normal operation from a UV_{CC} or UV_{IO} undervoltage event			50	us
Mode Change Characteristics (1)						
t_{PWRUP}	Time from VBAT exceeding VBAT UV until INH active	See Figure 22		1.9		ms
t_{MODE}	Mode change transition time	See Figure 18			50	us
$t_{INH\_SLP\_STB}$	Time after WUP or LWU event until INH asserted	See Figure 27			100	us
tgotosleep	go-to-sleep hold time	STB_N = LOW and EN = HIGH hold time for entering Sleep mode			50	us

Device Time Characteristics						
t_{WAKE}	Wake up time from a wake edge on WAKE, Standby or sleep mode, See Figure 25		50			us
$t_{WAKE\_INVALID}$	WAKE pin pulses shorter than this will be filtered out				20	us
t_{WK_FILTER}	Bus time to meet filtered bus requirements for wake-up request See Figure 27		0.5		1.8	us
$t_{WK\_TIMEOUT}$ (1)	Bus wake-up timeout value, See Figure 27		0.8		2	ms
t_{BIAS} (1)	Time from the start of a dominant-recessive-dominant sequence. Each phase 6 µs until V_{SYM}≥ 0.1, See Figure 21				250	us
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, See Figure 17		65	140	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive			75	140	ns
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (Dominant to Recessive)	R_L=60Ω, C_L=100pF, R_{CM}=open, See Figure 13			60	ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (Recessive to Dominant)				60	ns
$t_{SK(P)}$	Pulse skew ($\|t_{pHR}- t_{pLD}\|$)			5		ns
t_R	Differential output signal rise time			25		ns
t_F	Differential output signal fall time			20		ns
t_{TXD_DTO}	Dominant timeout	TXD=0V, R_L=60 Ω, C_L=open, See Figure 19	1.2		3.8	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high RXD output	$C_{L(RXD)}$=15pF See Figure 16			80	ns
t_{pDL}	Propagation delay time, bus dominant input to low RXD output				80	ns
t_R	Output signal rise time (RXD)			3		ns
t_F	Output signal fall time (RXD)			3		ns
t_{BUSDOM_DTO} (1)	Dominant time out	R_L=60 Ω, C_L=open	1.2		3.8	ms
Signal Improvement Timing Characteristics Characteristic						
$t_{SIC\_TX\_base}$	Signal Improvement time TX-base	Time from rising edge of the TXD signal to the end of the signal improvement phase			530	ns

$\Delta t_{bit(Bus)}$	Transmitted bit width variation	STB_N = V_{IO}, RL= 60Ω, C_L=100pF	-10		10	ns
$\Delta t_{bit(RXD)}$	Received bit width variation		-30		20	ns
Δt_{REC}	Received timing symmetry		-20		15	ns
CAN FD Time Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$=500ns	R_L=60Ω, C_L=100pF $C_{L(RXD)}$=15 pF See Figure 17	490		510	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$=200ns		190		210	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$=125ns(2)		115		135	ns
$t_{BIT(RXD)}$	Bit time on RXD bus output pins with $t_{BIT(TXD)}$=500ns		470		520	ns
	Bit time on RXD bus output pins with $t_{BIT(TXD)}$=200ns		170		210	ns
	Bit time on RXD bus output pins with $t_{BIT(TXD)}$=125ns(2)		95		135	Ns
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$=500ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$, See Figure 17	-20		15	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$=200ns		-20		15	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$=125ns(2)		-20		15	ns

Notes:

(1) Specified by design and verified via bench characterization, not tested in production.

(2) Measured during characterization and not an ISO 11898-2:2016 parameter.

(3) TXD, STB_N, EN level should not exceed V_{IO}.

7.6 Typical Characteristics

V_{BAT}=12V, V_{CC}=5V, V_{IO}=5V, R_L=60Ω, C_L=Open, RCM=Open, T_A=25°C, unless otherwise specified.

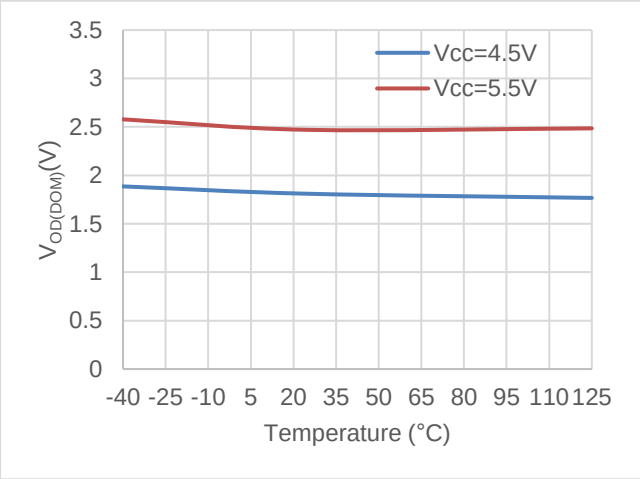


Figure 5.$V_{OD(DOM)}$ VS Temperature and V_{CC}

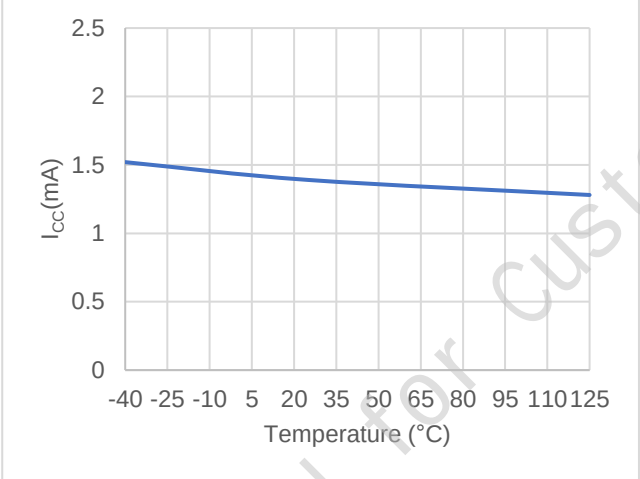


Figure 6. I_{CC} Recessive VS Temperature

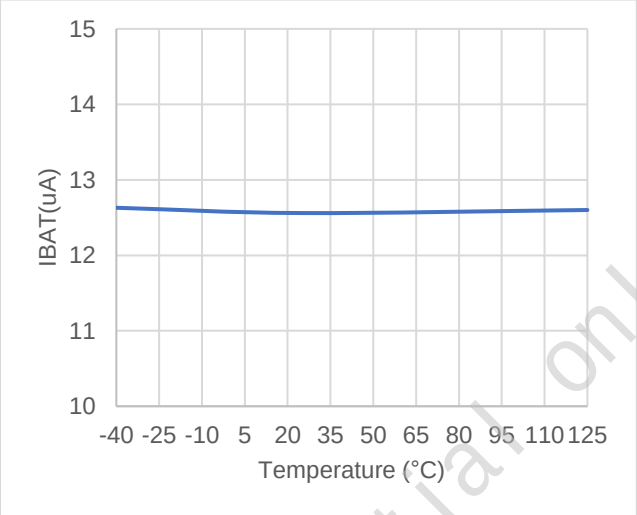


Figure 7. Sleep Mode：I_{BAT} VS Temperature

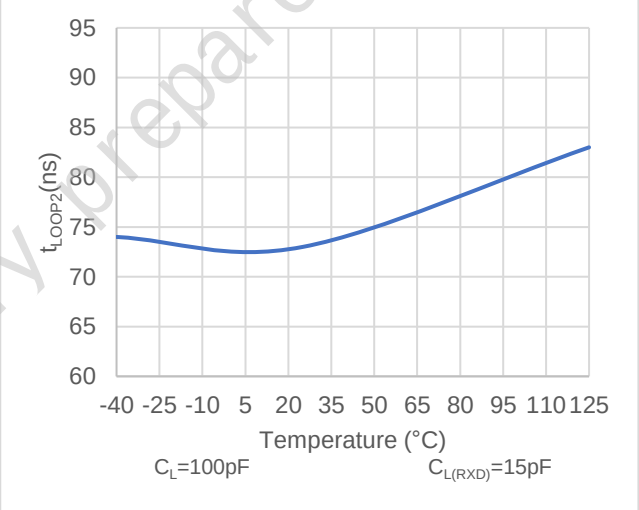


Figure 8.Total Loop Delay VS Temperature

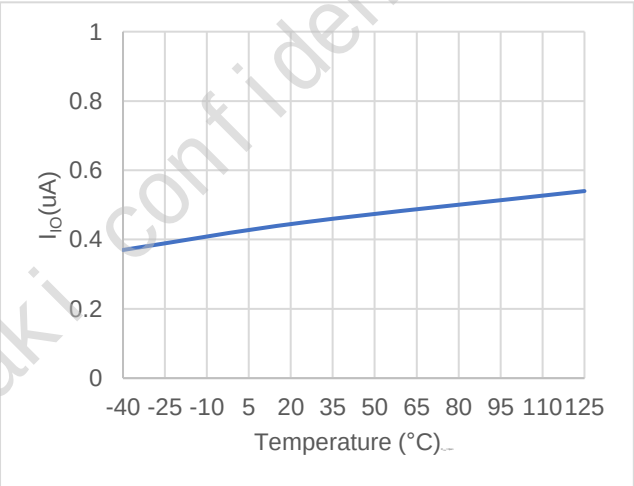


Figure 9.Normal Mode, Recessive：I_{IO} VS Temperature

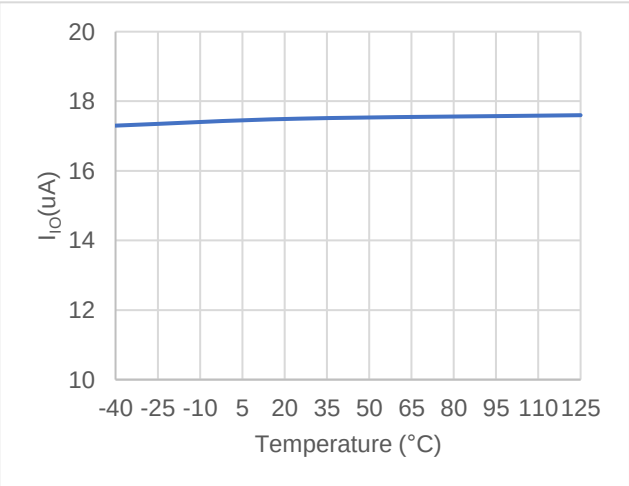


Figure 10.Normal Mode, Dominant：I_{IO} VS Temperature

8 Parameter Measurement Information

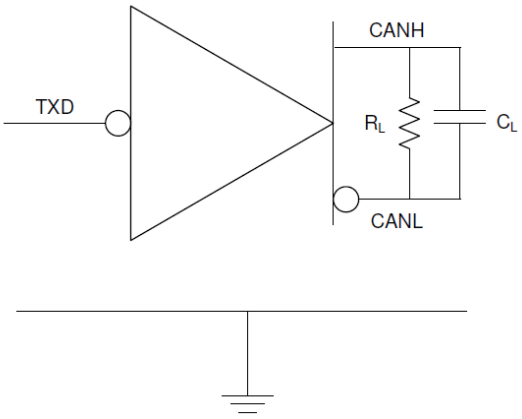


Figure 11. Supply Test Circuit

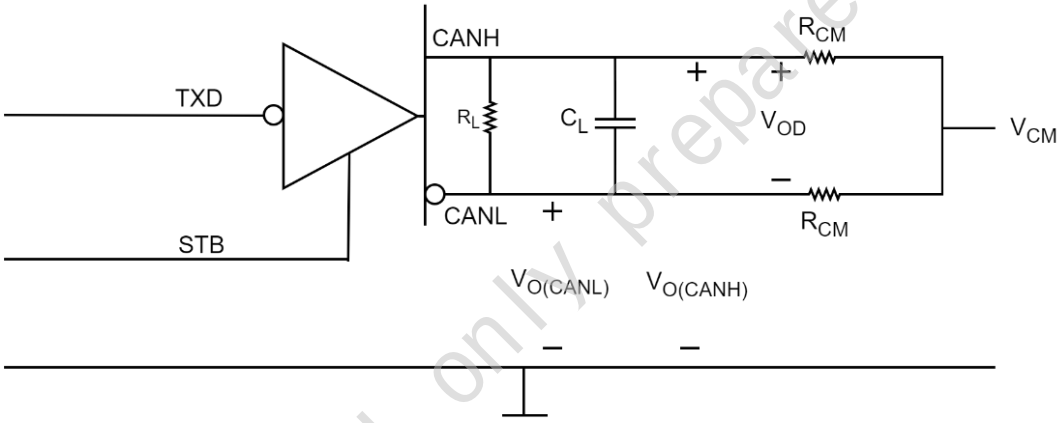


Figure 12.Driver Test Circuit

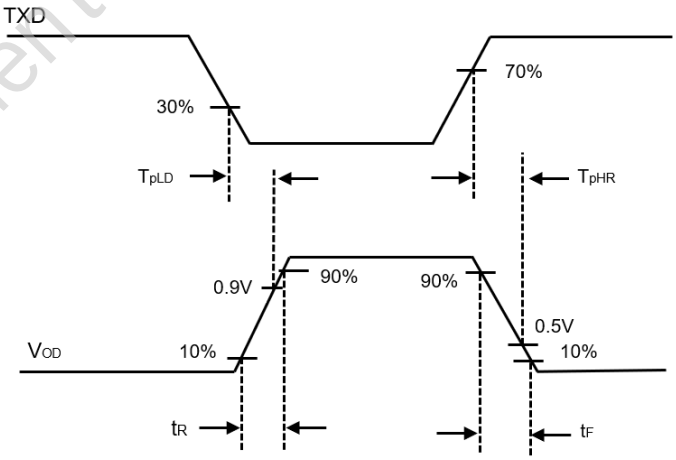


Figure 13. Driver Characteristic Measurement

Notes:

(1) The input signal on TXD shall have risen times and fall times (10% to 90%) of less than 10ns.

(2) C_L includes instrumentation and capacitance introduced by other CAN nodes.

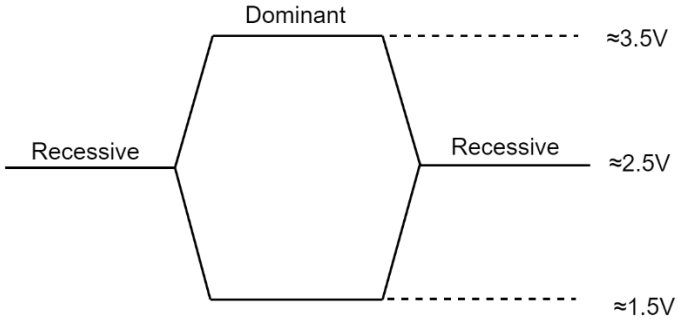


Figure 14. Bus Logic State and Voltage Definitions

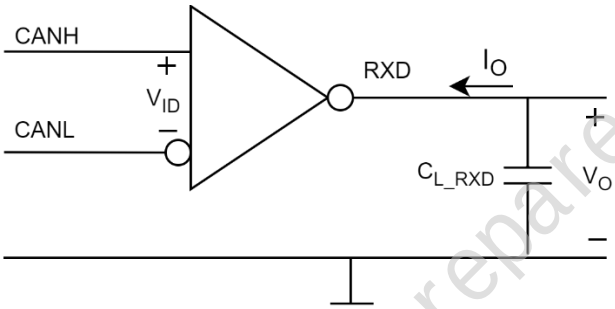


Figure 15. Receiver Test Circuit

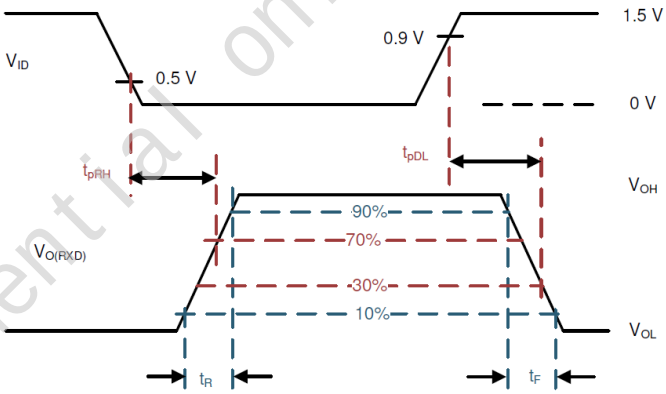


Figure 16. Receiver Characteristic Measurement

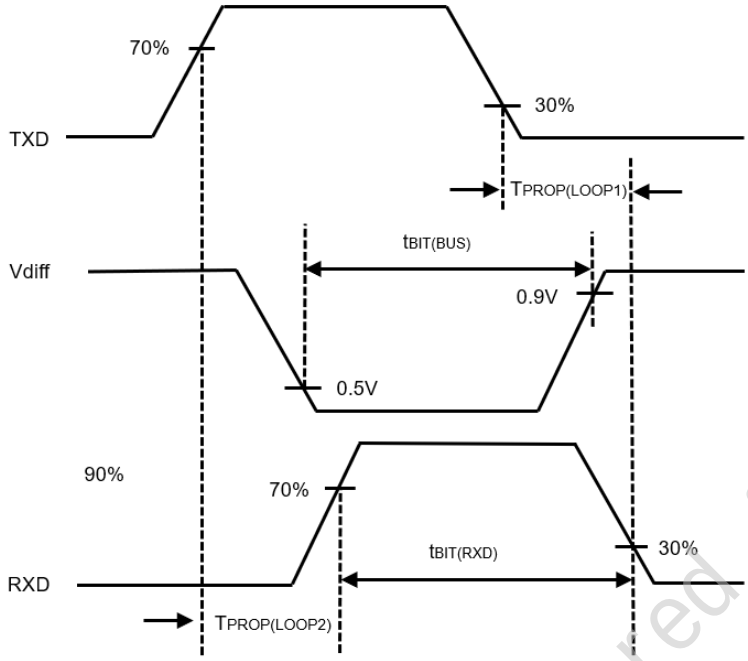


Figure 17. $T_{PROP(LOOP)}$ and CAN FD Timing Parameter Measurement

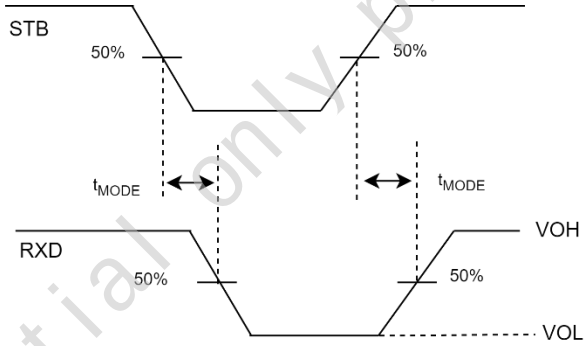


Figure 18. t_{MODE} Measurement

Note:

(1) The rise of STB and EN should be less than 500ns when the system changes the mode by changing the state of STB or EN, to prevent INH output instability.

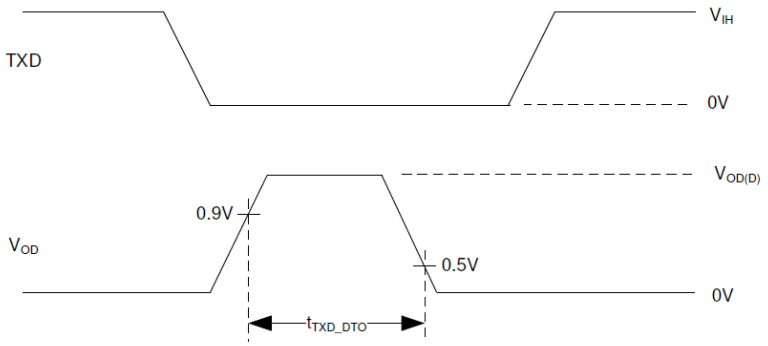


Figure 19. TXD Dominant Timeout Parameter Measurement

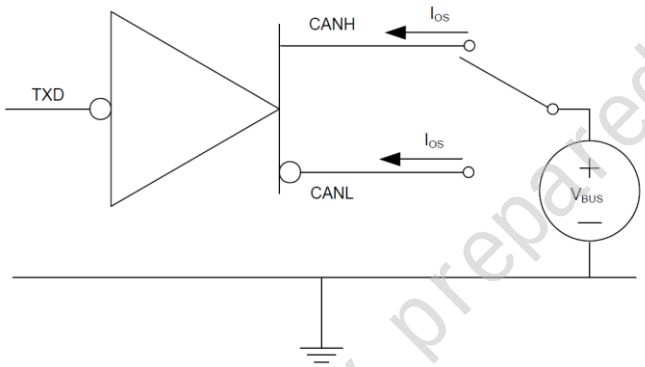


Figure 20. Driver Short-Circuit Current Test

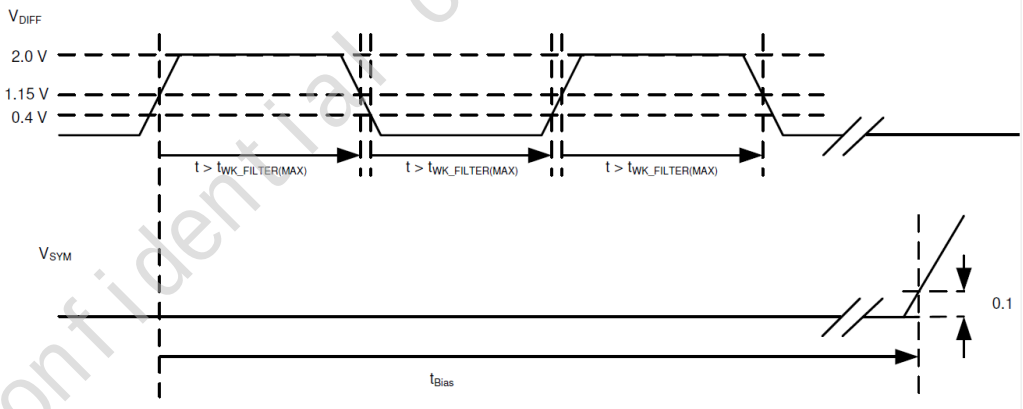


Figure 21. Test Signal Definition for Bias Reaction Time Measurement

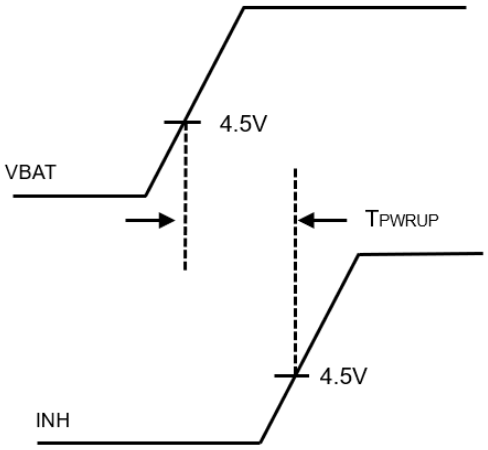


Figure 22.Power Up Timing

9 Detailed Description

9.1 Overview

The MCAN1463B meets the physical layer requirements of the ISO 11898-2:2016 and CiA 601-4 high speed CAN specifications. The devices support CAN FD networks up to 8 Mbps (megabits per second).

The device helps reduce battery current consumption by controlling the power supply via the INH output while supporting local and remote wake-up. This allows a low-power sleep state to further reduce system-level power consumption by powering off all system component except for the MCAN1463B.

The MCAN1463B includes many protection and diagnostic features including undervoltage detection, CAN bus fault detection, SWE timer, battery connection detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and bus fail detection.

The MCAN1463B includes the Signal Improvement Capability (SIC) that enhances the maximum data rate achievable in complex star topologies by minimizing signal ringing. An example of a star network is shown below.

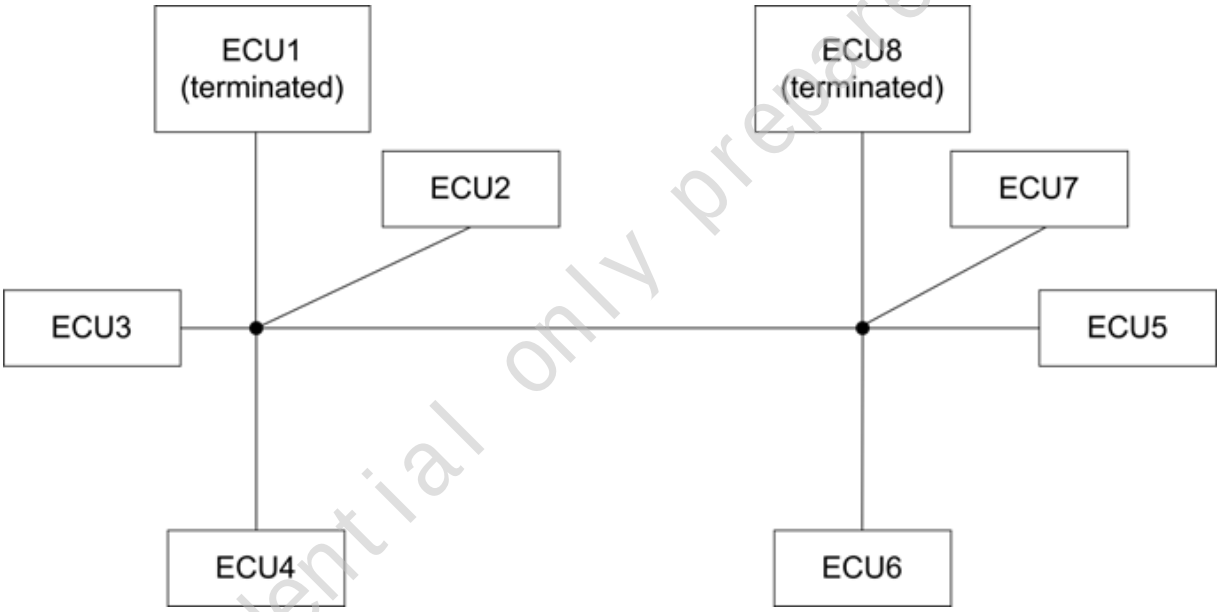


Figure 23. CAN Network: Star topology

9.2 Functional Block Diagram

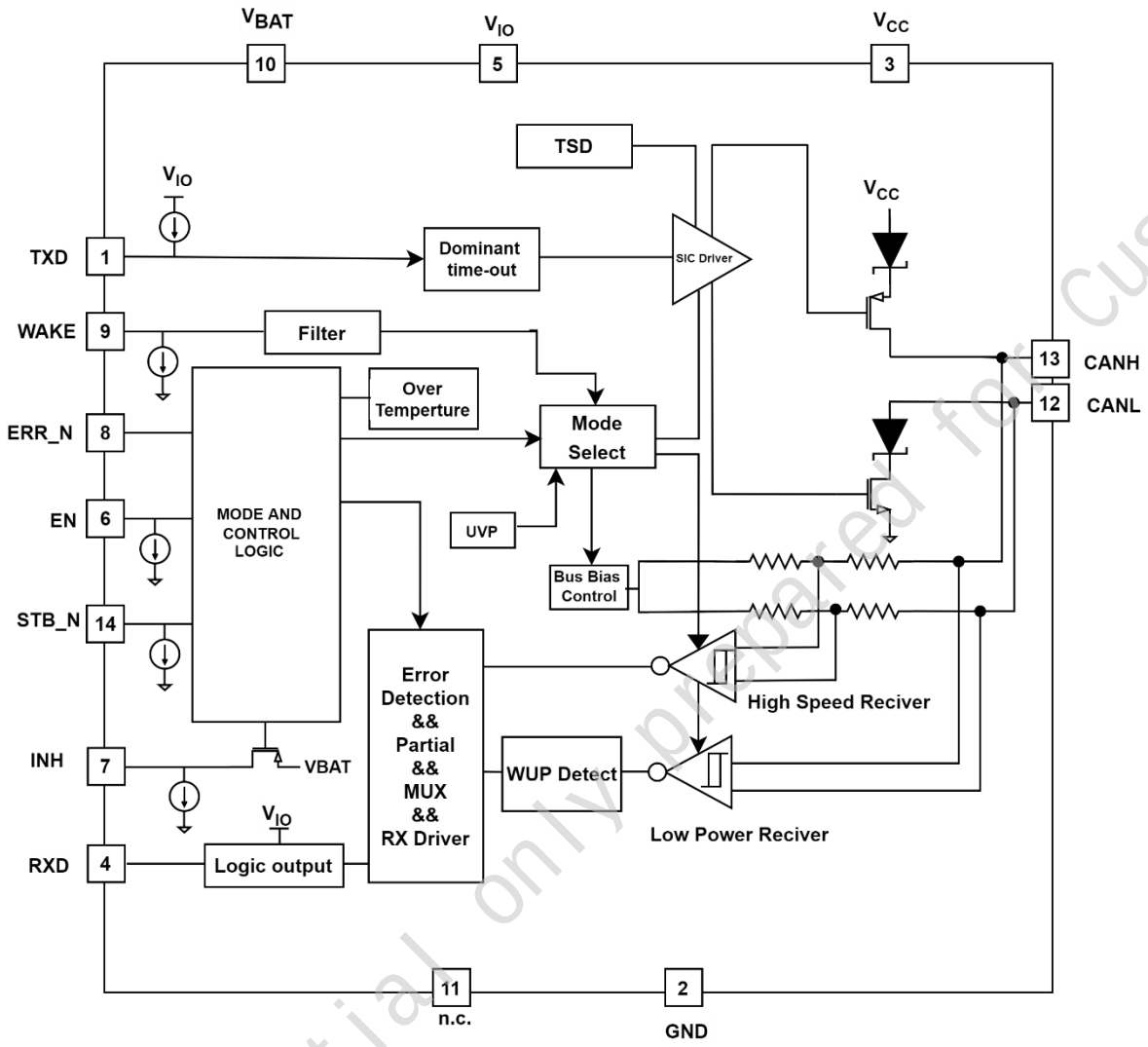


Figure 24. Function Block Diagram

9.3 Feature Description

9.3.1 Pin Description

9.3.1.1 V_{BAT} Pin

This pin is connected to the battery supply. It provides the supply to the internal regulators that support the digital core and the low power CAN receiver.

9.3.1.2 V_{CC} Pin

This pin provides the 5 V supply voltage for the CAN transceiver.

9.3.1.3 V_{IO} Pin

This pin provides the digital I/O voltage to match the CAN FD controller's I/O voltage. It supports I/O voltages from 1.7 V to 5.5 V providing a wide range of controller support.

9.3.1.4 TXD Pin

TXD is a logic-level input signal, referenced to V_{IO}, from a CAN FD controller to the MCAN1463B.

9.3.1.5 RXD Pin

RXD is a logic-level signal output, referenced to VIO, from the MCAN1463B to a CAN FD controller. The RXD pin is driven to the VIO level as logic-high outputs once a valid VIO is present.
When a wake-up event takes place, the RXD pin is pulled low.

9.3.1.6 ERR_N Pin

ERR_N is a logic-level output signal, referenced to V_{IO}, from the MCAN1463B to a CAN FD controller. Then ERR_N output is driven to the V_{IO} level as logic-high output. The ERR_N output is used to transmit the MCAN1463B status indicator flags to the CAN FD controller. Please see Table 2. Accessing internal flags via pin ERR_N for the specific fault scenarios that are indicated externally via the ERR_N pin.

9.3.1.7 EN and STB_N Pin

EN and STB_N is a logic-level input signal, referenced to V_{IO}, from a CAN FD controller to the MCAN1463B. The EN and STB_N input pin is for mode selection. EN and STB_N is internally pulled low to prevent excessive system power and false wake-up events.

9.3.1.8 INH Pin

The INH pin is a high-voltage output. It can be used to control external regulators. These regulators are usually used to support the microprocessor and VIO pin. The INH function is on in all modes except for sleep mode. In sleep mode, the INH pin is turned off, going into a high-impedance state. This allows the node to be placed into the lowest power state while in sleep mode.

This terminal should be considered a high-voltage logic terminal, not a power output. The INH pin should be used to drive the EN terminal of the systems power management device and should not be used as a switch for the power management supply itself. This terminal is not reverse-battery protected and thus should not be connected outside the system module.

9.3.1.9 WAKE Pin

The WAKE pin is a high-voltage reverse-blocked input used for the local wake-up (LWU) function. A local wake-up request is registered when the logic level on pin WAKE changes and the new level remains stable for at least t_{WAKE}.

9.3.1.10 CAN BUS Pin

These are the CAN high and CAN low, CANH and CANL, differential bus pins. These pins are internally connected to the CAN transceiver and the low-voltage wake receiver.

9.3.2 Internal flags

The MCAN1463B makes use of five internal flags for its fail-safe fallback mode control and system diagnosis support. Five of these flags can be polled by the controller via pin ERR_N. Which flag is available on pin ERR_N at any time depends on the active operating mode and on a few other conditions. Table 2 describes how to access these flags.

Table 2. Accessing internal flags via pin ERR_N

Internal flag	Flag available on pin ERR_N (1)	Flag set	Flag cleared
PWRON	In Listen-only mode (coming from Standby or Sleep mode)	V_{BAT} has risen above $UV_{BAT(R)}$	on entering Normal mode
Wake	In Standby and Sleep modes (Provided V_{IO} and V_{BAT} are present)	remote or local wake-up detected OR PWRON flag has been set	on entering Normal mode OR setting the U_{VNOM} flag
Wake-up source	in Normal mode (before the fourth dominant-to-recessive edge on pin TXD (2)	local wake-up OR PWRON flag has been set	on leaving Normal mode
UV_{NOM}	No indicated	$V_{CC}<UV_{CC(F)}$ for $t > t_{DET(UV)}$ OR $V_{IO}<UV_{IO(F)}$ for $t > t_{DET(UV)}$	$V_{CC}>UV_{CC(R)}$ for $t > t_{REC(UV)}$ and $V_{IO}>UV_{IO(R)}$ for $t > t_{REC(UV)}$ OR a wake-up request occurs
UV_{BAT}	No indicated	$V_{BAT}< UV_{BAT(F)}$	$V_{BAT}>UV_{BAT(R)}$ for $t > t_{PWRUP}$
Bus failure	in Normal mode (after the fourth dominant-to-recessive edge on pin TXD (2)	CANH/CANL Shorted to V_{BAT}, V_{CC}, GND	on re-entering Normal mode OR by setting the PWRON flag
Local failure	in Listen-only mode (coming from Normal mode)	on occurrence of: - TXD dominant failure OR - TXD-RXD short circuit OR - Bus dominant failure OR - Overtemperature	setting the PWRON flag OR on entering Normal mode (Provided that all local failures are resolved) OR RXD is dominant while TXD is recessive (Provided that all local failures are resolved)

Notes:

(1) Pin ERR_N is an active-LOW output, so a Low-level indicates a set flag and a High-level indicates a cleared flag. Flag available on pin ERR_N after delay 8us, When the conditions indicating flag are met.

(2) Allow for a TXD dominant time of at least 4us per dominant-recessive cycle.

9.3.2.1 PWRON flag

PWRON is the VBAT power-on flag. This flag is set when the voltage on pin VBAT above $UV_{BAT(R)}$ (usually because the battery was connected). The PWRON flag can be used for cold start diagnosis. The Wake and Wake-up source flags are set to ensure consistent system power-up under all supply conditions. Coming from Sleep or Standby and entering Listen-Only mode, a LOW level on pin ERR_N signals that the PWRON flag has been set. The flag is cleared when the transceiver enters Normal mode.

9.3.2.2 Wake flag

The Wake flag is set when the transceiver detects a local or remote wake-up request.

9.3.2.3 Local wake-up (via WAKE pin)

A local wake-up request is registered when the logic level on pin WAKE changes and the new level remains stable for at least t_{WAKE}. The Wake flag can be set in Standby or Sleep mode. Setting the Wake flag clears the UV_{NOM} flag and timers. Once set, the Wake flag status is immediately available on pins ERR_N and RXD (provided V_{IO} and V_{BAT} are present). This flag is also set at power-on and cleared when the UV_{NOM} flag is set or the transceiver enters Normal mode.

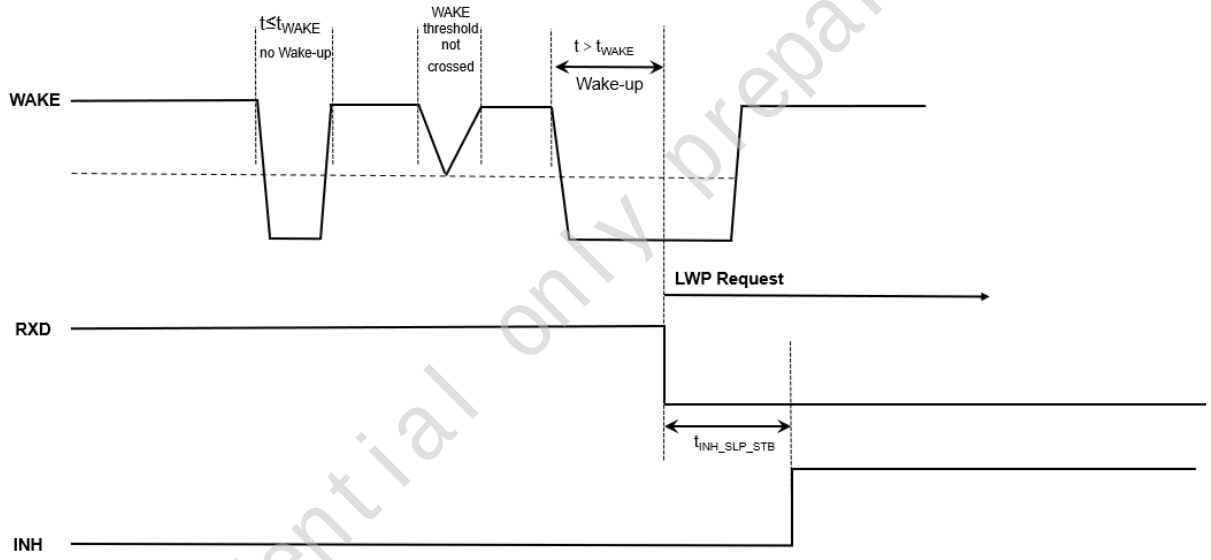


Figure 25. LWU Request Falling Edge

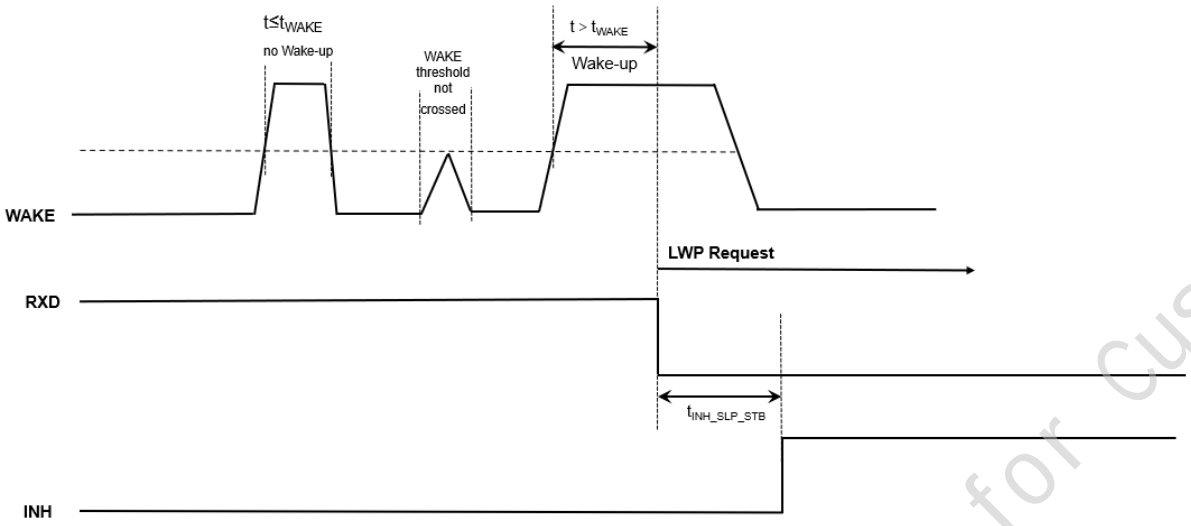


Figure 26. LWU Request Rising Edge

9.3.2.4 Remote wake-up (via the CAN bus)

The MACN1463B wakes up from Sleep to Standby mode when a dedicated wake-up pattern (specified in ISO 11898-2: 2016) is detected on the bus.

The wake-up pattern consists of:

• A dominant phase of at least t_{WK_FILTER} followed by

• A recessive phase of at least t_{WK_FILTER} followed by

• A dominant phase of at least t_{WK_FILTER}

For a dominant or recessive to be considered "filtered," the bus must be in that state for more than t_{WK_FILTER} time. The complete dominant-recessive-dominant pattern must be received within $t_{WK\_TIMEOUT}$ bus to be recognized as a valid wake-up pattern (see Figure 27). Otherwise, the internal wake- up logic is reset. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event. Pins RXD and ERR_N remain HIGH until the wake-up event has been triggered and then switch LOW. Pin INH remains floating until the wake-up event has been triggered and then switches HIGH.

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The device switches to Normal mode
- The complete wake-up pattern was not received within $t_{WK\_TIMEOUT}$
- A V_{CC} or V_{IO} undervoltage is detected

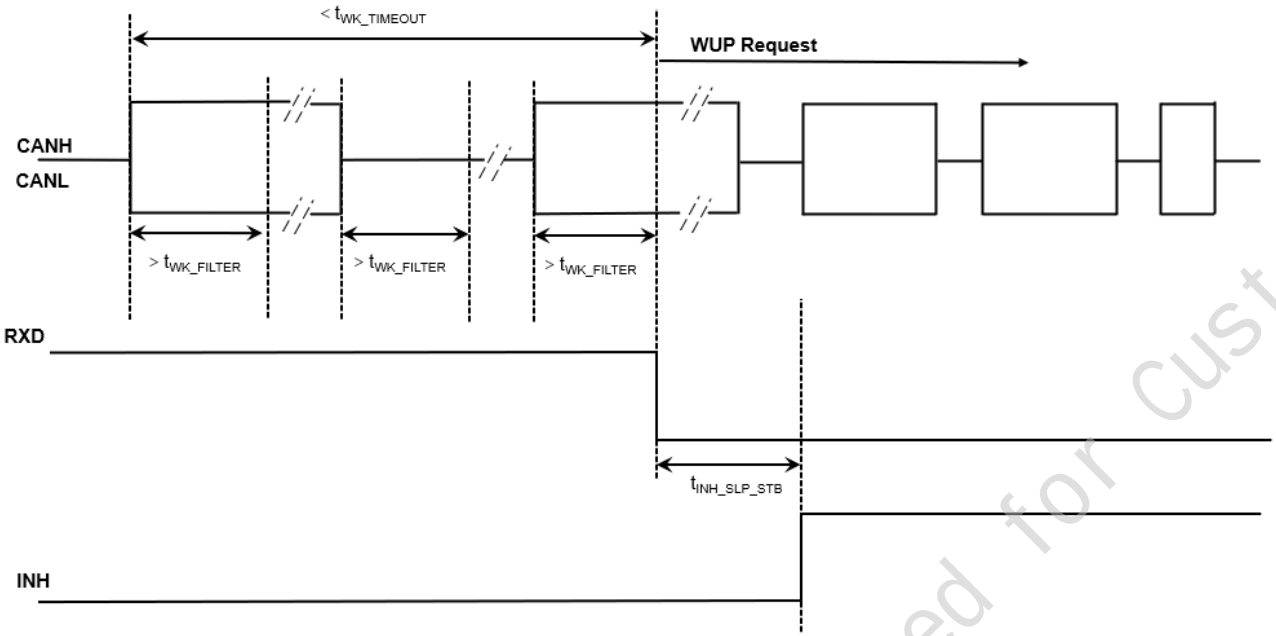


Figure 27. Wake Up Pattern

9.3.2.5 Wake-up source flag

Wake-up source recognition is provided via the Wake-up source flag. It is set after the Wake flag has been set by a local wake-up request via the WAKE pin. The Wake-up source flag can be polled via the ERR_N pin in Normal mode (see Table 2). This flag is also set at power-on and cleared when the transceiver leaves Normal mode.

9.3.2.6 UV_{NOM} flag

UV_{NOM} is the V_{CC} and V_{IO} undervoltage detection flag. The flag is set when the voltage on pin V_{CC} drops below the V_{CC} undervoltage detection voltage (UV_{CC}), for longer than the undervoltage detection time ($t_{DET(UV)}$), or when the voltage on pin V_{IO} drops below (UV_{IO}) for longer than ($t_{DET(UV)}$). When the UV_{NOM} flag is set, the transceiver enters Sleep mode to save power and to ensure the bus is not disturbed. In Sleep mode the voltage regulators connected to pin INH are disabled, avoiding any extra power consumption that might be generated as a result of a short-circuit condition.

Any wake-up request, setting the PWRON flag or a LOW-to-HIGH transition on STB_N will clear UV_{NOM} and the timers, allowing the voltage regulators to be reactivated (at least until UV_{NOM} is set again). UV_{NOM} will also be cleared if both V_{CC} and V_{IO} recover for longer than the undervoltage recovery time (t_{REC}). The transceiver will then switch to the operating mode indicated by the logic levels on pins STB_N and EN.

9.3.2.7 UV_{BAT} flag

UV_{BAT} is the V_{BAT} undervoltage detection flag. This flag is set when the voltage on pin V_{BAT} drops below UV_{BAT}. When UV_{BAT} is set, the transceiver will try to enter Standby mode to save power and will disengage from the bus (zero load). UV_{BAT} is cleared when the voltage on pin V_{BAT} recovers. The transceiver will then switch to the operating mode indicated by the logic levels on pins STB_N and EN.

9.3.2.8 Bus failure flag

The Bus failure flag is set if the transceiver detects a bus line short-circuit condition to V_{BAT}, V_{CC} or GND during four consecutive dominant-recessive cycles on pin TXD, while trying to drive the bus lines dominant. The Bus failure flag can be polled via the ERR_N pin in Normal mode

9.3.2.9 Local failure flag

In Normal and Listen-only modes, the transceiver can distinguish four local failure events, any of which will cause the Local failure flag to be set. The four local failure events are:

- TXD dominant failures
- TXD-to-RXD short circuit
- Bus dominant failures
- Overtemperature

The nature and detection of these local failures is described in Section 9.3.3. The Local failure flag can be polled via the ERR_N pin in Listen-only mode, when coming from Normal mode (see Table 2).

9.3.3 Local failure events

The MCAN1463B can detect four different local failure conditions. Any of these failures will set the Local failure flag, and in most cases the transmitter of the transceiver will be disabled.

9.3.3.1 TXD dominant Timeout (DTO)

A permanent LOW level on pin TXD (due to a hardware or software application failure) would drive the CAN bus into a permanent dominant state, blocking all network communications. The TXD dominant time-out function prevents such a network lock-up by disabling the transmitter if pin TXD remains LOW for longer than the TXD dominant time-out time (t_{TXD_DTO}). The transmitter remains disabled until the Local failure flag has been cleared. The TXD dominant time-out timer is reset when pin TXD is set HIGH.

This flag is cleared:

(1) Power-on when the PWRON flag is set

(2) Provided all local failures have been resolved, when:

The device enters Normal mode OR

RXD is dominant while TXD is recessive

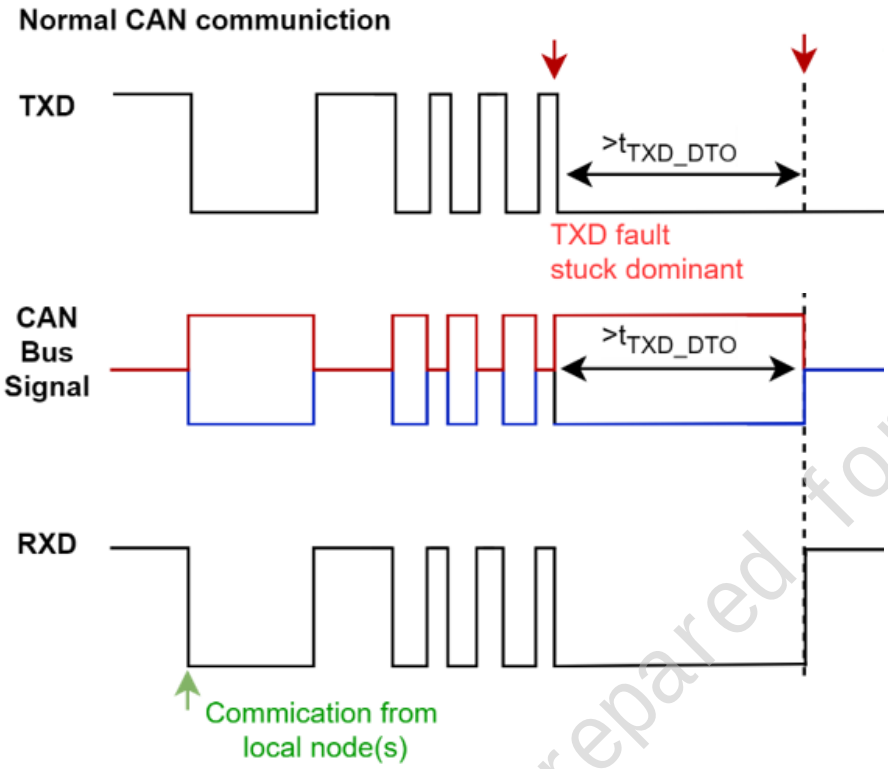


Figure 28. Timing Diagram for TXD DTO

9.3.3.2 TXD-to-RXD short circuit

A short-circuit between pins RXD and TXD would lock the bus in a permanent dominant state once it had been driven dominant, because the low-side driver of RXD is typically stronger than the high-side driver of the controller connected to TXD. TXD-to-RXD short-circuit detection prevents such a network lock-up by disabling the transmitter. The transmitter remains disabled until the Local failure flag has been cleared.

9.3.3.3 Bus dominant failures

A CAN bus short circuit (to VBAT, VCC or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not begin to transmit while the bus is dominant, the host controller would not be able to detect this failure condition. However, bus dominant clamping detection will detect the short circuit. The Local failure flag is set if the dominant state on the bus persists for longer than t_{BUSDOM_DTO}. By checking this flag, the controller can determine if a clamped bus is blocking network communications. There is no need to disable the transmitter. Note that the Local failure flag is reset as soon as the bus returns to recessive state.

9.3.3.4 Overtemperature detection

MCAN1463B turns off the CAN driver circuits if the junction temperature exceeds the thermal shutdown temperature 180℃. The CAN bus lines will be recessive and block the TXD-to-Bus transmission path until the junction temperature drops at least below 160℃, which is the thermal shutdown temperature minus the thermal shutdown hysteresis.

9.3.4 CAN Bus Short-Circuit Current Limiting

During Normal mode, the short-circuit current limit circuitry prevents MCAN1463B from damages by limiting the max working current when the CAN bus connects to the battery incorrectly. Short-circuit current limit the current flowing into MCAN1463B when an incorrect voltage is put on the CANH/CANL.

9.3.5 Unpowered Device

The device is designed to be ideal passive if it is unpowered. There is extremely low leakage current through the bus and the logic terminals when the unpowered device is connected to the CAN network. This is critical if some nodes of the network are unpowered while the rest of the network remains in operation. All terminals have extremely low leakage currents when the device is unpowered to avoid loading down other CAN nodes.

9.4 Device Functional Modes

The MCAN1463B contains two independent state machines, a system state machine and a CAN state machine.

9.4.1 System operating modes

The system state machine in the MCAN1463B supports five system operating modes: Normal, Standby, Listen, Sleep, and Off mode. Control pins STB_N and EN are used to select the operating mode. Figure 29 describes how to switch between operating modes.

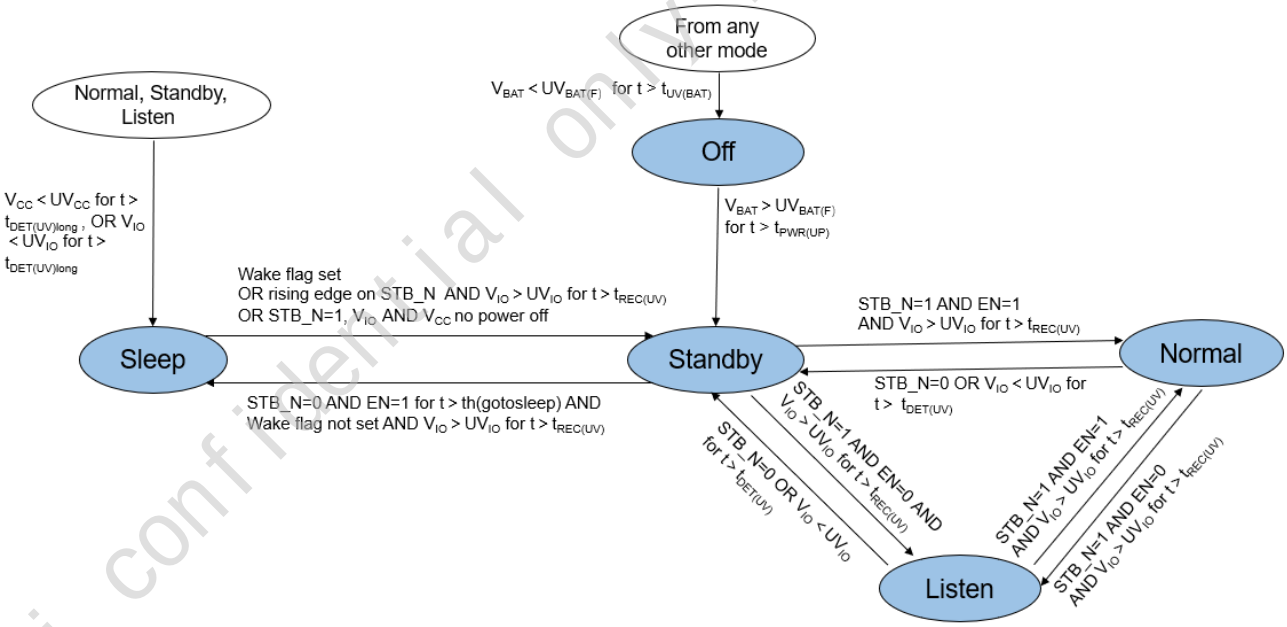


Figure 29.System state transition diagram

Table 3. MCAN1463B Mode Overview

STATE	VCC and VIO	VBAT	EN	STB_N	WAKE Flag	DRIVER	RECEIVER	RXD	INH
Normal	>UV_{CC} and > UV_{IO}	> UV_{BAT}	High	High	X	Enabled	Enabled	Mirror Bus state	High
Listen	>UV_{CC} and > UV_{IO}	> UV_{BAT}	Low	High	X	Disabled	Enabled	Mirror Bus state	High
Standby	>UV_{CC} and > UV_{IO}	> UV_{BAT}	High	Low	set	Disabled	Low Power Receiver is active	Low signals wake-up	High
	>UV_{CC} and > UV_{IO}	> UV_{BAT}	Low	Low	X	Disabled	Low Power Receiver is active	Low signals wake-up	High
	>UV_{CC} and < UV_{IO}	> UV_{BAT}	Low	Low	X	Disabled	Low Power Receiver is active	High impedance	High
Sleep	>UV_{CC} and > UV_{IO}	> UV_{BAT}	High	Low	cleared	Disabled	Low Power Receiver is active	High	Low
	<UV_{CC} and < UV_{IO}	> UV_{BAT}	X	X	X	Disabled	Low Power Receiver is active	High impedance	Low
Protected	X	< UV_{BAT}	X	X	X	Disabled	Disabled	High impedance	High impedance

9.4.1.1 Off mode

The MCAN1463B switches to Off mode from any mode when the battery voltage falls below the undervoltage detection threshold ($UV_{BAT(F)}$). Pins INH and ERR_N are in a high-ohmic state in Off mode.

9.4.1.2 Standby mode

Standby mode is the first-level power-saving mode of the MCAN1463B. When VBAT rises above the undervoltage detection threshold ($UV_{BAT(R)}$), the MCAN1463B starts to boot up, triggering an initialization procedure. It switches to Standby mode after t_{PWRUP}, resulting in a HIGH level on pin INH.

When V_{IO} rises above the undervoltage detection threshold, $UV_{IO(R)}$, the MCAN1463B switches to Normal mode if pins STB_N and EN are HIGH, and to Listen-only mode if STB_N is HIGH and EN is LOW. It will remain in Standby mode if STB_N is LOW and EN is LOW.

The MCAN1463B will switch to Sleep mode if VIO remains below $UV_{IO(F)}$ for $t_{DET(UV)long}$ or VCC remains below $UV_{CC(F)}$ for $t_{DET(UV)long}$. A transition from Standby mode to Sleep mode can also be triggered by holding STB_N LOW and EN HIGH for $t_{h(gotosleep)}$ (also known as a 'go-to-sleep' command). This 'go-to-sleep' command is overruled if the Wake flag is set, in which case the device remains in Standby mode.

In Standby mode, the transceiver is unable to transmit or receive data and the low-power receiver is activated to monitor bus activity.

9.4.1.3 Normal mode

HIGH levels on pin STB_N and pin EN selects Normal mode, provided the battery supply voltage, VBAT, and VIO are present. Pin INH remains HIGH. In Normal mode, both transmitter and receiver are enabled.

9.4.1.4 Listen mode

A HIGH level on pin STB_N and a LOW level on pin EN selects Listen-only mode, provided VBAT and VIO are present. Pin INH remains HIGH. In Listen-only mode the receiver is enabled, but the transmitter is disabled.

9.4.1.5 Sleep mode

Sleep mode is the second-level power-saving mode of the MCAN1463B. Sleep mode is entered in a number of ways:

(1) via Standby mode, STB_N LOW and EN HIGH, and Wake flag not set, VBAT is present

(2) via all other modes, except Off mode, as a result of V_{IO} undervoltage longer than $t_{DET(UV)long}$

(3) via all other modes, except Off mode, as a result of V_{CC} undervoltage longer than $t_{DET(UV)long}$

In Sleep mode, the transceiver behaves as described for Standby mode, with the exception that pin INH is set high-ohmic. Voltage regulators controlled by this pin are switched off and the current into pin VBAT is reduced to a minimum.

A number of events will cause the MCAN1463B to exit Sleep mode, switching to Standby mode:

(1) Setting the Wake flag

(2) A rising edge on pin STB_N (if $V_{IO} > UV_{IO}$)

(3) $V_{CC} > UV_{CC}$ and $V_{IO} > UV_{IO}$, STB_N HIGH.

9.4.2 CAN Operating mode

The MCAN1463B CAN state machine supports six operating modes.

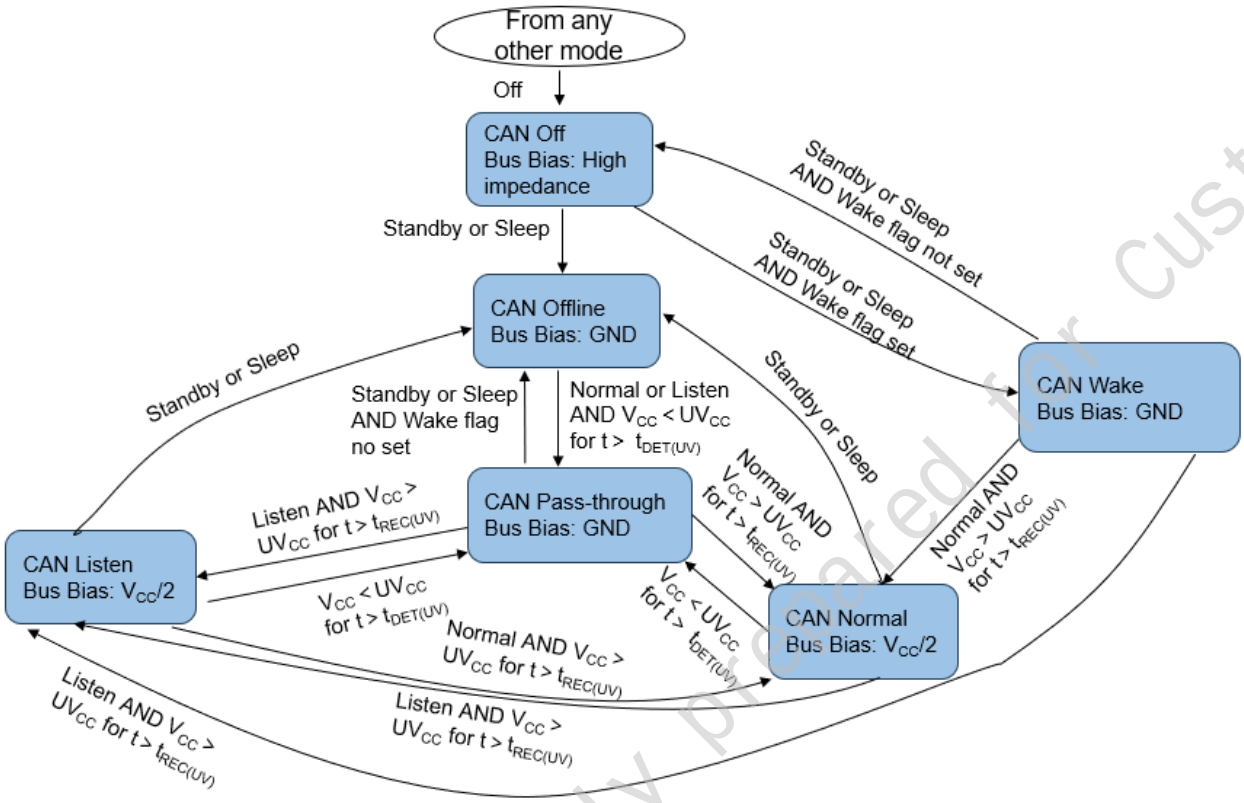


Figure 30. CAN state machine diagram

9.4.2.1 CAN Off mode

When the MCAN1463B system state machine is in Off mode, the CAN state machine will be in CAN Off mode, with the bus pins and pin RXD in a high-ohmic state.

9.4.2.2 CAN Offline mode

When the MCAN1463B system state machine is in Sleep or Standby mode and the Wake flag has not been set, the CAN state machine will be in CAN Offline mode. The bus pins are biased to ground.

The transceiver is unable to transmit or receive data and the low-power receiver is activated to monitor the bus for a wake-up pattern. Pin RXD is HIGH.

9.4.2.3 CAN Wake mode

When the MCAN1463B system state machine is in Sleep or Standby mode and the wake flag has been set, the CAN state machine will be in CAN Wake mode. Pin RXD will be LOW, reflecting the active wake-up request. The bus pins are biased to ground.

9.4.2.4 CAN Pass-through mode

When the MCAN1463B system state machine is in Normal or Listen-only mode and V_{CC} is below the undervoltage detection threshold ($UV_{CC(F)}$), the CAN state machine will be in CAN Pass-through mode.

The transceiver cannot transmit data via the bus lines in this mode. The output voltage on the bus pins is biased to ground. Differential data on the bus pins is converted to digital data via the low-power receiver and the results are output on pin RXD.

9.4.2.5 CAN Active mode

When the MCAN1463B system state machine is in Normal mode and V_{CC} is above the undervoltage detection threshold ($UV_{CC(R)}$), the CAN state machine will be in CAN Active mode. The transceiver can transmit and receive data via bus lines CANH and CANL. Pin TXD must be HIGH at least once in CAN Active mode before the first transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. In order to support high bit rates, especially in CAN FD systems, the Signal Improvement function largely eliminates topology-related reflections and impedance mismatches. In recessive state, the output voltage on the bus pins is $V_{CC}/2$.

9.4.2.6 CAN Listen mode

When the MCAN1463B system state machine is in Listen-only mode and VCC is above the undervoltage detection threshold ($UV_{CC(R)}$), the CAN state machine will be in CAN Listen mode. The transmitter is disabled. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. As in CAN Active mode, the bus pins are biased to $V_{CC}/2$.

9.4.3 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 31. In the dominant bus state, CAN bus is driven differentially, corresponding to a logic low on TXD and RXD. In recessive state, the bus is biased to $V_{CC}/2$ via high-resistance internal input resistors R_{IN}, corresponding to a logic high on TXD and RXD.

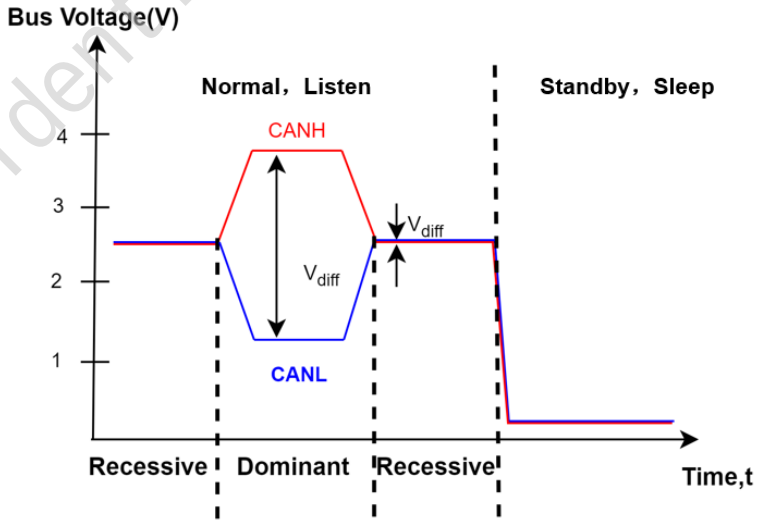


Figure 31.CAN Bus States

9.4.4 Driver and Receiver Function Tables

Table 4. Driver Function Table

Mode	TXD Input	Bus State
Normal	Low	Dominant
	H or Open	Recessive (VCC/2)
Listen	X	Recessive (VCC/2)
Standby	X	GND
Sleep	X	GND

Table 5. Receiver Function Table

Device Mode	Can Differential Inputs	Bus State	RXD Terminal
Normal/Listen	$V_{ID} \geq V_{IT+(MAX)}$	Dominant	Low
	$V_{IT-(MIN)} < V_{ID} < V_{IT+(MAX)}$	Indetermined	Indetermined
	$V_{ID} \leq V_{IT-(MIN)}$	Recessive	High
Standby/Sleep	$V_{ID} \geq V_{IT+(MAX)}$	Dominant	High Low if wake-up event persists
	$V_{IT-(MIN)} < V_{ID} < V_{IT+(MAX)}$	Indetermined	
	$V_{ID} \leq V_{IT-(MIN)}$	Recessive	

10 Application and Implementation

10.1 Application information

10.1.1 CAN Termination

MCAN1463B is typically used in the following network shown on Figure 32, and the bus termination should be placed on the two far end.

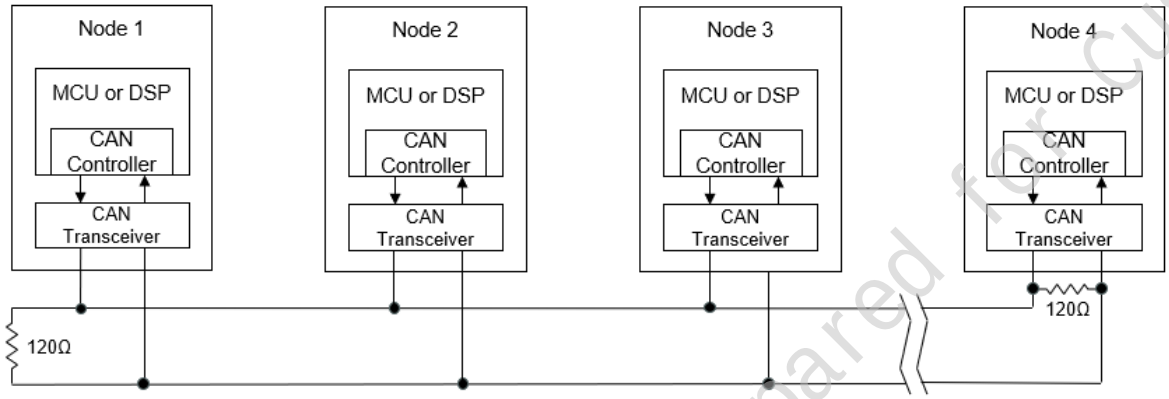


Figure 32. Typical CAN Bus

The characteristic impedance of the twisted pair cable is required to be equal to the characteristic impedance of the line. The terminated resistors need to place at the both end of the cable to prevent signal reflections. Stubs should be kept as short as possible to reduce unnecessary signal reflections. In order to keep common-mode voltage stable, especially in the high ambient temperature environment, split termination should be used.

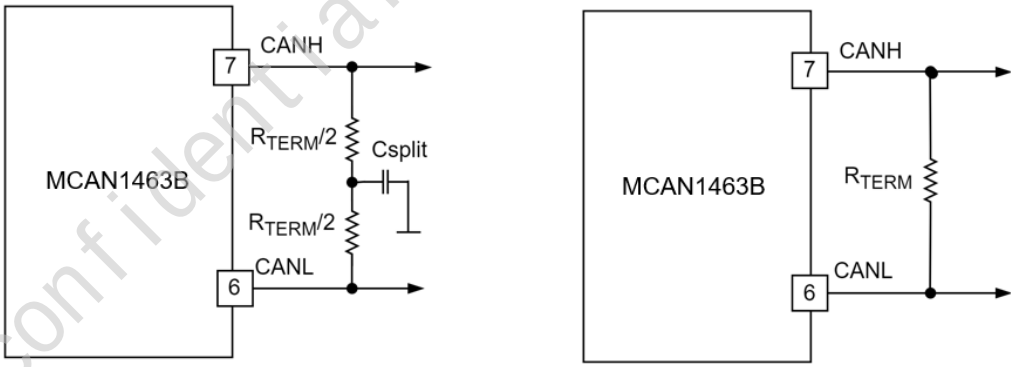


Figure 33. CAN Bus Termination Concepts

10.2 Typical Applications

The MCAN1463B transceiver is typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. These types of applications usually also include power management technology that allows for power to be gated to the application via an enable (EN) or inhibit (INH) pin. A single 5-V regulator can be used to drive both VCC and VIO, or independent 5V and 3.3V regulators can be used to drive V_{CC} and V_{IO} separately as shown in Figure 34 and Figure 35.

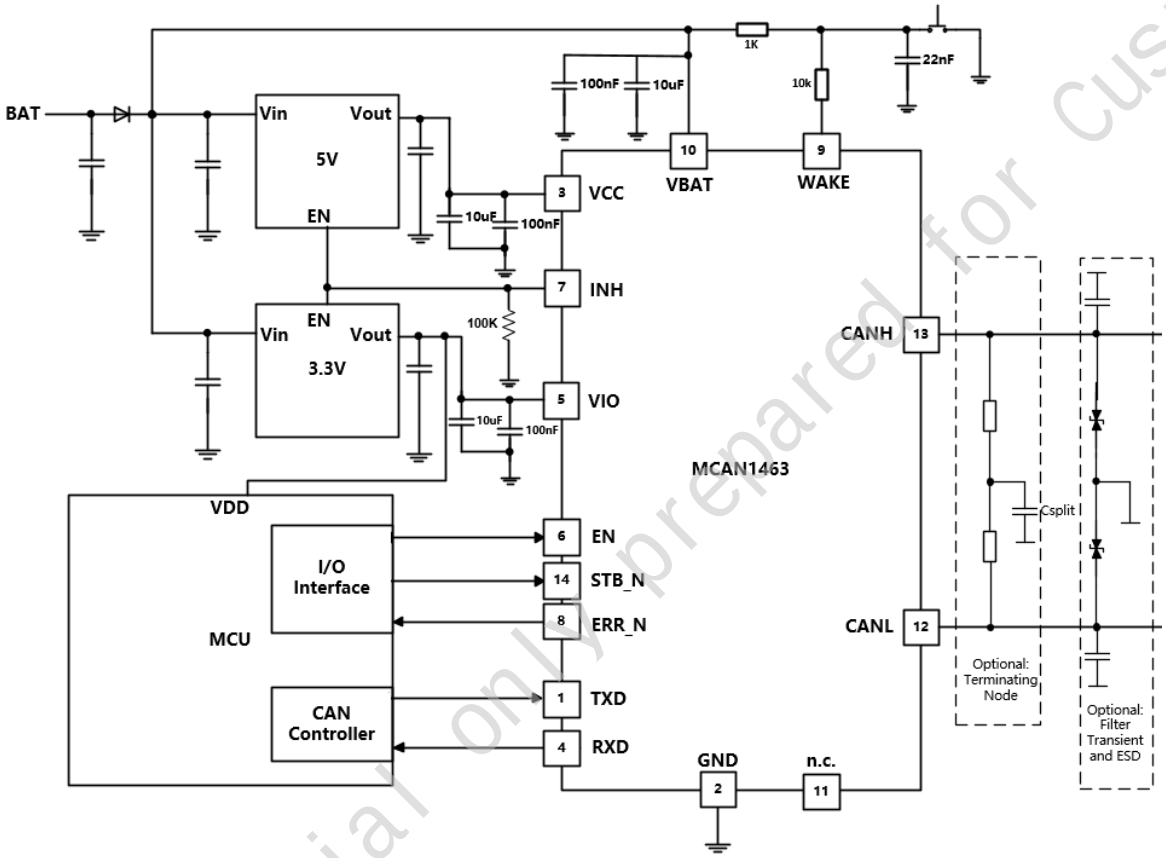


Figure 34. Typical CAN Bus Application with 3.3V MCU

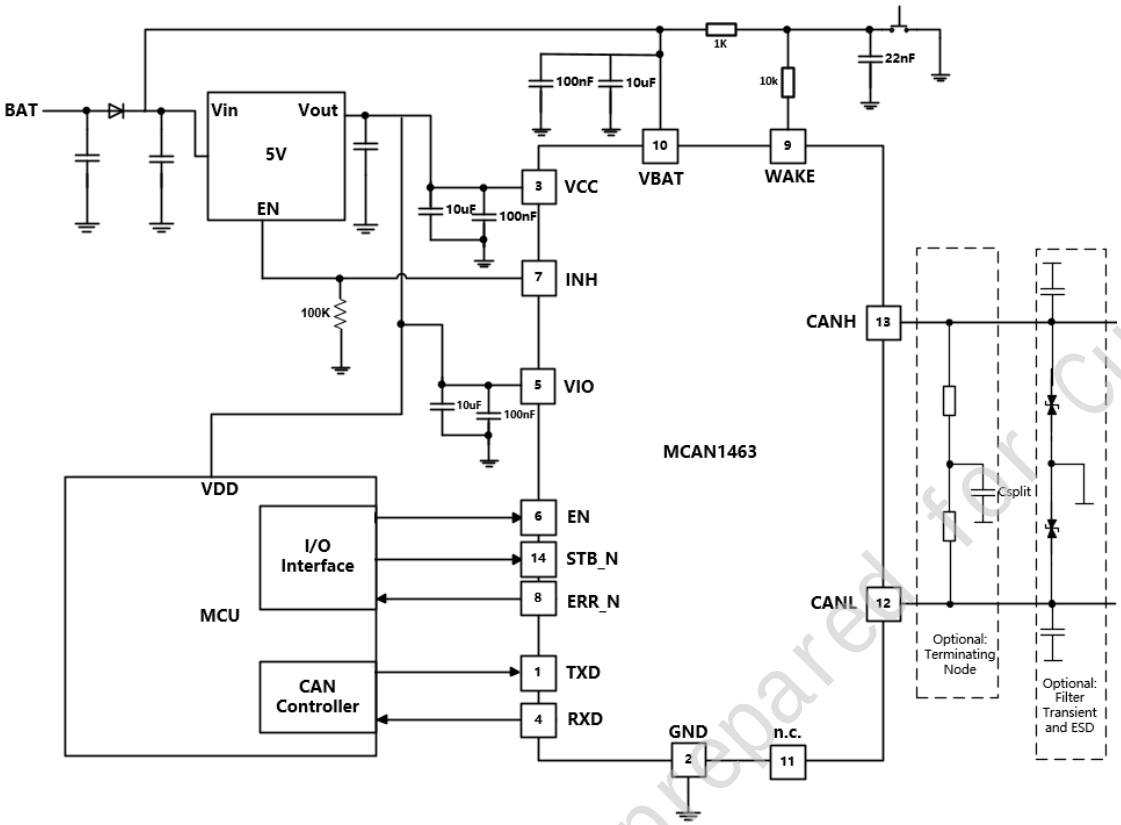


Figure 35. Typical CAN Bus Application with 5V MCU

11 Power Supply Recommendations

The MCAN1463B is designed to operate off of three supply rails; V_{BAT}, V_{CC}, and V_{IO}. V_{BAT} is a high-voltage supply pin designed to connect to the V_{BAT} rail, V_{CC} is a low-voltage supply pin with an input voltage range from 4.5 V to 5.5 V that supports the CAN transceiver and V_{IO} is a low-voltage supply pin with an input voltage range from 1.71 V to 5.5 V that provides the I/O voltage to match the system controller. For a reliable operation, a 100nF decoupling capacitor should be placed as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the output of switched-mode power supplies, and also helps to compensate for the resistance and inductance of the PCB power planes.

12 Layout

Reliable CAN bus design needs to use external transient protection device to protect the CAN device from suffering surge transients in the environment. Devices can deal with some ESD problems with the ESD protection inside. However, PCB design needs to consider higher levels of ESD immunity and external protection device such as TVS diodes needs to be used.

12.1 Layout Guidelines

(1) Place the protection circuitry as close to the bus connector, J1, to prevent transients, ESD from propagating onto the board.

(2) Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

(3) Bypass capacitors C1 and C2 on V_{CC}, C3 and C4, C5 and C6 on V_{BAT} should be placed as close as possible to the supply terminals

(4) Bus termination: This layout example shows split termination. Split termination is recommended to reduce common-mode EMI emission. This is where the termination is split into two resistors, R2 and R3, with the center or split tap of the termination connected to ground via capacitor C7.

12.2 Layout Example

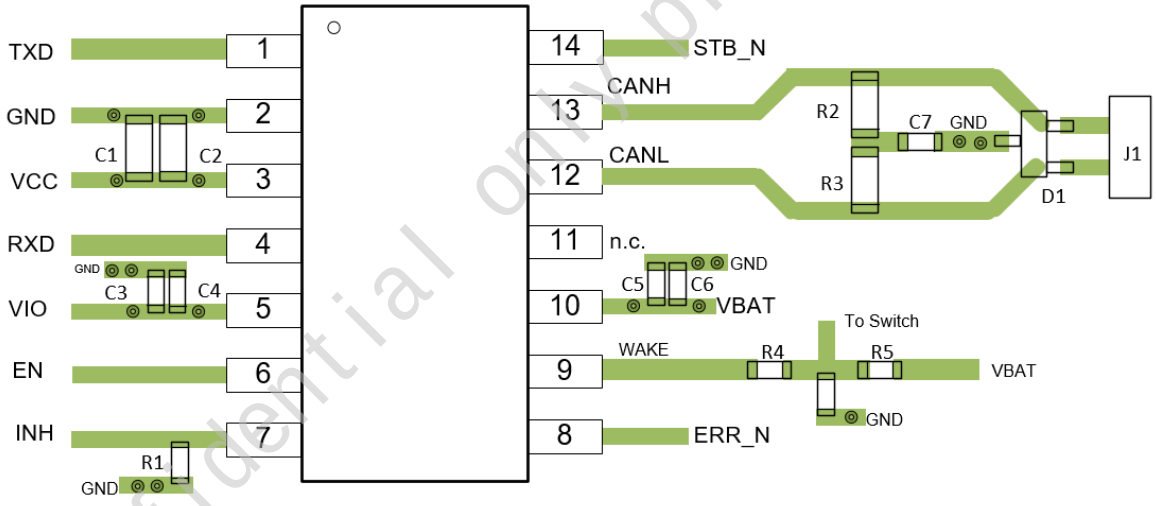


Figure 36. Layout Example

13 Receiving Notification of Documentation Updates

13.1 Device Support

13.2 Documentation Support

13.3 Receiving Notification of Documentation Updates

13.4 Support Resources

13.5 Trademarks

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14 Mechanical, Packaging

14.1 Package Size

14.1.1 SOP14

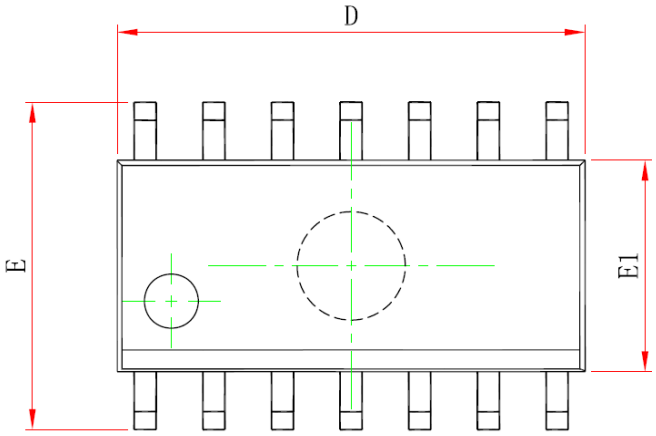


Figure 37. SOP14 Top View

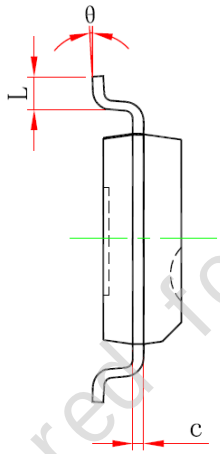


Figure 38. SOP14 Side View

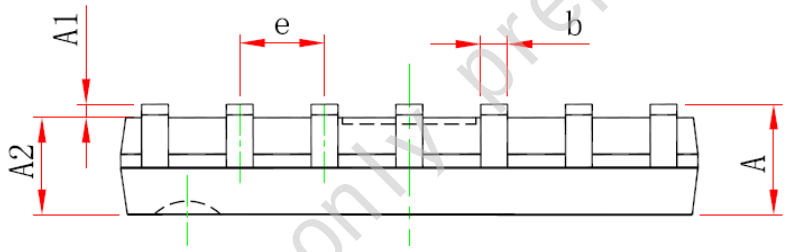


Figure 39. SOP14 Side View

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	1.40	1.50
b	0.31	-	0.51
c	0.10	-	0.25
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27(BSC)		
L	0.40	-	1.27
θ	0°	-	8°

14.1.2 DFN14

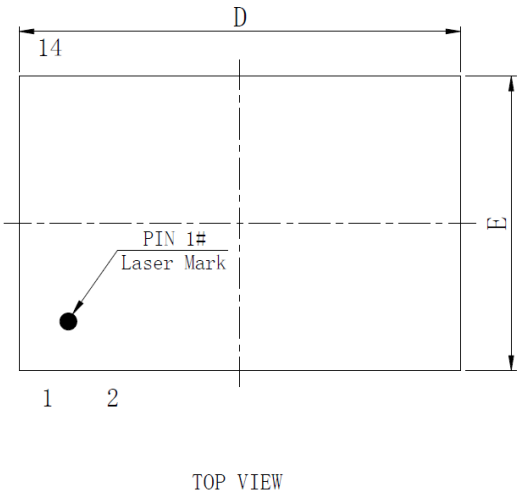


Figure 40. DFN14 Top View

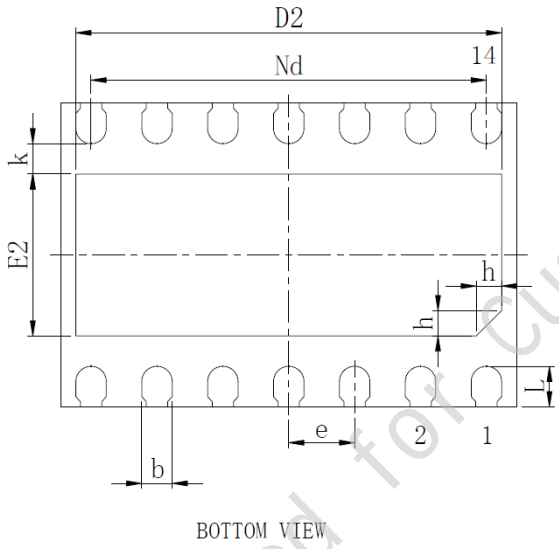


Figure 41 . DFN14 Bottom View

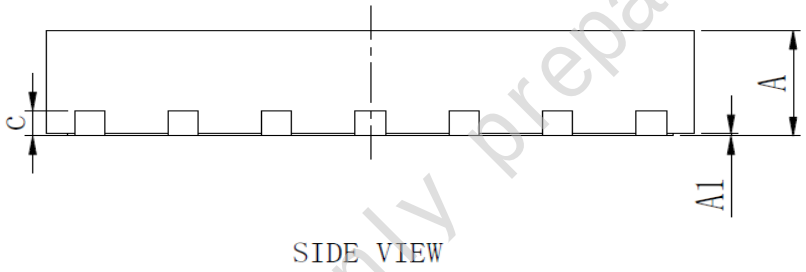


Figure 42. DFN14 Side View

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
c		0.203REF	
D	4.40	4.50	4.60
D2	4.10	4.20	4.30
e		0.65BSC	
Nd		3.90BSC	
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.35	0.40	0.45
h	0.20	0.25	0.30

14.2 Recommended Land Pattern

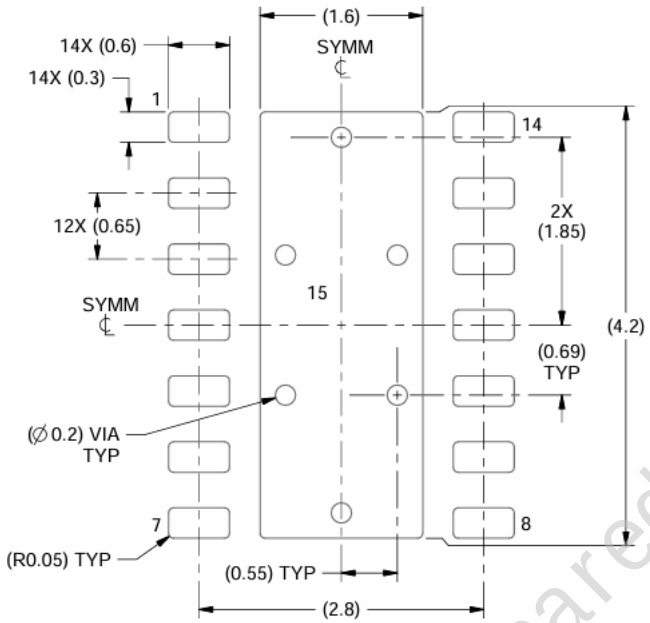


Figure 43. DFN14 Land Pattern

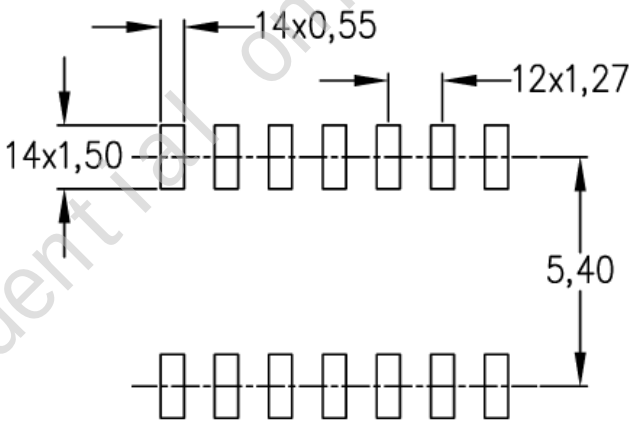


Figure 44. SOP14 Land Pattern

15 Reel and Tape Information

15.1 SOP14

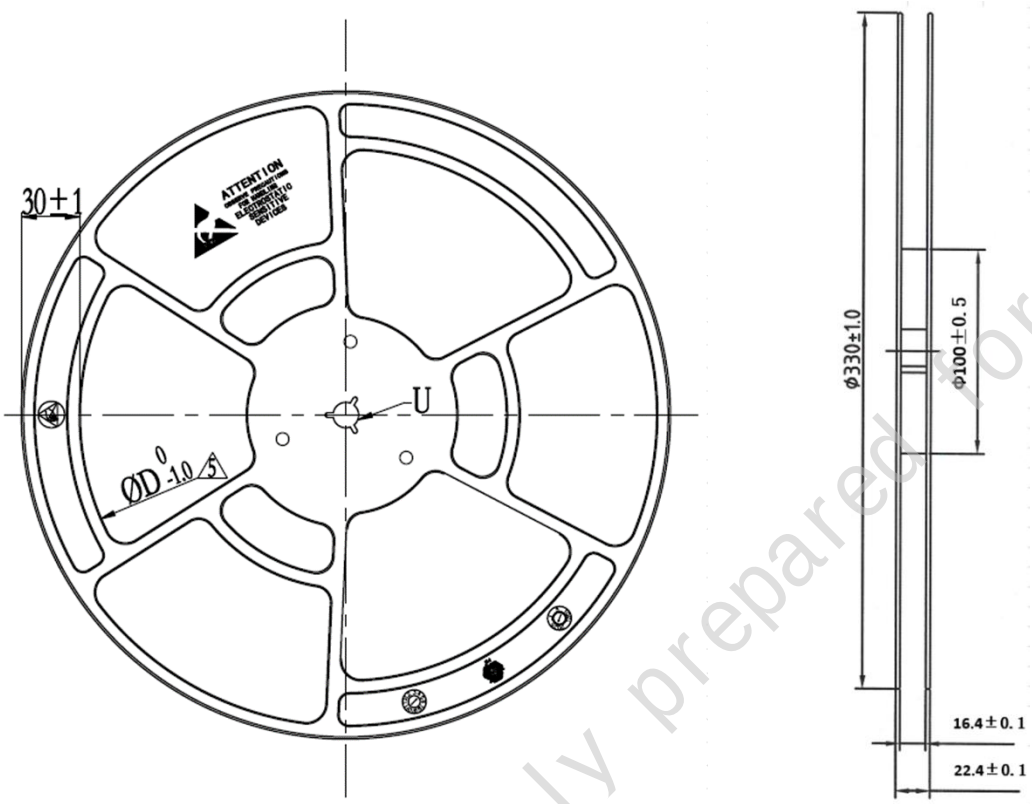
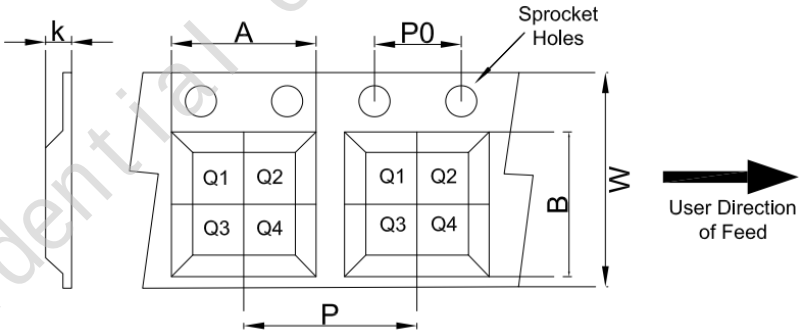


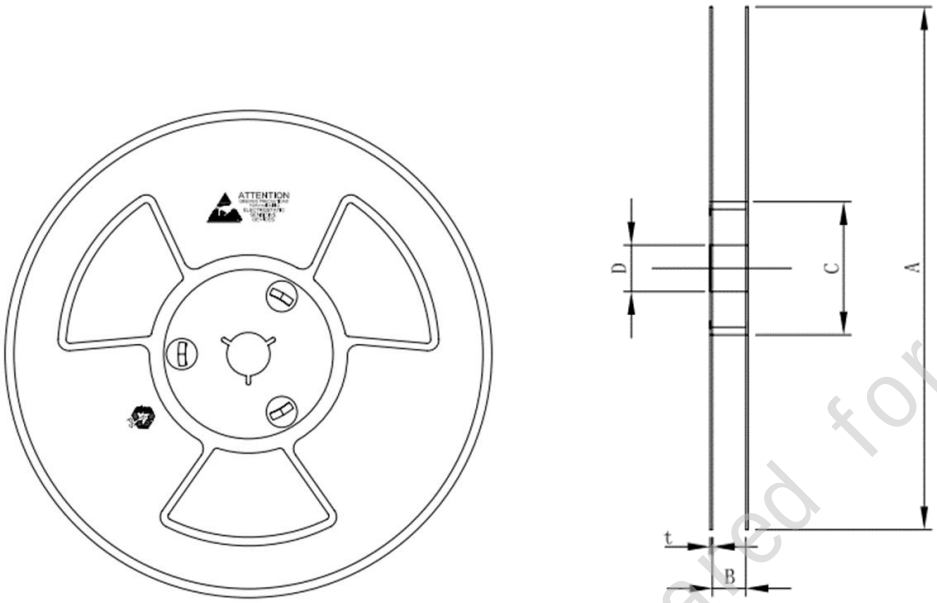
Figure 45. SOP14 Reel Dimensions



Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
MCAN1463BXAK-Q1	SOP14	14	4000	6.6±0.1	9.15±0.1	1.8±0.1	8±0.1	4±0.1	16±0.1	Q1

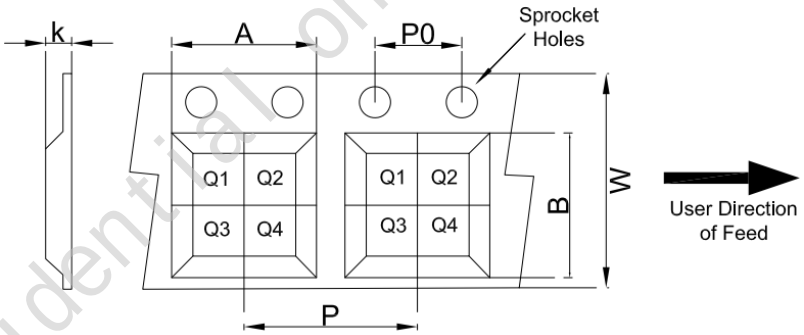
Figure 46. SOP14 Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

15.2 DFN14



Basic Dimension(mm)				
A	B	C	D	t
329±1	$12.4^{+2.0}_{-0.0}$	100±1	13.3±0.3	2.0±0.3

Figure 47. DFN14 Reel Dimensions

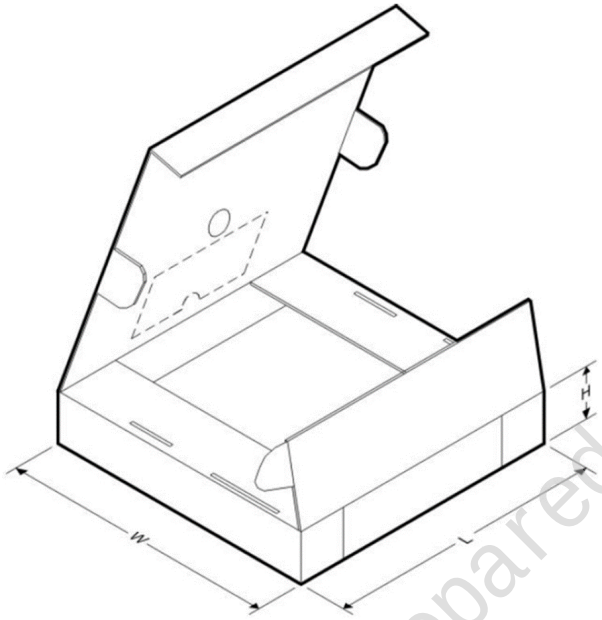


Device	Package Type	Pins	SPQ	A	B	K	P	P0	W	Pin1
			(pcs)	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	Quadrant
MCAN1463BXDH-Q1	DFN4.5x3-14L	14	3000	3.3±0.1	4.8±0.1	1.05±0.1	8.0±0.1	4.0±0.1	12.0±0.3	Q1

Figure 48. DFN14 Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

16 Tape and Reel Box Dimensions

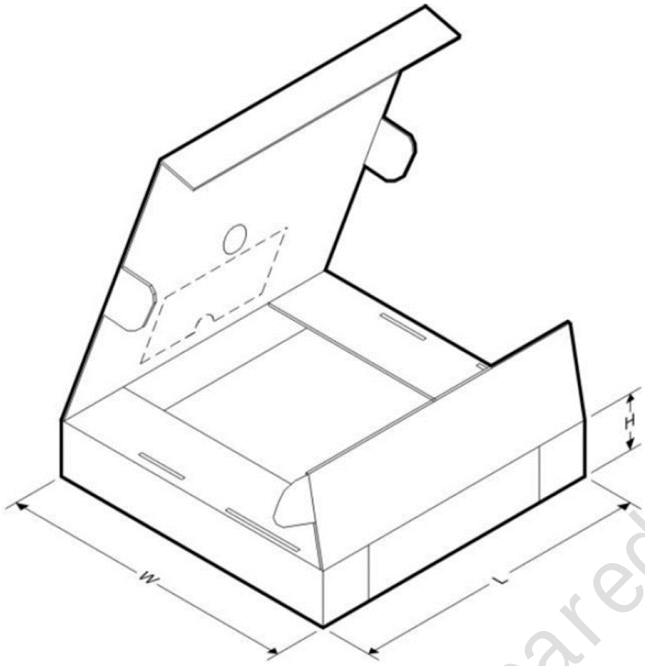
16.1 SOP14



Device	Package Type	Pins	SPQ	Length	Width	Height
			(pcs)	(mm)	(mm)	(mm)
MCAN1463BXAK-Q1	SOP14	14	8000	360	360	65

Figure 49. SOP14 Box Dimensions

16.2 DFN14



Device	Package Type	Pins	SPQ	Length	Width	Height
			(pcs)	(mm)	(mm)	(mm)
MCAN1463BXDH-Q1	DFN4.5x3-14L	14	3000	360	360	65

Figure 50. DFN14 Box Dimensions