High-Voltage Half-Bridge Resonant Controller

1. Descriptions

The MK2199 family are primary-side voltage-mode controllers specialized for resonant half-bridge topologies. They can be paired with synchronous rectification (SR) controller MK162X to achieve high-efficiency and reliable converter designs.

The IC features an optimized oscillator, allowing users to set the operating frequency range accurately via externally programmable components (e.g., resistors and capacitors).

MK2199 and MK2199L feature a fixed dead-time between the turn-off of one switch and the turn-on of the other. While MK2199D's dead-time can be configured through an external resistor, which guarantees soft-switching and enables high-frequency operation.

In order to optimize the startup current stress at start-up, MK2199 and MK2199D add a bootstrap capacitor pre-charging function, and reset the resonant tank current. However, MK2199L does not have these features.

In terms of overcurrent and short-circuit protection, the MK2199 and MK2199D can use the DELAY pin to set the restart time instead of latch-off protection. MK2199L provides overcurrent latch-off protection as needed.

Other functions include an additional protected input (DIS) allowing easy implementation of OTP or OVP, burst-mode operation, PFC stop function and brownout protection.

2. Applications

- AC/DC adapter
- High-Power density DC/DC
- Datacenter and telecom
- LCD and PDP TV

3. Features

- Wide VCC voltage ranges up to 26V max
- Adjustable dead time from 250ns to 1us (MK2199D)
- 50% duty cycle, variable frequency control of resonant half-bridge
- Two-level OCP: frequency-shift and auto-restart (MK2199 and MK2199D)
- Two-level OCP: frequency-shift and latched shutdown (MK2199L)
- High-accuracy oscillator up to 500kHz
- Burst mode operation at light load
- 3.3A source and 4A sink capability for both high-side and low-side gate drivers
- Bootstrap capacitor pre-charging (MK2199 and MK2199D)
- Input for power ON/OFF sequencing or brownout protection
- Safe-start procedure prevents hard switching at startup (MK2199 and MK2199D)
- 600V compatible high-side gate driver and high dv/dt immunity
- SOP-16 package

4. Typical Application

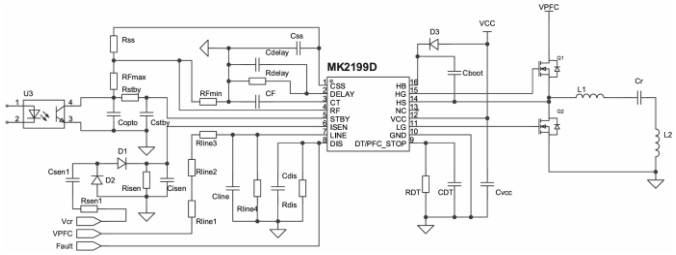

Figure 1. MK2199D Typical Application Diagram

5. Order Information

Order Part Number	Description
MK2199XAC	SOP-16, tape, 3000 pcs/reel
MK2199DXAC	SOP-16, tape, 3000 pcs/reel
MK2199LXAC	SOP-16, tape, 3000 pcs/reel

6. Pin Configuration and Functions

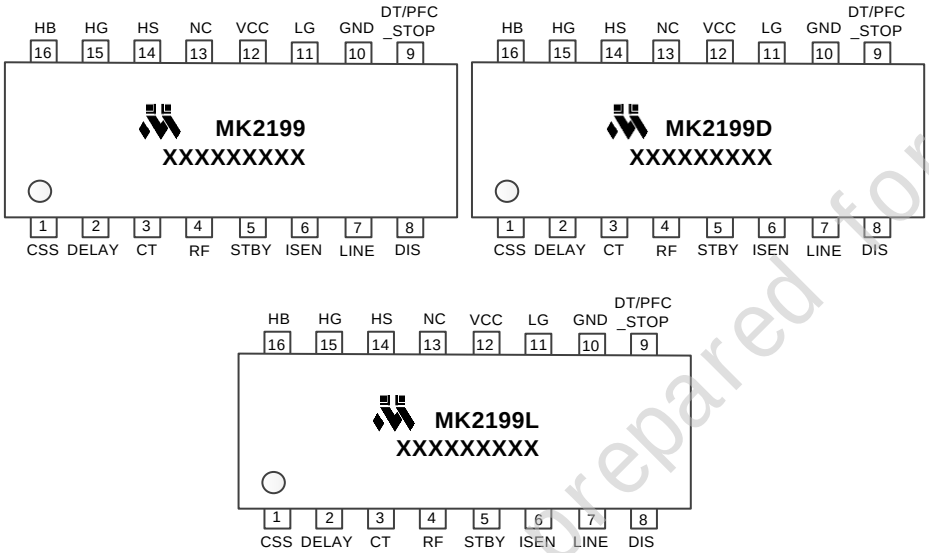

Figure 2. Pin Connection (Top View)

Table 1. Pin Functions

Pin NO.	Name	Function	Descriptions
1	CSS	Soft start	This pin connects an external capacitor to GND and a resistor to RF (pin 4) to set both the maximum oscillator frequency and the time constant for the frequency shift that occurs as the chip starts up (soft-start). An internal switch discharges this capacitor every time the chip turns off (VCC < VCC_{OFF}, LINE < V_{LINETH} or > $V_{LINECLAMP}$, DIS > V_{DISTH}, ISEN > $V_{ISENDIS}$, DELAY > $V_{DELYTH1}$) to make sure it is soft-started next time.
2	DELAY	Delayed shutdown	A capacitor and a resistor are connected from this pin to GND to set the maximum duration of an overcurrent condition before the IC stops switching and the delay after which the IC restarts switching.
53	CT	Timing capacitor	A capacitor connected from this pin to GND is charged and discharged by internal current generators programmed by the external network connected to pin 4 (RF) to determine the switching frequency of the converter.
4	RF	Minimum oscillator frequency setting	This pin provides a precise reference, and a resistor connected from this pin to GND defines a current that is used to set the minimum oscillator frequency.
5	STBY	Burst mode	The pin senses the voltage related to the feedback control, which is compared to an internal reference. If the

			voltage on the pin is lower than the reference, the IC enters an idle state. Tie the pin to RF if burst mode is not used.
6	ISEN	Current sense input	The pin senses the primary current though a sense resistor or a capacitive divider for lossless sensing. This input is not intended for a cycle-by-cycle current control. Therefore, the voltage signal must be filtered to get average current information.
7	LINE	Line sensing input	The pin is to be connected to the high-voltage input bus with a resistor divider to perform either AC or DC (in systems with PFC) brownout protection.
8	DIS	Disable protection	With an internal comparator, when the voltage on this pin exceeds the threshold, the IC is shut down and brings its consumption almost to a “before startup” level. Tie the pin to GND if the function is not used.
9	DT/PFC_STOP	Dead time program and PFC controller	This pin, normally open, is intended for stopping the PFC controller for protection purposes or during burst mode operation. Leave this pin unconnected if not used. For the MK2199D, it can also be used to program dead time.
10	GND	Chip ground	Common ground connection for sensing networks and driver outputs.
11	LG	Low side driver	Low-side gate driver output.
12	VCC	Supplies the controller	This supply pin accepts up to 26Vdc max. The pin is connected to an external auxiliary supply.
13	NC	High-voltage spacer	The pin is not internally connected to isolate the high-voltage pin and ease compliance with safety regulations (creepage distance) on the PCB.
14	HS	Midpoint	The midpoint of the half-bridge and HG’s floating ground. Current return of HG current.
15	HG	High side driver	High-side gate driver output.
16	HB	HG power supply	HG power supply with the bootstrap capacitor connected between this pin and pin 14 (HS). It is fed by an external bootstrap diode driven in-phase with the low-side gate driver.

7. Specifications

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	Supply voltage VCC	-0.3	26	V
DT/PFC_STOP	DT/ PFC_STOP to GND	-0.3	26	
LG (2)	LG to GND	-0.3	26	
HG (2)	Voltage on HG	V_{HS} - 0.3	V_{HB} + 0.3	
HB	HB to GND	-0.3	626	
HS	Voltage on HS	V_{HB} - 25	V_{HB} + 0.3	
CSS, DELAY, RF, CT, ISEN, STBY, DIS (2)	Analog inputs and outputs	-0.3	6	
LINE	Maximum voltage of LINE pin (I_{LINE} ≤ 1 mA)	-	Self-limited	V
I_{RF}	Maximum source current of RF	0	3	mA
d_{HS}/d_t	Maximum voltage slew rate of HS	-	50	V/ns
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	
T_{sld}	Soldering temperature (10 second)		260	

Notes:

(1) Stresses beyond the “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in “RECOMMENED OPERATING CONDITIONS”. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Output pin not to be voltage driven.

7.2 ESD Ratings

		Value	Unit
Electrostatic Discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±2000	V

Notes:
(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

7.3 Moisture Sensitivity Level

Moisture Sensitivity Level	SOP-16	MSL3

7.4 Recommended Operating Conditions

		Min	Max	Unit
Recommended Operation Conditions	VCC Voltage	9	24	V
	DIS Voltage	-0.3	3.3	
	LINE Voltage	-0.3	5	
	I_{RF} Current	0	2	mA
	I_{CT} Current	0	2	
	Operating Junction Temperature	-40	+125	°C

7.5 Thermal Information

		Value	Unit
Package Thermal Resistance	θ_{JA} (Junction to ambient)	85	°C/W
	θ_{JC} (Junction to case)	28	°C/W

Note:
(1) Measured on 2s2p PCB of JEDEC

7.6 Electrical Characteristics

T_J = -40 to 125 °C, VCC = 15 V, C_{HG} = C_{LG} = 1 nF, C_{CT} = 470 pF, R_{RF} = 12 kΩ, 1 µF from VCC to GND. All voltages are measured with respect to ground (pin 10). Currents are positive when flowing into the IC, unless otherwise specified.

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
IC Supply Voltage						
VCC	Operating range	After device turn-on	9	-	26	V
VCC_{ON}	Turn-on threshold	Voltage rising @ -40~125 ℃	10	10.3	10.6	V
		Voltage rising @25 ℃	10.1	10.3	10.5	V
VCC_{OFF}	Turn-off threshold	Voltage falling @ -40~125 ℃	8	8.3	8.6	V
		Voltage falling @25 ℃	8.1	8.3	8.5	V
VCC_{HYS}	Hysteresis (1)	-	-	1.9	-	V
High-Side Floating Gate-Drive Supply						
I_{LKHB}	HB pin leakage current	V_{HB} = 600 V	-	-	10	µA
I_{LKHS}	HS pin leakage current	V_{HS} = 600 V	-	-	10	µA
Supply Current						
$I_{STARTUP}$	Start-up current	Before device turn-on VCC = 9 V	-	200	275	µA
		Before device turn-on VCC = 9 V @25 ℃	-	200	250	
I_Q	Quiescent current	Device on, V_{STBY} = 1 V	-	1	1.2	mA
I_{OP}	Operating current	Device on, V_{STBY} = V_{RF}	-	2.8	3.2	mA
I_{RC}	Residual consumption	V_{DIS} > V_{DISTH} or V_{DELAY} > $V_{DELAYTH2}$ or V_{LINE} < V_{LINETH} or V_{LINE} = V_{CLAMP}	-	540	630	µA
Overcurrent Comparator						
$I_{ISENBIAS}$	Input bias current	V_{ISEN} = 2 V	-	-	1	µA
T_{LEB}	Leading edge blanking (1)	After V_{HG} and V_{LG} low-to-high transition	-	280	-	ns
V_{ISEN}	Frequency shift threshold	Voltage rising	0.77	0.8	0.84	V

$V_{ISENHYS}$	Hysteresis (1)	Voltage falling	-	50	-	mV
$V_{ISENDIS}$	Restart/latch threshold	Voltage rising	1.46	1.51	1.56	V
Line Sensing						
V_{LINETH}	Threshold voltage	Voltage rising or falling	1.22	1.25	1.3	V
$I_{LINEHYS}$	Current hysteresis	V_{LINE} = 0.3 V	12	15	18	µA
$V_{LINECLAMP}$	Clamp level	I_{LINE} = 1 mA	6.6	-	7.2	V
DIS Function						
$I_{DISBIAS}$	Input bias current	V_{DIS} = 0 to 3 V	-1	-	1	µA
V_{DISTH}	Disable threshold	Voltage rising	1.75	1.8	1.88	V
Oscillator						
T_{ON}	LG/HG on time	R_{RF} = 10 kΩ C_{CT} = 470 pF	4.46	4.6	4.71	µs
F_{OSC}	Oscillation frequency (1)	1 / (2 * T_{ON} + 2 * TD)	97.8	100	104	kHz
		Maximum recommended	-	-	500	kHz
TD	Deadtime	Between HG and LG	0.35	0.38	0.4	µs
V_{CFP}	Peak value (1)	-	-	3	-	V
V_{CFV}	Valley value (1)	-	-	0.01	-	V
V_{REF}	Voltage reference at pin 4	-	1.94	2	2.06	V
T_{ONMAX}	Max on time (1)	MK2199 only	-	14	-	µs
DT/PFC_STOP Function						
$I_{PFCSTOPLEAK}$	High level leakage current	V_{PFC_STOP} = VCC, V_{DIS} = 0 V	-1	-	1	µA
R_{PFC_STOP}	ON-state resistance (1)	I_{PFC_STOP} = 1 mA, V_{DIS} = 1.5 V	-	130	-	Ω
$V_{LPFCSTOP}$	Low saturation level	V_{DIS} = 2 V	-	-	0.2	V
DT_{ADJ}	Adjustable dead time (1)	R_{DT} = 20 kΩ MK2199D only	-	350	-	ns
		R_{DT} = 0 Ω MK2199D only	-	1000	-	
Soft-Start Function						
$I_{CSSLEAK}$	Open-state current	V_{CSS} = 2 V	-	-	0.5	µA
R_{CSS}	Discharge resistance	V_{ISEN} = 1 V	-	130	187	Ω
Standby Function						
$I_{STBYBIAS}$	Input bias current	V_{DIS} = 0 to 2 V	-	-	1	µA
$V_{STBYDIS}$	Disable threshold	Voltage falling	1.21	1.25	1.28	V

$V_{STBYHYS}$	Hysteresis (1)	Voltage rising	-	50	-	mV
Delayed Shutdown Function						
$I_{DELYLEAK}$	Open-state current	V_{DELAY} = 0 V	-	-	0.5	µA
$I_{DELYCHARGE}$	Charge current	V_{DELAY} = 1 V V_{ISEN} = 1 V	105	144	185	µA
$V_{DELYTH1}$	Threshold for forced operation at max frequency	Voltage rising	1.95	2.00	2.07	V
$V_{DELYTH2}$	Shutdown threshold	Voltage rising	3.35	3.5	3.65	V
$V_{DELYTH3}$	Restart threshold	Voltage rising	0.29	0.31	0.33	V
Low-Side Gate Driver (Voltages Referred to GND)						
V_{LGL}	Output low voltage	I_{SINK} = 200 mA	-	-	1.5	V
V_{LGH}	Output high voltage	VCC = 15 V	14.8	15	15.2	V
$I_{SOURCEPKLG}$	Peak source current (1)	-	-	-	3.3	A
$I_{SINKPKLG}$	Peak sink current (1)	-	-	-	4	A
T_{LGTF}	LG fall time	C_{LOAD} = 1 nF	-	18	-	ns
T_{LGTR}	LG rise time	C_{LOAD} = 1 nF	-	20	-	ns
High-Side Gate Driver (Voltages Referred to HS)						
V_{HGL}	Output low voltage	I_{SINK} = 200 mA	-	-	1.5	V
V_{HGH}	Output high voltage	VCC = 15 V	14.8	15	15.2	V
$I_{SOURCEPKHG}$	Peak source current (1)	-	-	-	3.3	A
$I_{SINKPKHG}$	Peak sink current (1)	-	-	-	4	A
T_{HGTF}	HG fall time	C_{LOAD} = 1 nF	-	18	-	ns
T_{HGTR}	HG rise time	C_{LOAD} = 1 nF	-	20	-	ns

Notes:

(1) Values are guaranteed by design and verified by characterization on bench, not tested in production.

7.7 Typical Characteristics

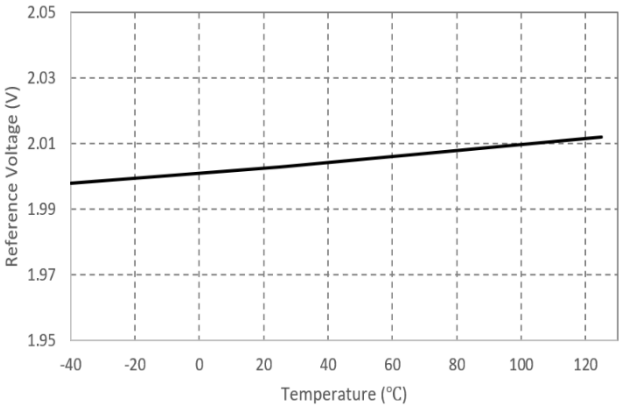

Figure 3. Reference voltage vs temperature

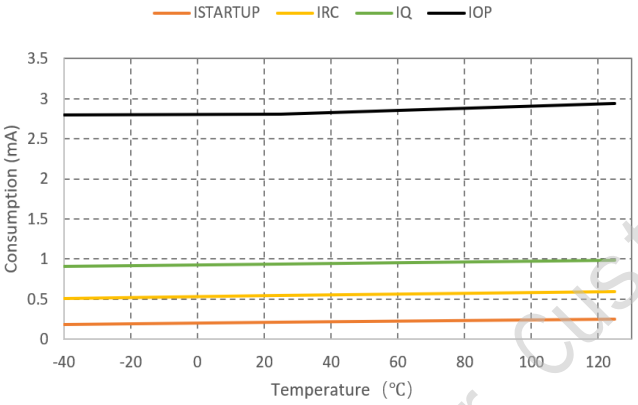

Figure 4. IC consumption vs temperature

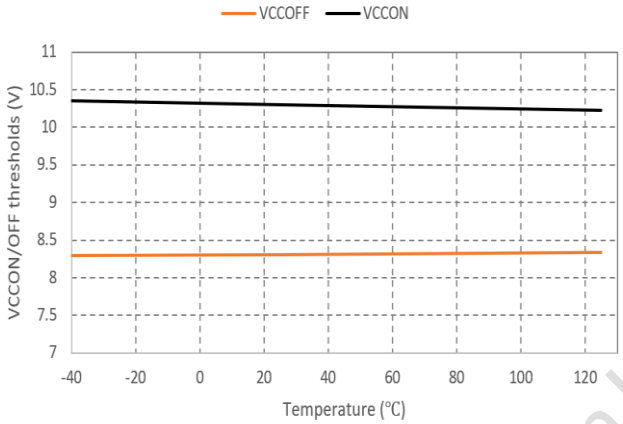

Figure 5. VCC$_{ON/OFF}$ thresholds vs temperature

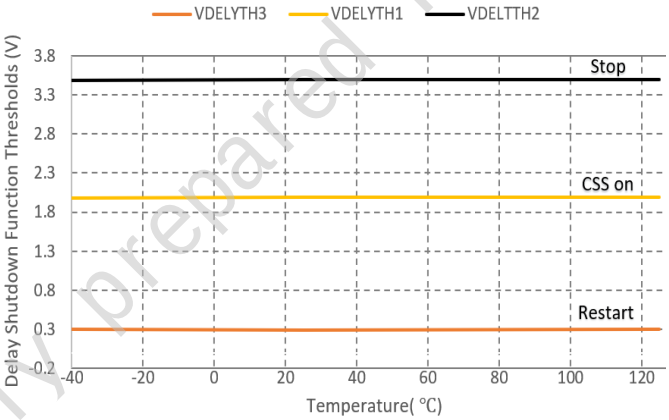

Figure 6. Delay shutdown function thresholds vs temperature

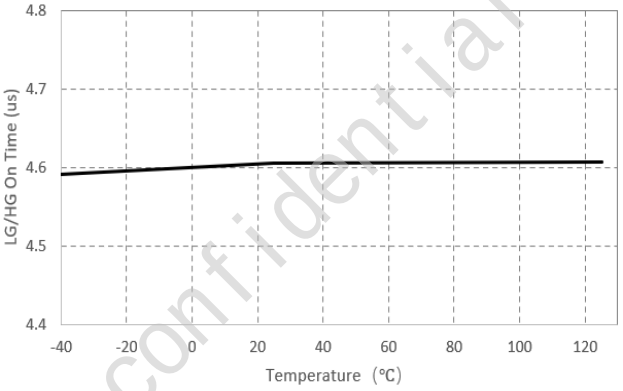

Figure 7. LG/HG on time vs temperature

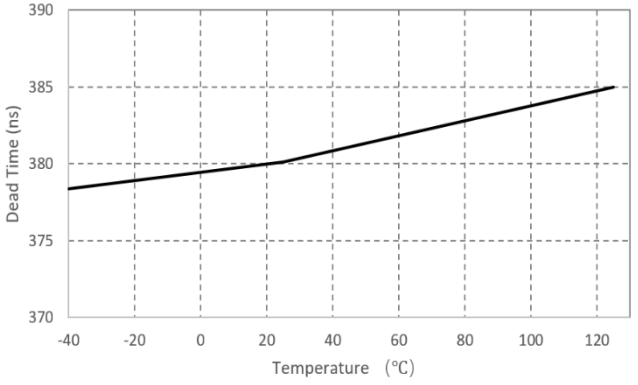

Figure 8. Dead time vs temperature

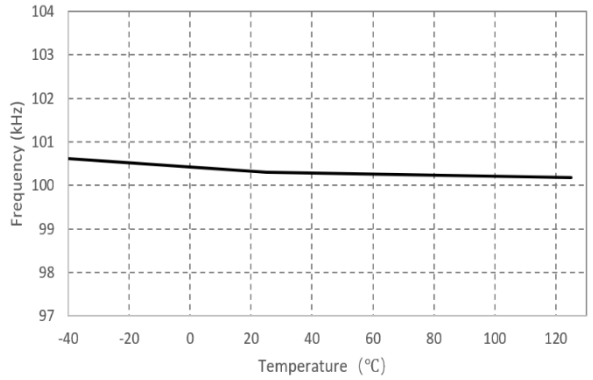

Figure 9. Frequency vs temperature

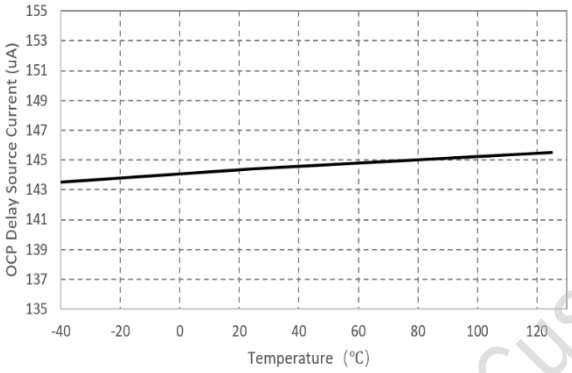

Figure 10. OCP delay source current vs temperature

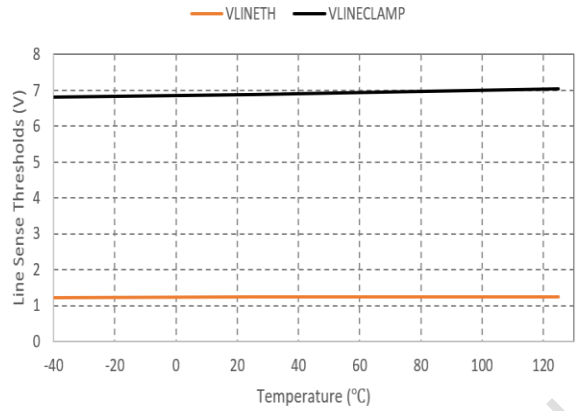

Figure 11. Line sense thresholds vs temperature

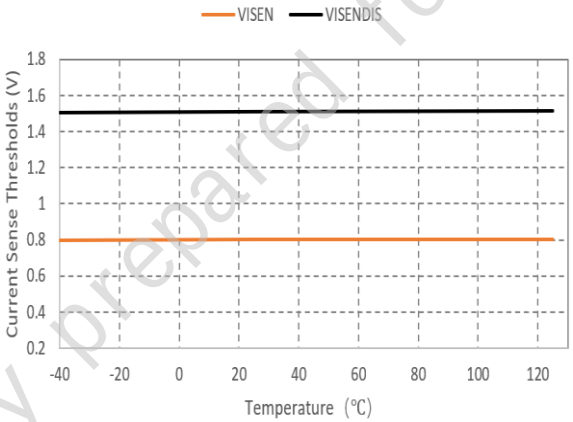

Figure 12. Current sense thresholds vs temperature

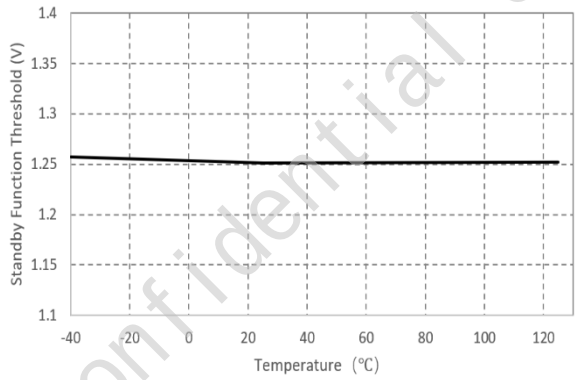

Figure 13. Standby function threshold vs temperature

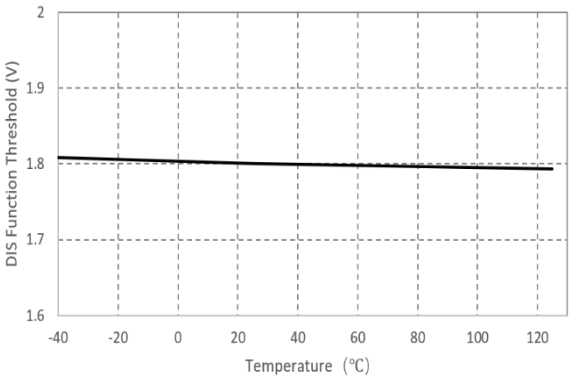

Figure 14. DIS function threshold vs temperature

8. Detailed Description

8.1 Overview

The MK2199 family are primary-side voltage-mode controllers specialized for resonant half-bridge topologies. They can be paired with synchronous rectification (SR) controller MK162X to achieve high-efficiency and reliable converter designs.

The IC optimizes the oscillator, and users can set the precise operating frequency range of the converter using an externally programmable component.

MK2199 and MK2199L feature a fixed dead-time between the turn-off of one switch and the turn-on of the other. While MK2199D's dead-time can be configured through an external resistor, which guarantees soft-switching and enables high-frequency operation.

In order to optimize the startup current stress at start-up, MK2199 and MK2199D add a bootstrap capacitor pre-charging function, and reset the resonant tank current. However, MK2199L does not have these features.

In terms of overcurrent and short-circuit protection, the MK2199 and MK2199D can use the DELAY pin to set the restart time instead of latch-off protection. MK2199L provides overcurrent latch-off protection as needed.

Other functions include an additional protected input (DIS) allowing easy implementation of OTP or OVP, burst-mode operation, PFC stop function and brownout protection.

The MK2199, MK2199D, and MK2199L can be selected based on application requirements. Table 2 compares these devices, which lists parameters that may affect external component values.

Table 2. MK2199 and MK2199D vs MK2199L

Parameter	MK2199L	MK2199	MK2199D
Fault protection: latched shutdown or auto-restart	Latched shutdown	Auto-restart	Auto-restart
Bootstrap capacitor pre-charging	No	Available	Available
Safe-start procedure prevents hard switching at startup	No	Available	Available
Adjustable dead time	No	No	Available
Enable Maximum ON time (RF pin > 2 V, T_{ONMAX} = 14 us)	No	Available	No

8.2 Functional Block Diagram

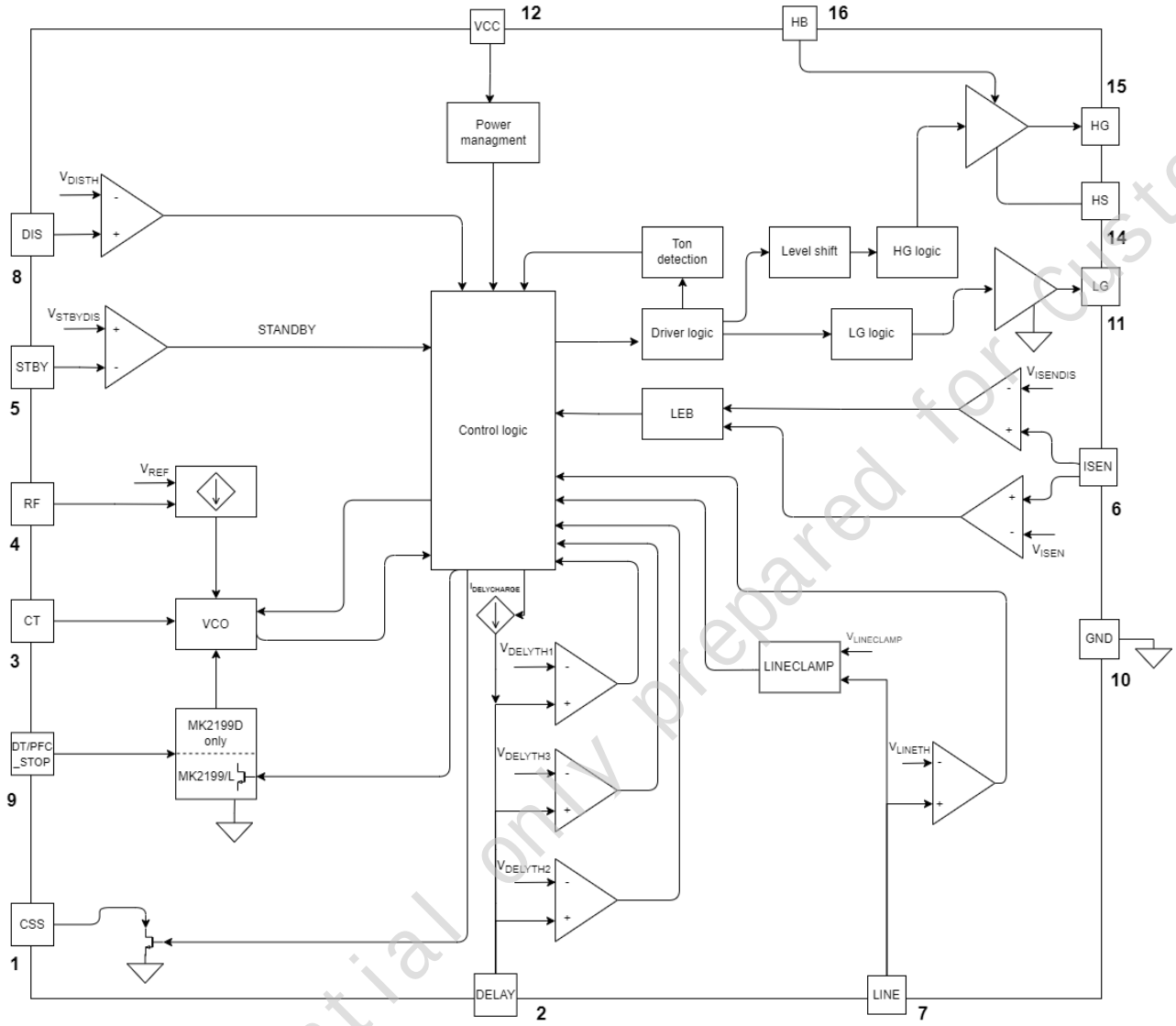

Figure 15. Block Diagram

8.3 Feature Description

8.3.1 VCC Power Supply and Undervoltage Lockout (UVLO)

The VCC operation voltage ranges from 9V to 24V, making it suitable for various applications. For the best performance, place a typical 0.1uF decoupling capacitor as close as possible between the VCC and GND pins, and add a 1uF to 10uF bypass capacitor in parallel to reduce switching noise.

MK2199 has an internal undervoltage lockout (UVLO) protection feature in the VCC supply circuit blocks. When the voltage on the VCC pin exceeds VCC_{ON}, the controller exits the UVLO state and activates the circuitry. When VCC voltage drops to below VCC_{OFF}, the controller re-enters the UVLO state.

The VCC power supply voltage of MK2199 can support up to 24V, and the driver output voltage is approximately equal to the VCC voltage. To avoid damaging power MOSFETs, the maximum VCC voltage of MK2199 needs to be carefully considered.

8.3.2 Soft-Start

Soft-start avoids excessive inrush current during start-up by progressively increasing the converter's power capability. In resonant converters, the deliverable power depends inversely on frequency, so the soft- start is done by sweeping the operating frequency from an initial high value until the control loop takes over. The soft-startup of MK2199 is simply realized with the addition of an R-C series circuit from pin 4 (RF) to ground, as shown in Figure 16.

Initially, the capacitor C_{SS} is totally discharged, so that the series resistor R_{SS} is effectively in parallel to RF_{min} and the resulting initial frequency is determined by R_{SS} and RF_{min} only, since the optocoupler's phototransistor is cut off (as long as the output voltage is not too far away from the regulated value). The following formula can help calculate start-up frequency:

$$f_{start} = \frac{1}{3 * CF * (RFmin||Rss)}$$

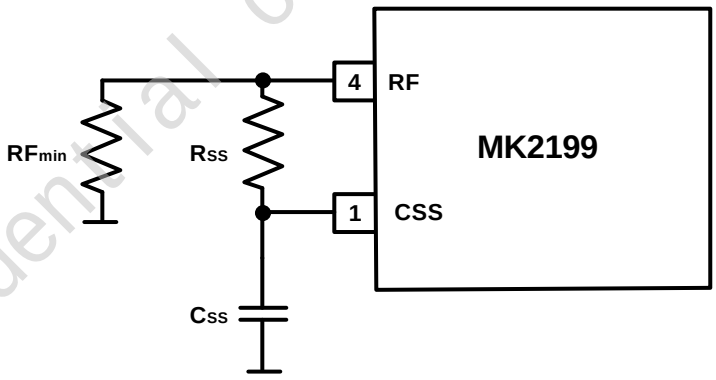

Figure 16. Soft-Start Circuit

The C_{SS} capacitor charges progressively until it reaches the reference voltage, consequently, the current through R_{SS} goes to zero. This conventionally takes 5 times the R_{SS}·C_{SS} time constant. Once the output voltage gets close to the regulated value, the feedback loop takes over, and the operating frequency is determined by the optocoupler's phototransistor.

During this frequency sweep phase, the operating frequency decays with the exponential charging of C_{SS}. Initially, the frequency changes relatively quickly, but the rate of change becomes slower as the process proceeds. This counteracts the tank circuit's non-linear frequency dependence, which causes the converter's power capability to change slightly when the frequency is far from resonance but rapidly as it

approaches the resonant frequency.

In order to further reduce the start-up current stress, MK2199 and MK2199D have optimized the turn-on pulses. First, the low-side gate driver is turned on with a wider pulse in order to pre-charge the bootstrap capacitor to a voltage exceeding the HB UVLO threshold and reset the resonant tank current. Subsequently, a normal dedicated startup sequence is applied to reduce the start-up stress. The specific control strategy and measured waveforms are shown in Figure 17. If a system cannot accept pre-charging feature, where LG's first pulse lasts too long without HG being turned on, the MK2199L can be used.

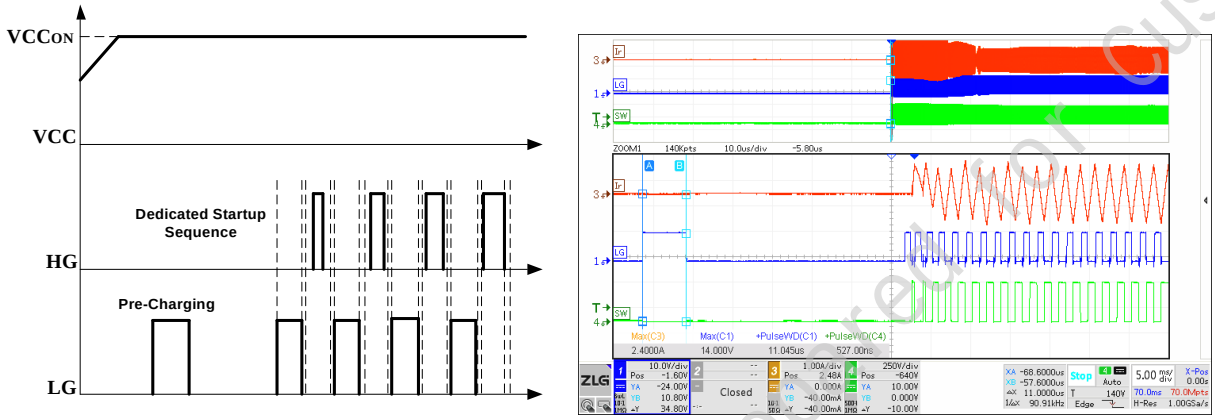

Figure 17. Dedicated Startup Sequence Detail

8.3.3 Line Sensing Function

This function essentially stops the IC as the converter's input voltage falls below the specified range, and triggers a restart as the voltage returns within range. The sensed voltage can be either the rectified and filtered mains voltage, in which case the function acts as a brownout protection, or in systems with a PFC pre-regulator front-end, the output voltage of the PFC stage, in which case the function serves as power-on/power-off sequencing.

The MK2199 is turned off with an internal comparator if the non-inverting input at Pin 7 (LINE) is below undervoltage threshold V_{LINETH}, as shown in Figure 18. Under this condition, the soft start is prohibited, the DT/PFC_STOP end is open, and the IC power consumption is reduced. The MK2199 is re-enabled if the voltage at LINE is higher than V_{LINETH} with the hysteresis set by internal current $I_{LINEHYS}$. The internal current $I_{LINEHYS}$ is active when the voltage at the LINE is below the threshold V_{LINETH}, and is shut down when the LINE voltage is above the threshold.

This approach provides flexible choices of ON/OFF thresholds and hysteresis with single external resistor divider. The following relationship can estimate the R_H and R_L:

$$R_H = \frac{V_{INON} - V_{INOFF}}{I_{LINEHYS}}$$

$$R_L = R_H \frac{V_{LINETH}}{V_{INOFF} - V_{LINETH}}$$

This approach provides an additional degree of freedom; it is possible to set the ON threshold and the OFF threshold separately by properly choosing the resistors of the external divider (as shown in Figure 18). With voltage hysteresis, fixing one threshold automatically fixes the other one depending on the built-in hysteresis of the comparator.

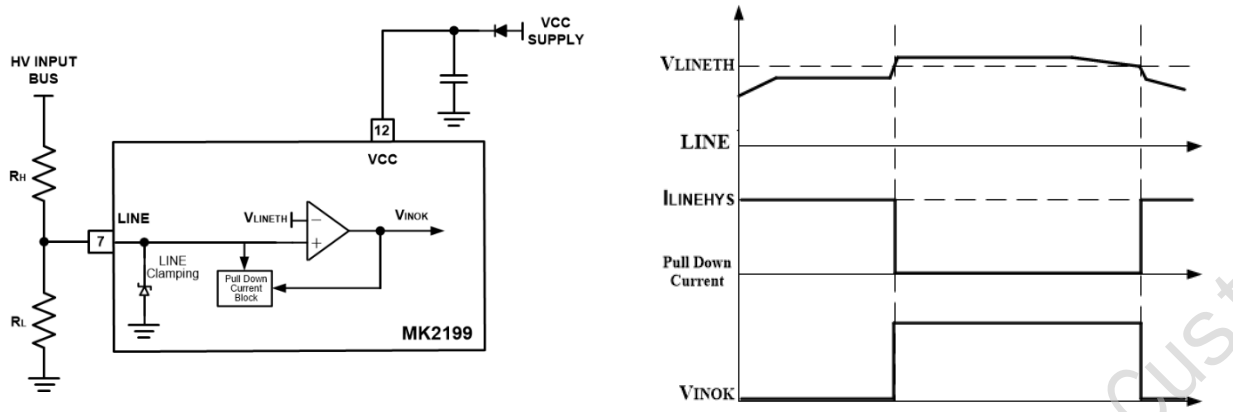

Figure 18. Line Sensing Function Internal Block Diagram and Timing Diagram

As an additional measure of safety, if the voltage on the LINE pin exceeds $V_{LINECLAMP}$, the MK2199 is shut down. If the VCC supply voltage remains above the UVLO threshold, the IC will restart as the voltage falls below $V_{LINECLAMP}$. Once the device is operating, the LINE pin is a high impedance input due to the high value resistors connected externally, making it susceptible to noise pickup. This noise may alter the OFF threshold or cause unintended shutdowns, particularly during ESD tests. Bypass the pin to ground with a small film capacitor (e.g., 1-10 nF) to prevent such malfunctions. When unused, the LINE pin must be connected to a voltage greater than V_{LINETH} but lower than $V_{LINECLAMP}$.

8.3.4 Oscillator

The oscillator frequency is set by capacitor CF, connected from PIN3 to GND, which is alternately charged and discharged via the network connected to PIN4. PIN4 provides an accurate V_{REF} reference and sources a current of approximately I_{RF}. The oscillator frequency is directly proportional to this sourced current. A simplified internal circuit is shown in the block diagram of Figure 19.

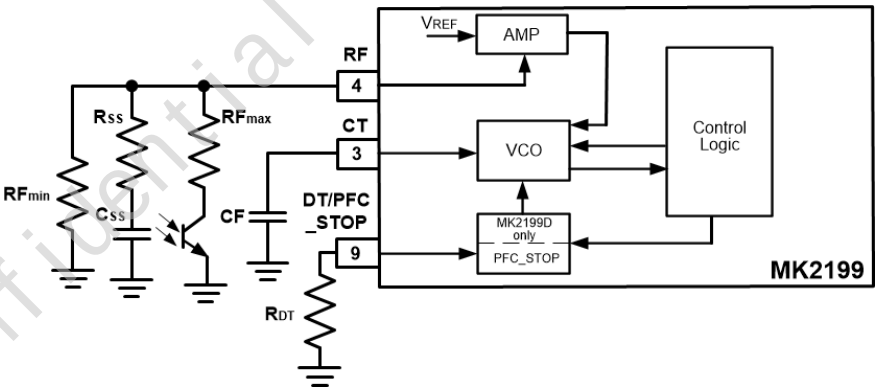

Figure 19. Oscillator Internal Block Diagram

The load network connected to the RF pin typically consists of three circuit branches:

1. A resistor RF_{min} is connected between the RF (pin 4) and GND, which determines the minimum operating frequency.

2. A resistor RF_{max} is connected between the RF (pin 4) and the collector of the phototransistor (emitter grounded) that transfers the feedback signal from the secondary side back to the primary side; while in operation, the phototransistor will modulate the current through this branch, hence modulating the oscillator

frequency to perform output voltage regulation; the value of RF_{max} determines the maximum frequency at which the half-bridge operates when the phototransistor is fully saturated.

3. An RC series circuit (C_{SS} + R_{SS}) connected between the RF pin and ground enables frequency shifting during startup. Note that this branch's contribution is negligible during steady-state operation (ideal case). It is approximately calculated using the following formula:

$$f_{min} = \frac{1}{3 \cdot CF \cdot RF_{min}}$$

$$f_{max} = \frac{1}{3 \cdot CF \cdot (RF_{min} || RF_{max})}$$

Once CF is set in the range of hundreds of picofarads to nanofarads (e.g., 100 pF – 1 nF), the values of RF_{min} and RF_{max} are determined according to the selected oscillator frequency range (from lowest to the highest). This frequency span must ensure the output voltage remains stabilized through the feedback control loop. RF_{max} requires a different selection criterion if burst-mode operation at no-load is employed. It is approximately calculated using the following formula:

$$RF_{min} = \frac{1}{3 \cdot CF \cdot f_{min}}$$

$$RF_{max} = \frac{RF_{min}}{\frac{f_{max}}{f_{min}} - 1}$$

Figure 20, illustrates the relationship between the oscillator waveform and the gate-driving signals.

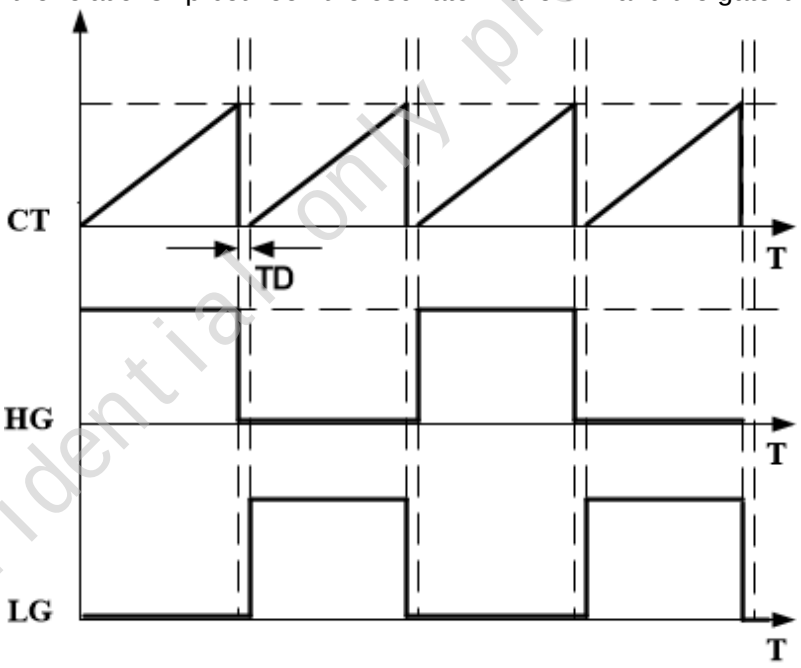

Figure 20. Oscillator waveforms relationship with gate-driving signals

To ensure symmetry in high-side (HG) and low-side (LG) pulse widths, the MK2199 integrates a unique oscillator structure.

As shown in Figure 20, when HG turns on, the CT pin begins charging the capacitor CF. After reaching a fixed voltage, HG is pulled low, the capacitor CF rapidly discharges, and the dead time countdown begins. When the dead time countdown completes, LG turns on and the CT pin resumes charging the capacitor CF.

This enhanced oscillator circuit structure ensures both HG and LG pulse widths adhere to the same

operational framework, thereby eliminating performance discrepancies. Additionally, the structure features programmable dead time configuration, enabling precise adjustment of the timing interval.

For the MK2199D variant, the dead time can be configured via an external resistor connected pin 9 (DT/PFC_STOP). The dead time can be calculated using the following formula:

$$\mathrm{TD\ (s)} \approx \frac{7 * 10^{-3}}{\mathrm{R_{DT}}}$$

For example, R_{DT} = 20 kΩ, TD = 350 ns. The characteristic curve between dead time TD and resistance R_{DT} is shown in Figure 21.

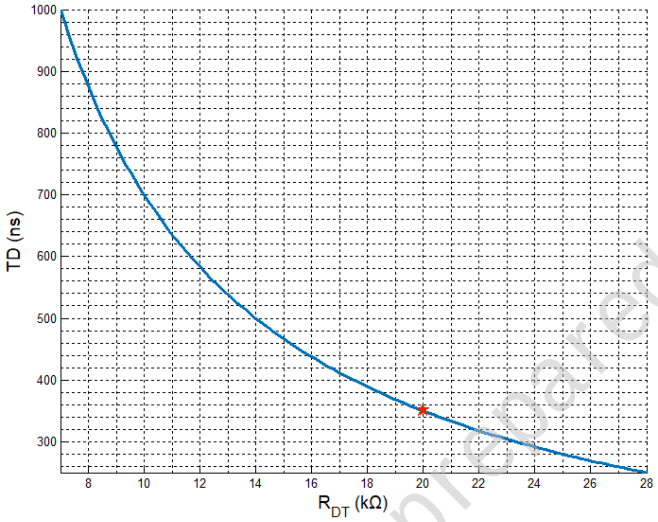

Figure 21. The Characteristic Curve Between Dead Time TD and Resistance R_{DT}

8.3.5 Current Sensing and OCP (ISEN pin)

The resonant half-bridge operates as a fundamentally voltage-mode control topology, where the current-sensing input serves solely for overcurrent protection (OCP). Unlike PWM-controlled converters, where energy flow is regulated by primary switch duty cycle, the resonant half-bridge controls power transfer by adjusting the switching frequency relative to the resonant frequency.

In the resonant half-bridge, the duty cycle remains fixed, and energy transfer is regulated by switching frequency, a characteristic that shapes its current-limiting approach. By contrast, PWM-controlled converters limit energy transfer by terminating switch conduction immediately upon detecting current exceeding a set threshold, enabling fast overcurrent protection.

In a resonant half-bridge overcurrent protection circuit, the switching frequency (i.e., the oscillator frequency) must be increased. This adjustment cannot occur as quickly as turning off a switch: it takes at least one oscillator cycle to observe a frequency change. This implies that, to effectively modulate energy flow, the frequency change rate must be slower than the switching frequency itself. This, in turn, implies that cycle-by-cycle current limitation is infeasible, necessitating that the primary current information fed to the current-sensing input be averaged. Of course, the averaging time must be sufficiently short to prevent the primary current from reaching excessive values. Figure 22 shows a typical application circuit with high efficiency.

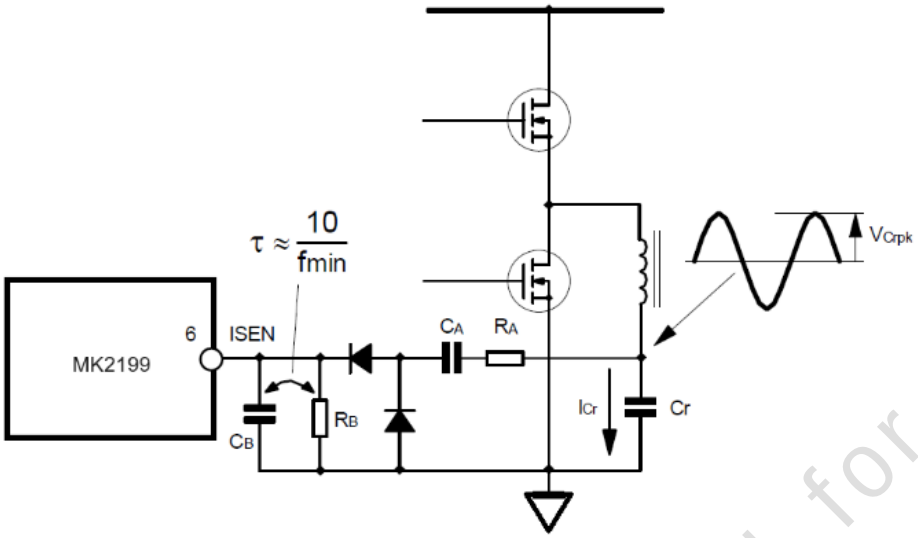

Figure 22. Lossless Current Sensing Technique with Capacitive Shunt

The device provides a current-sensing input (pin 6, ISEN) and an overcurrent management system. The ISEN pin feeds into two comparators: the inverting input of the first comparator is referenced to V_{ISEN}, while the inverting input of the second comparator is referenced to $V_{ISENDIS}$. If the voltage higher than V_{ISEN}, the first comparator outputs a high signal, turning on an internal switch that discharges the soft-start capacitor. This action rapidly increases the oscillator frequency, limiting energy transmission. The discharge continues until the ISEN voltage drops below (V_{ISEN} - $V_{ISENHYS}$). When the output is shorted, this operation results in a nearly constant peak primary current.

When the ISEN voltage exceeds V_{ISEN} and reaches $V_{ISENDIS}$, triggering the second comparator threshold, the MK2199 and MK2199D disable their gate drivers and pull the DT/PFC_STOP pin low. The MK2199 and MK2199D support auto-recovery functionality via the DELAY pin, which configures the restart timeout without latch-off protection. For applications requiring latch-off protection, the MK2199L variant latches off the outputs upon overcurrent detection. To reset the latch, The VCC supply voltage must be cycled below the UVLO threshold.

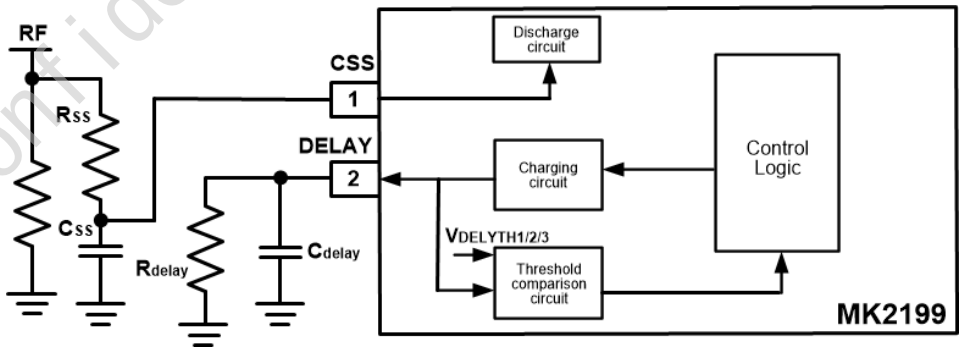

Figure 23. CSS and DELAY Internal Block Diagram

The designer can externally configure the maximum allowable duration for converter operation under overload or short-circuit conditions. As shown in Figure 23, this function is implemented by connecting an external capacitor C_{delay} in parallel with a resistor R_{delay} from Pin 2 (DELAY) to ground. When the voltage

on the ISEN pin exceeds V_{ISEN}, the first OCP comparator, besides discharging the soft-start capacitor C_{SS}, activates an internal current generator. This generator sources approximately $I_{DELYCHARGE}$ from the DELAY pin, charging capacitor C_{delay}. During an overload or short-circuit, the OCP comparator and the internal current source are repeatedly activated. Capacitor C_{delay} is then charged by an average current that primarily depends on the time constant of the current-sense filtering circuit on C_{SS} and the resonant circuit parameters. The discharge through R_{delay} can be neglected, considering that the associated time constant is typically much longer. Once C_{delay} charges to $V_{DELYTH1}$ the internal switch that discharges C_{SS} is held low continuously, regardless of the OCP comparator output, and the $I_{DELYCHARGE}$ current source remains enabled until the voltage on C_{delay} reaches $V_{DELYTH2}$. Once the voltage across C_{delay} reaches $V_{DELYTH2}$, the controller stops switching, and the DT/PFC_STOP pin is pulled low. Consequently, the internal current source is disabled, allowing C_{delay} to discharge slowly through R_{delay}. The IC restarts once the voltage across C_{delay} drops below $V_{DELYTH3}$.

8.3.6 OVP or OTP Protection （DIS pin）

The DIS pin is used to implement over-voltage protection (OVP) or over-temperature protection (OTP). For OTP, an external NTC voltage divider monitors temperature, and for OVP, an optocoupler samples the output voltage, or monitors the primary VDD_PRI voltage for over-voltage. When the DIS pin voltage exceeds V_{DISTH}, the internal comparator toggles, triggering the controller to enter protection mode. Different device variants offer latch-up or auto-recovery options to suit various applications. A typical application circuit is shown in Figure 24.

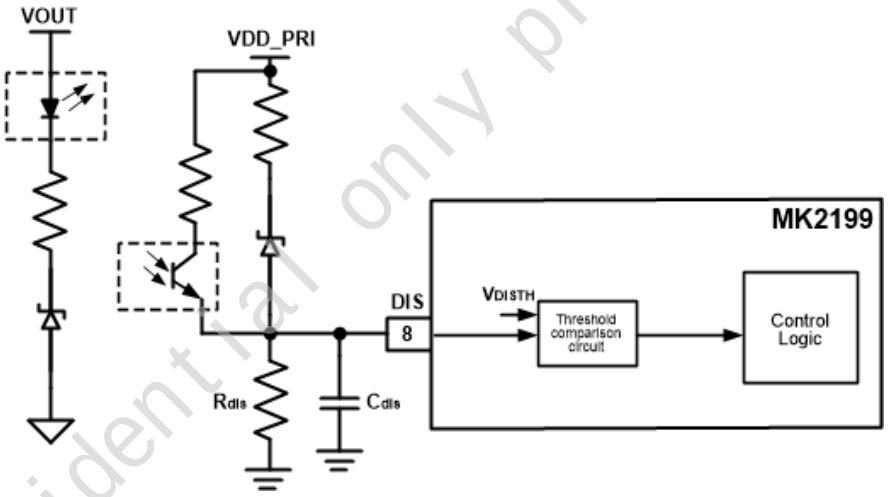

Figure 24. OVP Typical Application Circuit

8.3.7 Operation at No Load or Very Light Load （STBY pin）

The designer can configure the converter to operate in burst mode, where several switching cycles are followed by extended idle periods with both MOSFETs turned off. This approach significantly reduces the average switching frequency. Consequently, the average value of the residual magnetizing current, and the associated losses is significantly reduced, enabling the converter to meet energy-efficiency standards. The controller can be operated in burst mode by using pin 5 (STBY). when STBY pin voltage drops below $V_{STBYDIS}$, the IC enters an idle state where both gate-drive outputs are held low, the oscillator stops, the soft-start capacitor C_{SS} retains its charge and only the V_{REF} reference at the RF pin stays alive to minimize IC consumption. The IC resumes normal operation as the voltage on STBY pin exceeds $V_{STBYDIS}$ by $V_{STBYHYS}$.

To implement burst mode operation, the voltage applied to Pin 5 (STBY) must be tied to the feedback loop. Figure 25 illustrates the simplest implementation.

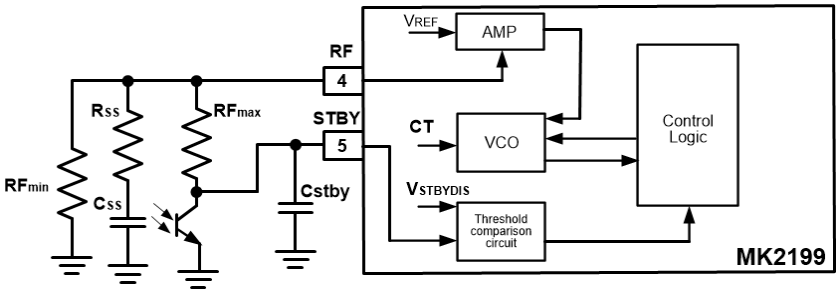

Figure 25. Burst Mode Implementation Circuit

9. Application and Implementation

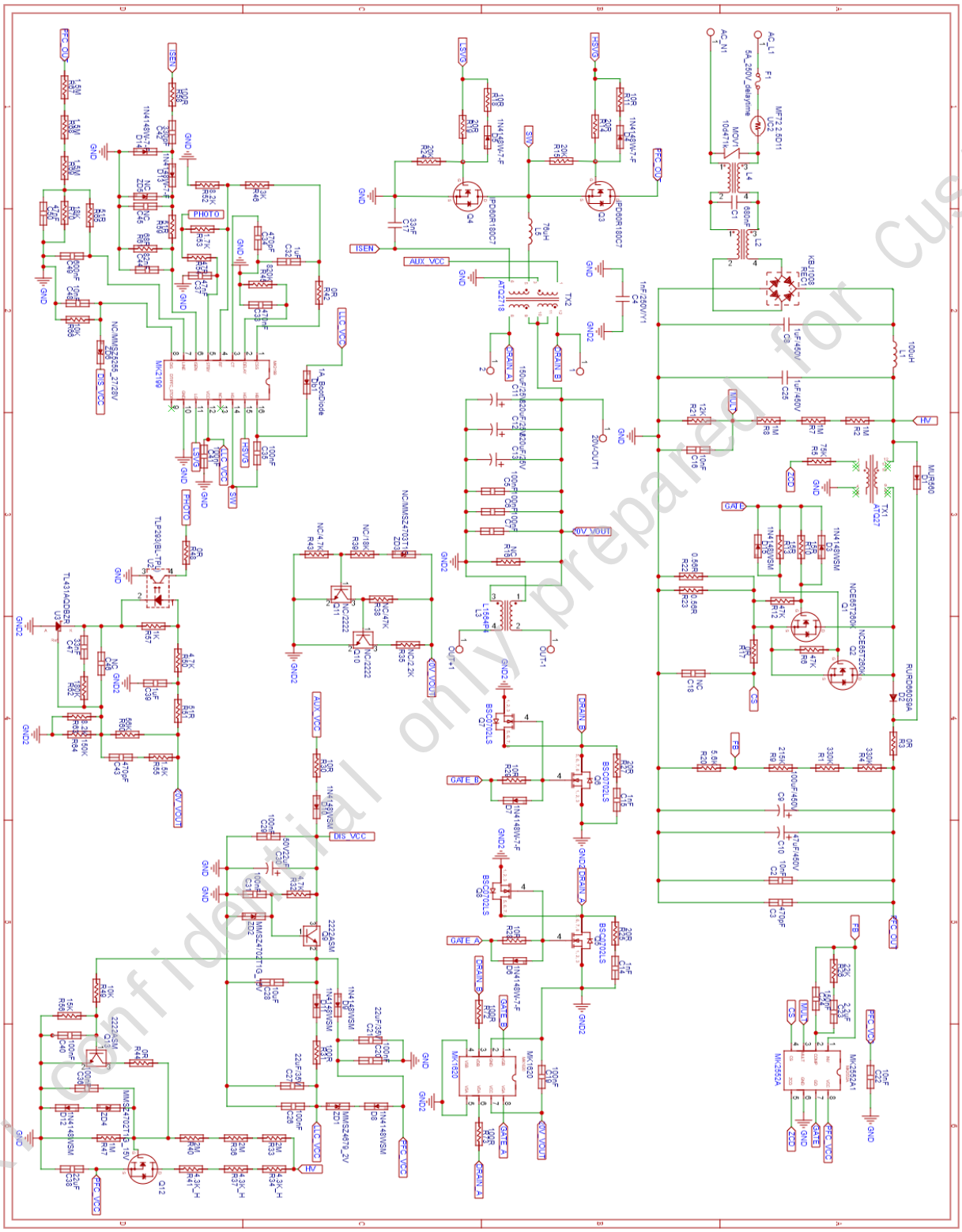

Figure 26. MK2199 Reference Design Circuit （MK2552+MK2199+MK1620 240W 20V）

10. Power Supply Recommendations

11. Layout

11.1 Layout Guidelines

To achieve high performance of the MK2199, the following layout tips must be followed.

1. Multi-point grounding, signal ground and power ground need to be separated.
2. The two drive signals are differential traces, and the loop needs to be as small as possible.
3. The resistor / capacitor of the ISEN, RF and CT pins needs to be located close to the IC.
4. At least one low-ESR ceramic bypass capacitor (100nF) must be used and placed as close as possible between the MK2199's VCC and GND pins.
5. At least one low-ESR ceramic bypass capacitor (100nF) must be used and placed as close as possible between the MK2199's HB and HS pins.
6. Use separate clean traces for VCC and GND pins.
7. Use separate clean traces for HB and HS pins.
8. The GND pin on the ground plane needs to route with a short and wide trace, or use a GND plane underneath the IC connected to the GND pin as well.
9. The pinout of the MK2199 is ideally suited for separating the high di/dt induced noise on the power ground from the low current quiet signal ground required for adequate noise immunity.

11.2 Layout Example

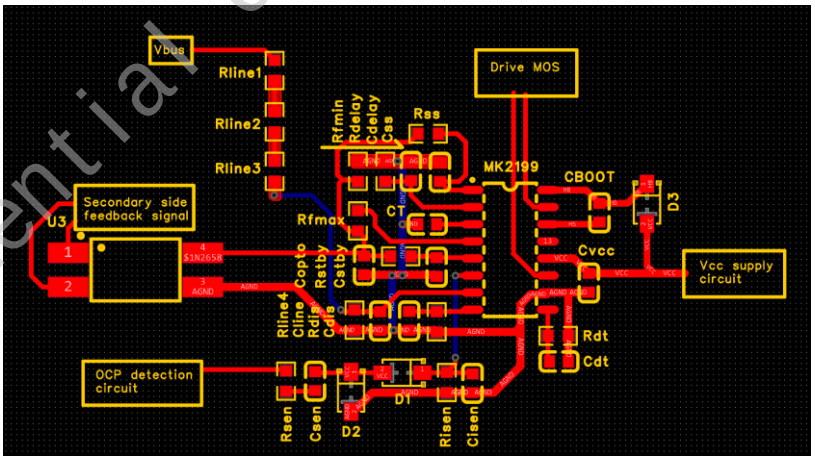

Figure 27. MK2199 Layout Example

12. Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13. Mechanical, Packaging

13.1 Package Size

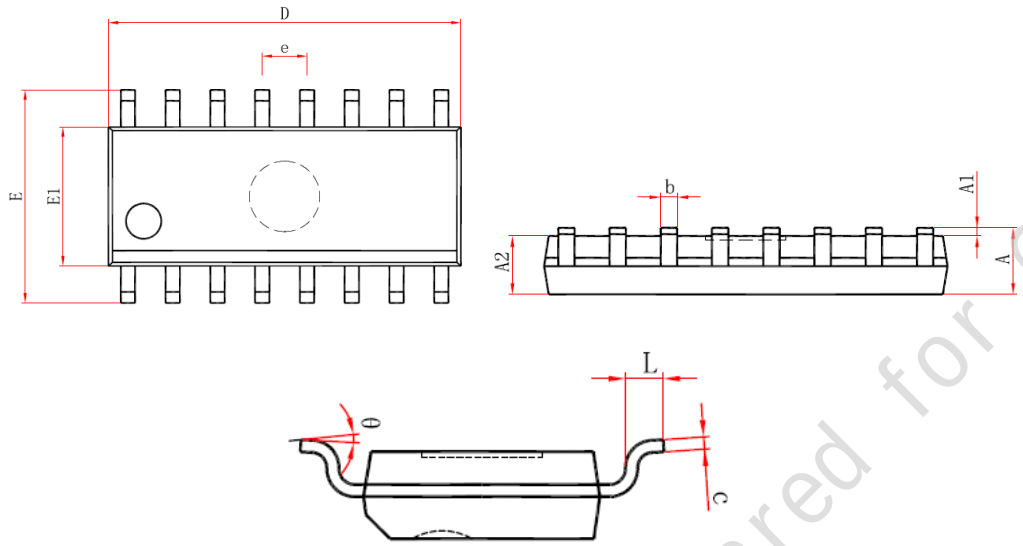

Figure 28. Package Dimensions

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
A2	1.30	1.40	1.50
b	0.33	-	0.51
c	0.17	-	0.25
D	9.80	10.00	10.20
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27(BSC)		
L	0.4	-	1.27
θ	0°	-	8°

Notes:

(1) This drawing is subject to change without notice

(2) The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

14. Reel and Tape Information

14.1 Reel and Tape Information

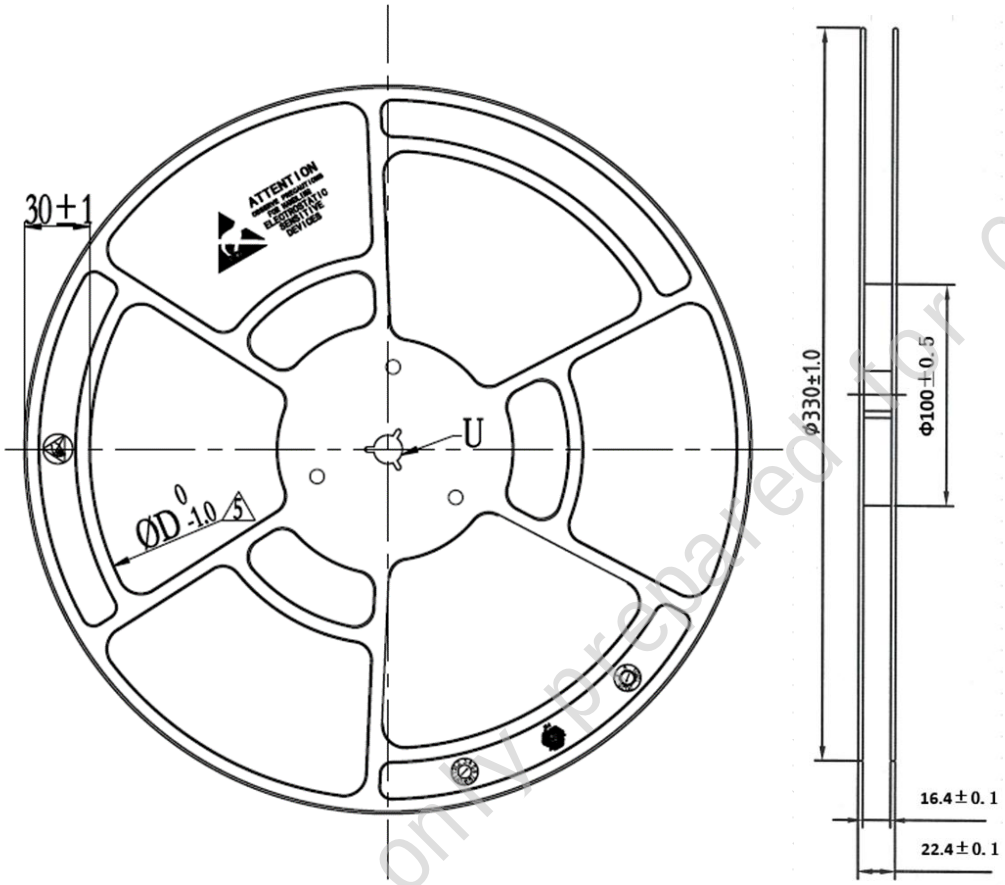

Figure 29. Reel Dimensions

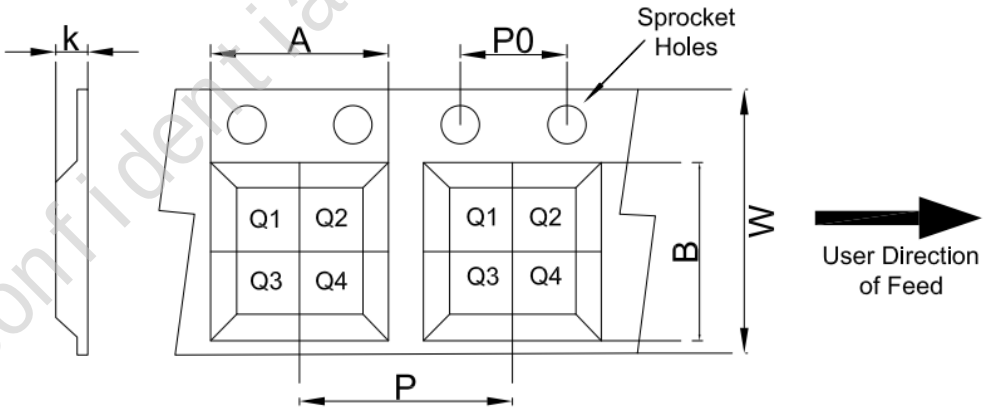

Figure 30. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
MK2199XAC	SOP16	16	3000	6.7±0.1	10.4±0.1	2.1±0.1	8.0±0.1	4.0±0.1	16±0.3	Q1
MK2199DXAC	SOP16	16	3000	6.7±0.1	10.4±0.1	2.1±0.1	8.0±0.1	4.0±0.1	16±0.3	Q1
MK2199LXAC	SOP16	16	3000	6.7±0.1	10.4±0.1	2.1±0.1	8.0±0.1	4.0±0.1	16±0.3	Q1

15. Tape and Reel Box Dimensions

15.1 Reel Box Dimensions

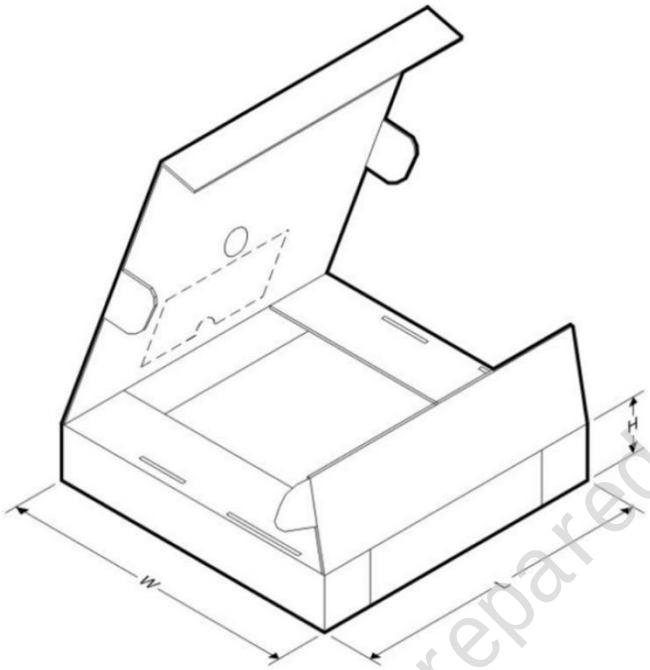

Figure 31. Rell Box Dimensions

Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MK2199XAC	SOP16	16	6000	360	360	65
MK2199DXAC	SOP16	16	6000	360	360	65
MK2199LXAC	SOP16	16	6000	360	360	65