4-A, 7-A Peak, 5.7kV$_{RMS}$ Isolated Dual-Channel Gate Driver

1. Description

The MD18023A/B/C-Q1 is an isolated dual channel gate driver family designed with 4-A source current and 7-A sink current to drive IGBTs, Si and SiC MOSFETs.

The device can be configured as two low-side drivers, two high-side drivers and a half bridge driver. The input side is isolated from the output side by 5.7kVRMS isolation barrier with a minimum of 200-V/ns common mode transient immunity (CMTI).

The inputs can handle -10V to 26V DC, which increases robustness against ringing from parasitic inductance of long routing traces.

Other features include resistor programmable dead time (DT PIN) control, disable feature to shutdown both outputs, and UVLO for all supplies.

2. Applications

- Isolated AC-DC and DC-DC power supplies
- Server, telecom, datacom, and industrial infrastructures.
- PV Inverters
- HEV and EV battery chargers

3. Features

- Universal: Dual Low-side, Dual High-side, and Half Bridge Driver
- 4-A Source and 7-A Sink Peak Currents
- CMTI greater than 200V/ns
- Input Pins Can Tolerate -10V to 26V, Independent of Supply Voltage Range
- Fast Disable for Power Sequencing
- TTL Compatible Inputs
- Safety-related Certifications:
  (1) 8000-VPK reinforced Isolation per EN 60747-17
  (2) 4242-VPK based Isolation per EN 60747-17
  (3) SOW16:5.7kVRMS isolation for 1minute per UL 1577
  (4) SOP16: 3kVRMS isolation for 1minute per UL 1577
- Available in SOP16 and SOW16 packages

4. Typical Applications

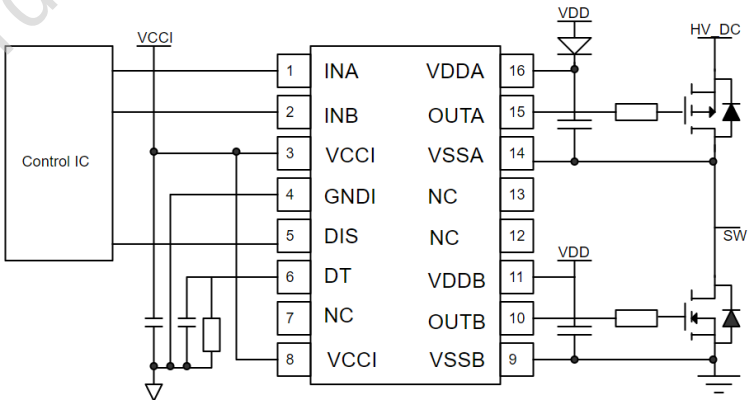
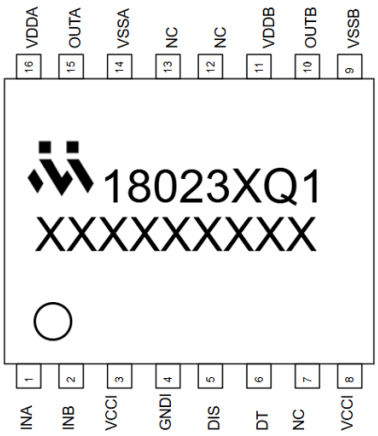


Figure 1.Typical Application Diagram

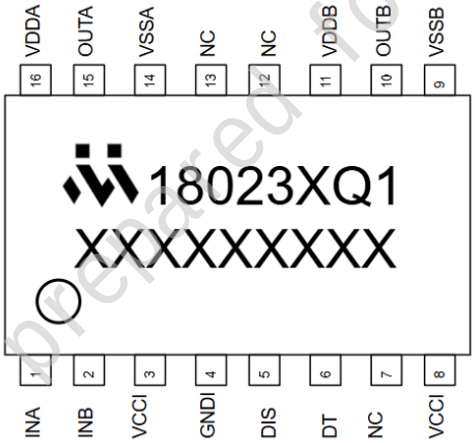
5. Order Information

Order Code	UVLO	DT	EN/DIS	Package	Pins	SPQ (pcs)
MD18023AWAC-Q1	5V	YES	DIS	SOW-16	16	1500
MD18023BWAC-Q1	8V	YES	DIS	SOW-16	16	1500
MD18023CWAC-Q1	12V	YES	DIS	SOW-16	16	1500
MD18023ANAC-Q1	5V	YES	DIS	SOP-16	16	3000
MD18023BNAC-Q1	8V	YES	DIS	SOP-16	16	3000
MD18023CNAC-Q1	12V	YES	DIS	SOP-16	16	3000

6. Package Reference and PIN Functions



SOW-16



SOP-16

Name		Description	
SOW-16	SOP-16	Symbol	Function
1	1	INA	Input signal for A channel. Input of Channel A with internal pull-down resistance to GNDI.
2	2	INB	Input signal for B channel. Input of Channel B with internal pull-down resistance to GNDI.
3, 8	3, 8	VCCI	Primary-side (input side) supply voltage. Locally decoupled to GNDI using low ESR/ESL capacitor located as close to the device as possible.
4	4	GNDI	Primary-side (input side) ground reference. All signals in the primary side are referenced to this ground.
5	5	DIS	Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using 1nF low ESR/ESL capacitor close to DIS pin when connecting to a micro controller with distance.
6	6	DT	Programmable dead time function. Tying DT to VCCI allows the outputs to overlap. Placing a 5kΩ to 200kΩ resistor (R_{DT}) between DT and GNDI adjusts dead time according to: DT (ns) = 12 x R_{DT} (kΩ). It is recommended to parallel a ceramic capacitor, 470 pF or lower, close to the DT pin with R_{DT} to achieve better noise immunity. It is not recommended to leave DT floating.
7,12,13	7,12,13	NC	No Internal connection.
9	9	VSSB (1)	Ground for secondary-side driver A. Ground reference for secondary side B channel.
10	10	OUTB	Output of Channel B
11	11	VDDB (1)	Secondary-side power for driver B. Locally decoupled to VSSB using a low ESR/ESL capacitor located as close to the device as possible.
14	14	VSSA (1)	Ground for secondary-side driver A. Ground reference for secondary side A channel.
15	15	OUTA	Output of Channel A
16	16	VDDA (1)	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.

Note:

（1）VDD stands for VDDA or VDDB, VSS stands for VSSA or VSSB.

7. Specifications

7.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted) (1)

	MIN	MAX	Unit
VCCI-GNDI	-0.3	26	V
INA, INB, DIS(EN)	-10	26	V
DT	-0.3	26	V
VDDA-VSSA, VDDB-VSSB	-0.3	30	V
OUTA-VSSA, OUTB-VSSB	-0.3	VDDA/B+0.3	V
OUTA-VSSA, OUTB-VSSB, Transient for 200ns	-2	VDDA/B+0.3	V
OUTA-VSSA, OUTB-VSSB, Transient for 100ns	-5	VDDA/B+0.3	V
Junction Temperature (T_J)	-40	150	°C
Storage Temperature	-65	150	°C
Channel A to Channel B Maximum Repetitive Isolation		1500	V_{peak}

Note:

(1) Exceeding these ratings may cause permanent damage to the device. The device is not guaranteed to function outside of its operating conditions.

7.2 ESD Ratings

		Value	Unit
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

Notes:

(1) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002.

(2) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011.

7.3 Recommended Operating Conditions

	MIN	MAX	Unit
VCCI-GNDI	3.0	24	V
INA, INB, DIS(EN)	-8	24	V
VDDA-VSSA, VDDB-VSSB for A Version	5.5	28	V
VDDA-VSSA, VDDB-VSSB for B Version	8.5	28	V
VDDA-VSSA, VDDB-VSSB for C Version	12.5	28	V
Junction Temperature	-40	140	°C
Ambient Temperature	-40	125	°C

7.4 Thermal Information (1)

	$R_{\theta JA}$	$R_{\theta JC}$	Unit
SOP-16	122.3	38.1	°C/W
SOW-16	104.3	30.4	°C/W

Note:

(1) According to JEDEC JESD51-2, JESD51-7 at natural convection on FR4 1s0p board

7.5 Insulation Specifications

Description	Test Condition	Symbol	Value		Unit
			SOW-16	SOP-16	
Min. External Air Gap (Clearance)		CLR	8	4	mm
Min. External Tracking (Creepage)		CPG	8	4	mm
Distance through the Insulation		DTI	100	50	um
Comparative Tracking Index	DIN EN 60112	CTI	>600		V
Material Group	IEC 60112		I		
Insulation Specification per EN 60747-17					
Climatic Category			40/125/21		
Pollution Degree			2		
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1250	700	V_{RMS}
	DC voltage		1768	990	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	1768	990	V_{peak}
Input to Output Test Voltage, Method B1	$V_{ini.b} = V_{IOTM}$ $V_{pd(m)} = V_{IORM} \times 1.5$ $t_{ini} = t_m = 1$ sec $q_{pd} \leq 5$pC 100% production test	$V_{pd(m)}$		1050	V_{RMS}
	$V_{ini.b} = V_{IOTM}$ $V_{pd(m)} = V_{IORM} \times 1.875$ $t_{ini} = t_m = 1$ sec $q_{pd} \leq 5$pC 100% production test	$V_{pd(m)}$	2344		V_{RMS}
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{ini.a} = V_{IOTM}$ $V_{pd(m)} = V_{IORM} \times 1.3$ $t_{ini} = 60$ sec $q_{pd} \leq 5$pC	$V_{pd(m)}$		910	V_{RMS}
	$V_{ini.a} = V_{IOTM}$ $V_{pd(m)} = V_{IORM} \times 1.6$ $t_{ini} = 60$ sec $q_{pd} \leq 5$pC	$V_{pd(m)}$	2000		V_{RMS}

Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{ini.a} = V_{IOTM}$ $V_{pd(m)} = V_{IORM} \times 1.2$ t_{ini} = 60 sec t_m = 10 sec $q_{pd} \leq$ 5pC	$V_{pd(m)}$	1500	840	V_{RMS}
Maximum Transient Isolation Voltage	t = 60 sec	V_{IOTM}	8000	4242	V_{peak}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.3 \times V_{IOSM}$	V_{IOSM}		5000	V_{peak}
	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$		8000		V_{peak}
Isolation Resistance	V_{IO} = 500 V, T_{amb} = 25℃	R_{IO}	> 10^{12}		Ω
	VIO = 500 V 100°C ≤ Tamb ≤ 125°C		> 10^{11}		
	V_{IO} = 500 V, $T_{amb} = T_S$		> 10^9		
Isolation Capacitance	f = 1MHz	C_{IO}	1.0		pF
UL 1577					
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}$, t = 1 sec 100% production test	V_{ISO}	5700	3000	V_{RMS}

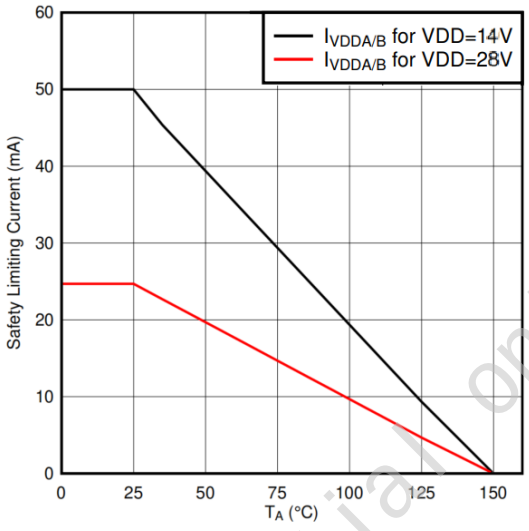
7.6 Safety-Limiting Values (1)

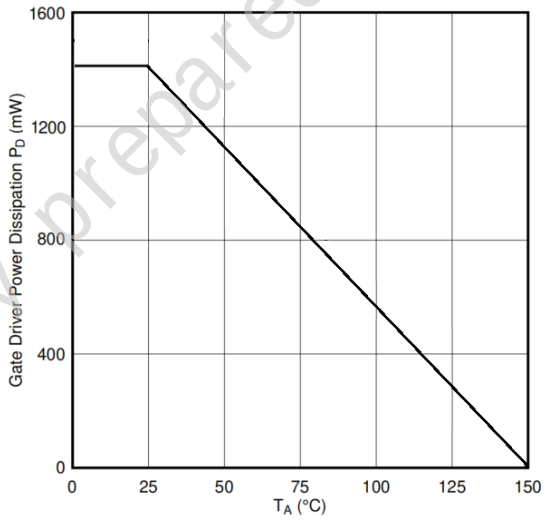
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Safety output supply current	I_S	VDD=14V			50	mA
		VDD=28V			25	mA
Safety supply power	P_S	INPUT			20	mW
		DRIVER A			700	mW
		DRIVER B			700	mW
		Total			1420	mW
Safety temperature	T_S				150	℃

Notes:

（1） Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

（2） The maximum safety temperature (T_S) has the same value as the maximum junction temperature (T_J). The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature (T_A).





7.7 Safety-Related Certifications

The MD18023 (A/B/C) WAC-Q1 (SOW16)

Certified according to EN 60747-17	UL 1577 Component Recognition Program
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}. Maximum repetitive peak isolation voltage, 1768 V_{PK}; Maximum surge isolation voltage, 8000 V_{PK}	Single Protection, 5700V_{RMS} Isolation Voltage
File (In progress)	File (In progress)

The MD18023 (A/B/C) NAC-Q1 (SOP16)

Certified according to EN 60747-17	UL 1577 Component Recognition Program
Basic insulation Maximum transient isolation voltage, 4242 V_{PK}. Maximum repetitive peak isolation voltage, 990 V_{PK}; Maximum surge isolation voltage, 5000 V_{PK}	Single Protection, 3000V_{RMS} Isolation Voltage
File (In progress)	File (In progress)

7.8 Electrical Characteristics

VCCI = 3.3 V or 5 V, 0.1µF capacitor from VCCI to GNDI, V_{VDD}= 15 V, 1µF capacitor from VDD to VSS, DT pin tied to VCCI, C_L = 0 PF, TA = –40°C to +125°C, (unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Currents						
VCCI quiescent current	I_{VCCI_OFF}	INA = INB = 0V VCCI=5V	0.7	1.3	2.4	mA
VDDA(B) quiescent current	$I_{VDDA(B)\_OFF}$	INA = INB = 0V VDD=15V	0.7	1.2	1.8	mA
VCCI operating current	I_{VCCI_ON}	f_{INA}=f_{INB} = 500kHz Duty = 50% C_{LOAD}=100pF		5.0	9.0	mA
VDDA(B) operating current	$I_{VDDA(B)\_ON}$			3.0	5.0	mA
Inputs (INA, INB, DIS)						
Input voltage rising threshold	V_{ITH}		1.55	1.75	1.95	V
Input voltage falling threshold	V_{ITL}		0.6	0.75	0.95	V
Input voltage hysteresis	V_{ITHYS}			1		V
Undervoltage Lockout						
VCCI rising threshold	V_{CCIR}		2.5	2.65	2.8	V
VCCI falling threshold	V_{CCIF}		2.4	2.53	2.66	V
VCCI threshold hysteresis	V_{CCIHYS}			0.12		V
VDDA(B) rising threshold	$V_{DDA(B)R}$	For A Version	5.2	5.5	5.8	V
VDDA(B) falling threshold	$V_{DDA(B)F}$		4.9	5.2	5.5	V
VDDA(B) threshold hysteresis	$V_{DDA(B)HYS}$		0.1	0.3	0.5	V
VDDA(B) rising threshold	$V_{DDA(B)R}$	For B Version	7.7	8.3	8.9	V
VDDA(B) falling threshold	$V_{DDA(B)F}$		7	7.6	8.2	V
VDDA(B) threshold hysteresis	$V_{DDA(B)HYS}$		0.4	0.7	1	V
VDDA(B) rising threshold	$V_{DDA(B)R}$	For C Version	10.5	12	13.5	V
VDDA(B) falling threshold	$V_{DDA(B)F}$		9.5	10.5	11.5	V
VDDA(B) threshold hysteresis	$V_{DDA(B)HYS}$		1	1.5	2	V
OUTPUTS (OUTA, OUTB)						
Source peak current	I_{SRC} (1)	C_{LOAD} = 0.22uF F_{SW} = 1kHz		4		A
Sink peak current	I_{SNK} (1)			7		A
High output voltage	V_{OH}	I_{OUT} = -10mA		12	20	mV
Low output voltage	V_{OL}	I_{OUT} = 10mA		6	10	mV
Output pullup resistance	R_{OH}	I_{OUT} = -10mA		1.2	2	Ω
Output pulldown resistance	R_{OL}	I_{OUT} = 10mA		0.6	1	Ω
DEAD TIME AND OPERLAP PROGRAMMING						
Dead time DT (ns) = 12 x R_{DT} (kΩ)	DT	DT tied to VCCI	Overlap			
		Open	5			us
		R_{DT} = 5kΩ	50	70	90	ns
		R_{DT} = 20kΩ (1)	200	240	280	ns

SWITCHING CHARACTERISTICS						
Rise time	t_R	C_{LOAD}=1.8nF		12	16	ns
Fall time	t_F	C_{LOAD}=1.8nF		8	12	ns
Minimum input pulse width that passes to output	t_{PWMIN}			50	80	ns
Rising propagation delay	$t_{RPDA(B)}$			70	90	ns
Falling propagation delay	$t_{FPDA(B)}$			55	75	ns
Pulse width distortion	t_{PWD}	$\lvert t_{RPDA(B)} - t_{FPDA(B)} \rvert$			30	ns
Channel A to Channel B delay match	t_{PDM}	$\lvert t_{RPDA} - t_{RPDB} \rvert$ $\lvert t_{FPDA} - t_{FPDB} \rvert$			10	ns
VCCI power-up time delay	t_{start_VCCI}	INA = INB = High		55	90	us
VDD power-up time delay	t_{start_VDD}	INA = INB = High		6	10	us
Common Mode Transient Immunity	CMTI (1)			200		V/ns

Note:

(1) Not subject to production test, guarantee by design.

7.9 Typical Characteristics

VDD = 15V, VCCI = 3.3 V, T_A = 25°C, no load unless otherwise noted.

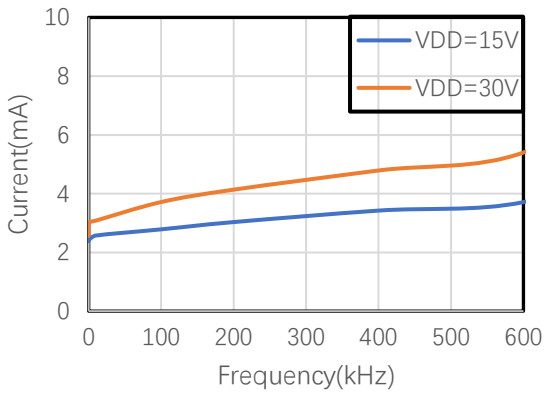


Figure 2. Per Channel ($I_{VDDA/B}$) Current Consumption Vs. Frequency (No Load)

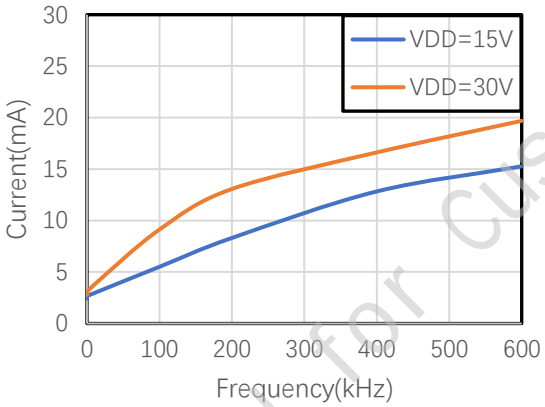


Figure 3. Per Channel (IVDDA/B) Current Consumption Vs. Frequency (1nF Load)

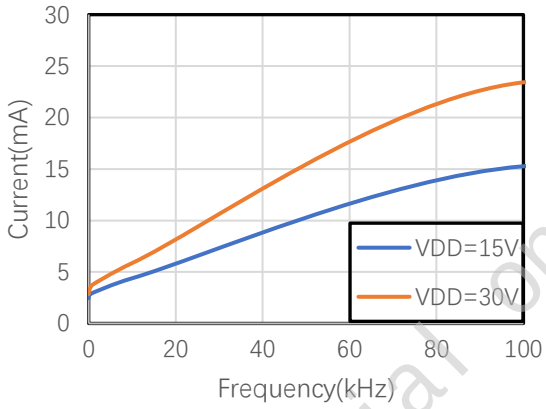


Figure 4. Per Channel (IVDDA/B) Current Consumption Vs. Frequency (10nF Load)

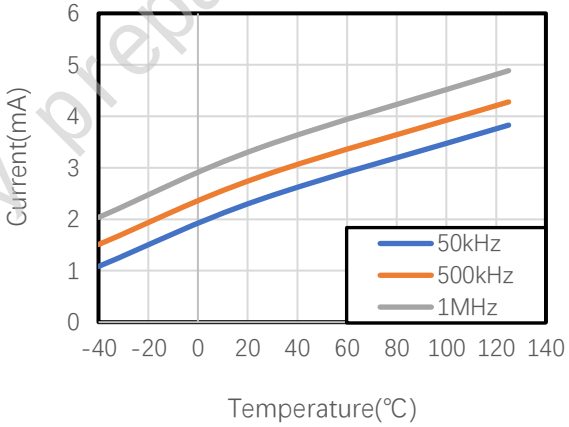


Figure 5. Per Channel (IVDDA/B) Supply Current Vs. Temperature (100-pF Load)

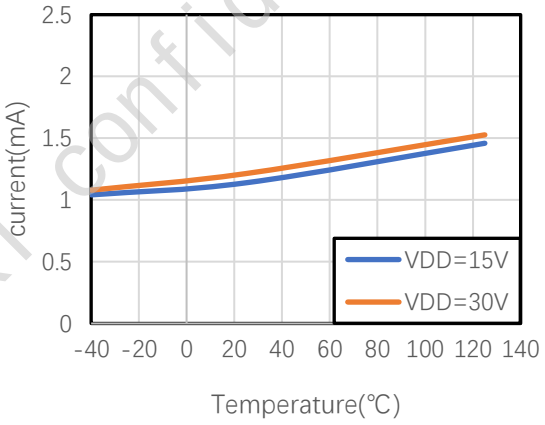


Figure 6. Per Channel (IVDDA/B) Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)

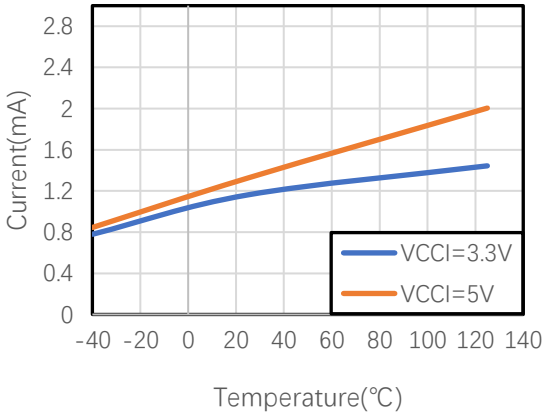


Figure 7. IVCCI Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)

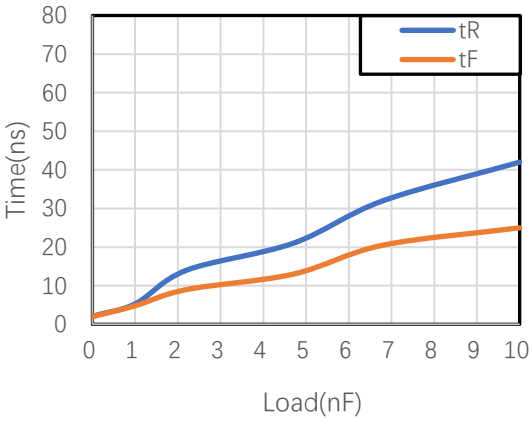


Figure 8. Rising and Falling Times

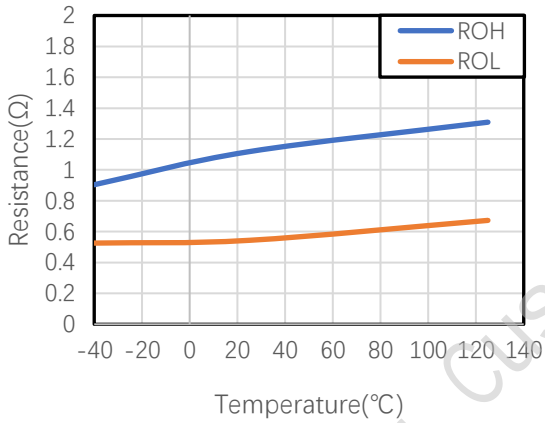


Figure 9. Output Resistance

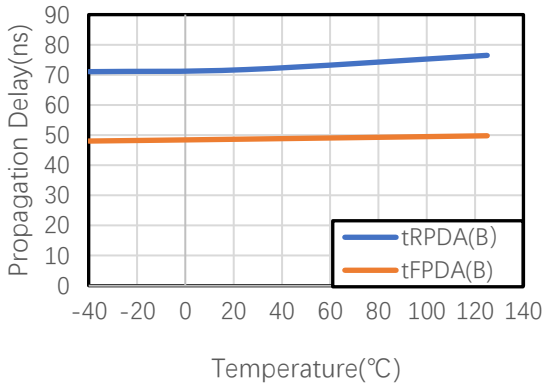


Figure 10. Propagation Delay

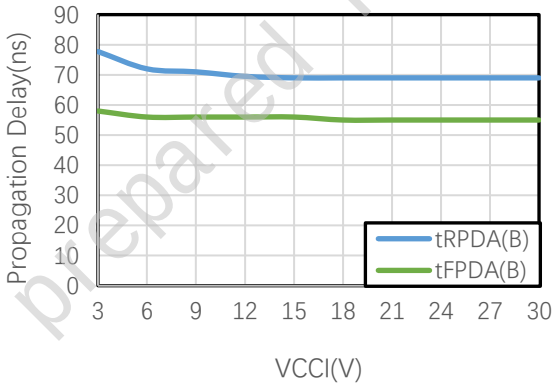


Figure 11. Propagation Delay

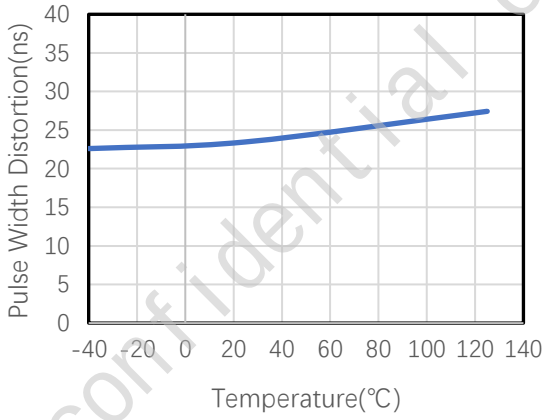


Figure 12. Pulse Width Distortion

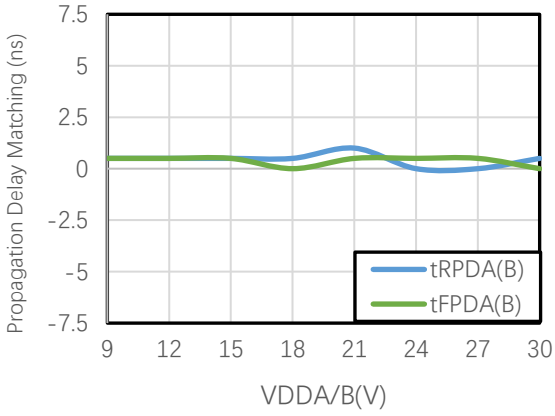


Figure 13. Propagation Delay Matching (tPDM)

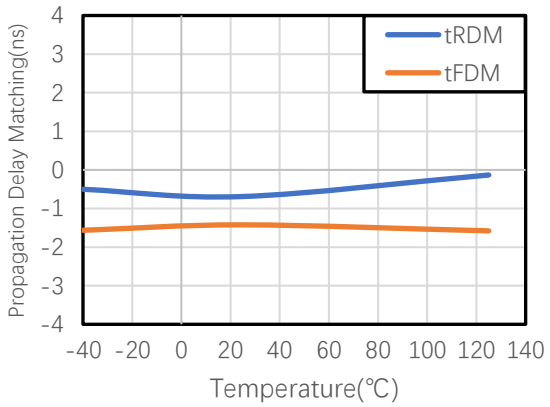


Figure 14. Propagation Delay Matching (tPDM)

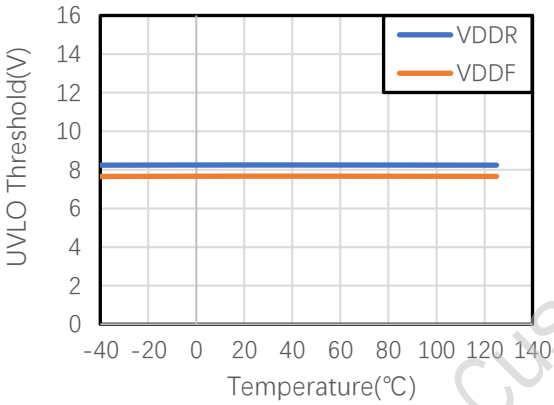


Figure 15. VDD UVLO Threshold

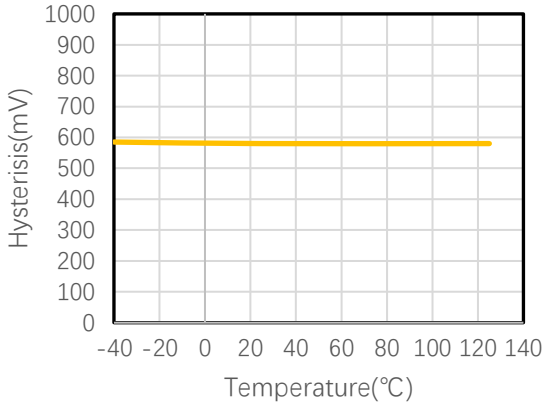


Figure 16. VDD UVLO Hysteresis

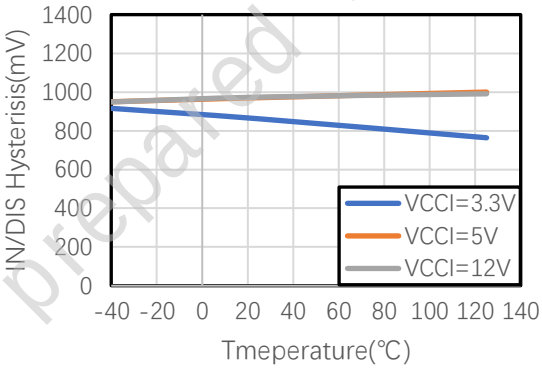


Figure 17. IN/DIS Hysteresis

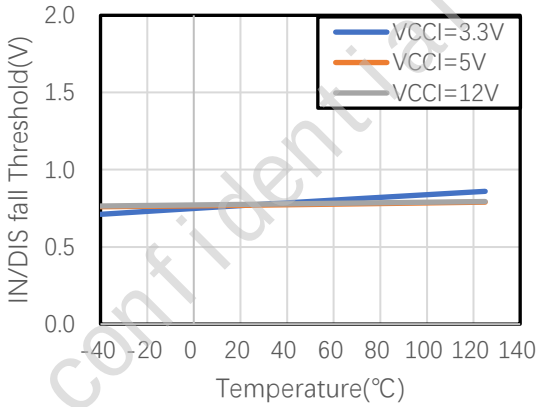


Figure 18. IN/DIS Fall Threshold

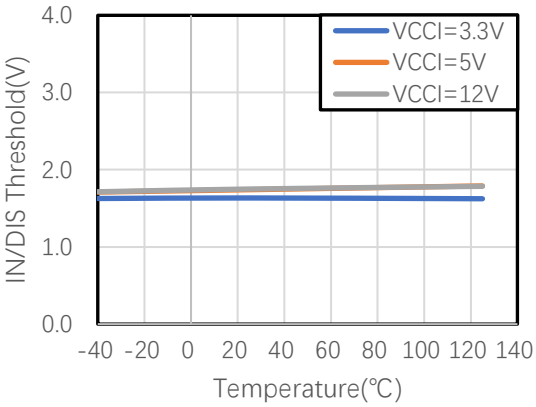


Figure 19. IN/DIS Rise Threshold

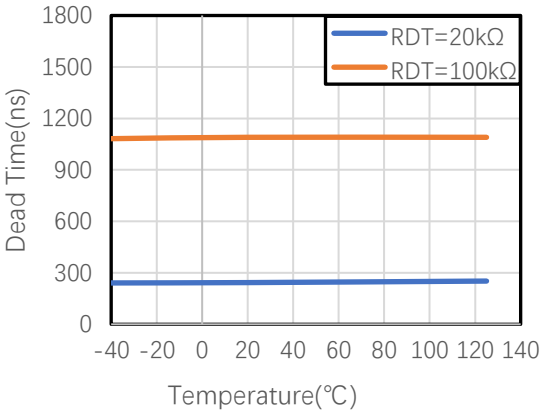


Figure 20. Dead Time

8. Parameter Measurement Information

8.1 Propagation Delay and Pulse Width Distortion

Figure 21 shows how one calculates pulse width distortion (t_{PWD}) and delay matching (t_{PDM}) from the propagation delays of channel A and channel B. It can be measured by ensuring that both inputs are in phase, and the dead time function disabled by shorting the DT Pin to VCCI.

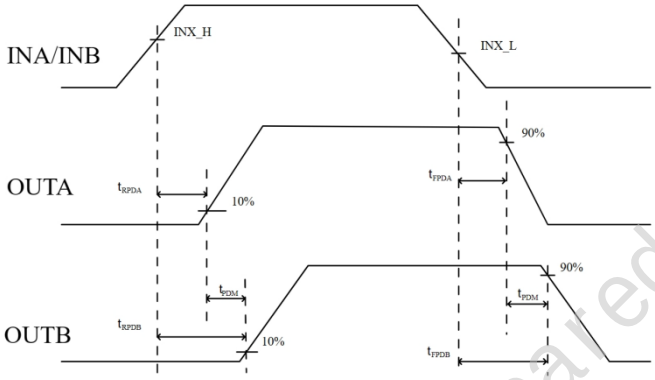


Figure 21. Propagation Delay and Channel to Channel Delay Match Time, connect DT to VCCI

8.2 Rising and Falling Time

Figure 22 shows the criteria for measuring rising (t_R) and falling (t_F) times.

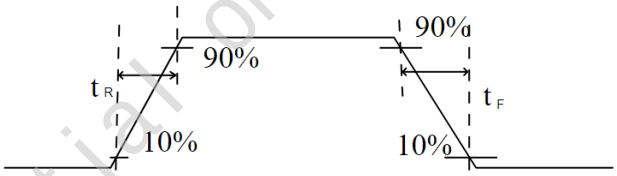


Figure 22. Rising and Falling Time Criteria

8.3 Input and Disable Response Time

Figure 23 shows the response time of the disable function. It is recommended to use a 1nF low ESR/ESL bypass capacitor close to DIS pin when connecting DIS pin to a micro controller with distance. For more information, see Disable Pin.

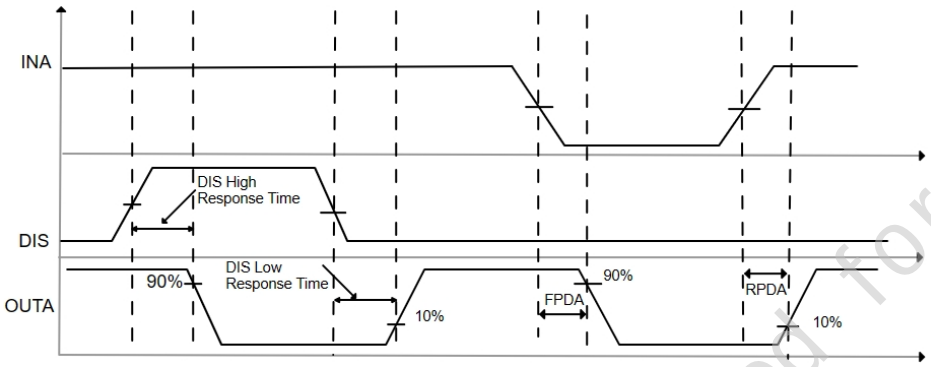


Figure 23. Disable Pin Timing

8.4 Power-up UVLO Delay to Output

Before the driver is ready to deliver an appropriate output state, there is a power-up delay time from the rising edge of the undervoltage lockout (UVLO) to outputs, which is defined as t_{start_VCCI} to OUTA(B) for VCCI UVLO (typically 55us) and t_{start_VDD} to OUTA(B) for VDD UVLO (typically 6us). It is recommended to consider proper margin time before launching PWM signal after the driver's VCCI and VDD bias supply is ready. Figure 24 and Figure 25 show the power up UVLO delay timing diagram for VCCI and VDD.

If INA or INB are active before VCCI or VDD have crossed their respective turn-on thresholds, the output will not update until VCCI or VDD has exceeded its UVLO rising threshold by the t_{start_VCCI} to OUTA(B) or t_{start_VDD} to OUTA(B) duration.

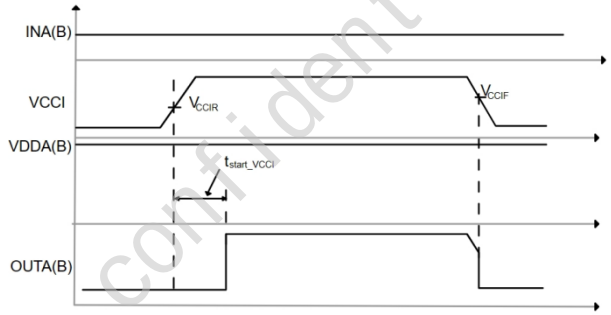


Figure 24. VCCI Power-up UVLO Delay

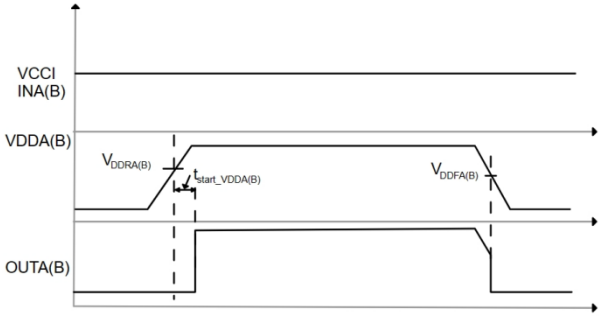


Figure 25. VDD Power-up UVLO Delay

8.5 CMTI Testing

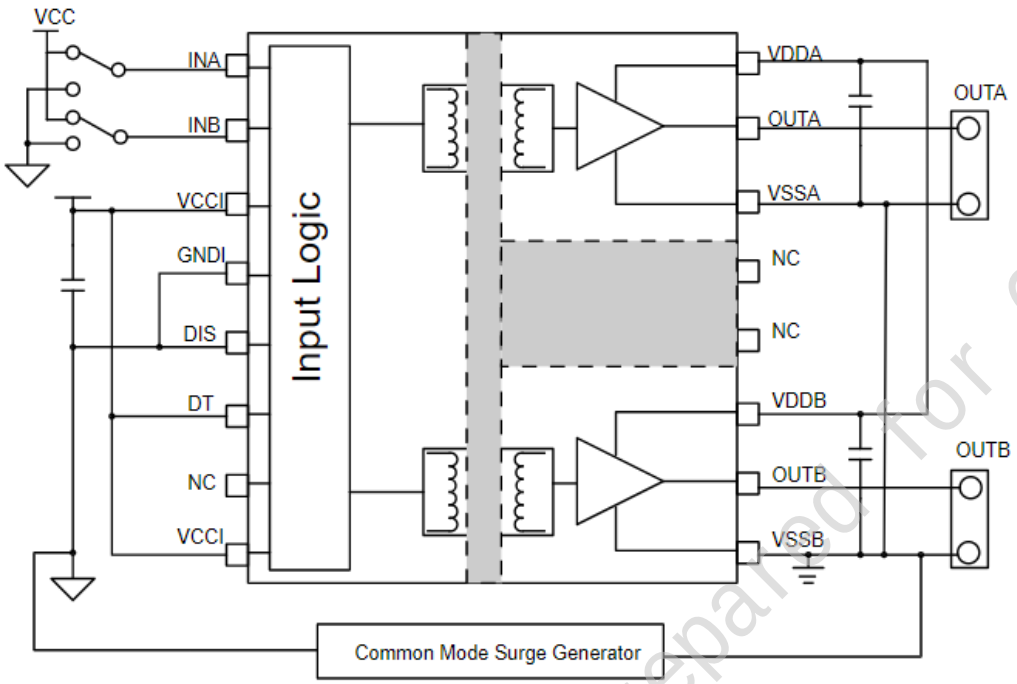


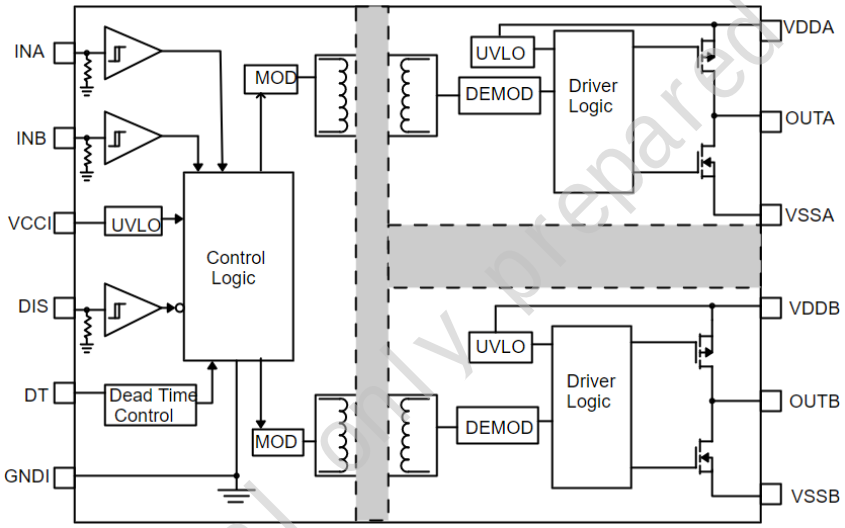
Figure 26. Simplified CMTI Testing Setup

9. Detailed Descriptions

9.1 Overview

The MD18023A/B/C-Q1 is an isolated dual channel gate driver family designed with 4-A source current and 7-A sink current to drive IGBTs, Si and SiC MOSFETs. The device can be configured as two low-side drivers, two high-side drivers and a half bridge driver. The input side (primary-side) is isolated from the output side (secondary-side) by 5.7kV$_{RMS}$ isolation barrier with a minimum of 200 V/ns common mode transient immunity. The inputs can handle -10V to 26V DC voltage range, which increases robustness against ringing from parasitic inductance of long routing traces. Other features include resistor programmable dead time (DT PIN) control, disable(enable) feature to shutdown both outputs, and UVLO functions for all supplies.

9.2 Functional Block Diagram



9.3 Input and Output Logic Table

MD18023A/B/C-Q1 operates in normal mode and UVLO mode. In the normal mode, the output state is dependent on states of the input pins. See as below:

Inputs		DIS	Outputs		Note
INA	INB		OUTA	OUTB	
L	L	L	L	L	
L	H	L	L	H	
H	L	L	H	L	
H	H	L	L	L	DT is programmed with R_{DT} & floating
H	H	L	H	H	DT is pulled high to VCCI
Floating	Floating	L	L	L	
Any	Any	H	L	L	Bypass using 1-nF capacitor close to DIS (EN) pin when connecting to a micro-controller with distance.

9.4 Input Stage

The input pins of MD18023A/B/C-Q1 are based on a TTL compatible input-threshold logic. The input voltage range is independent of the VCCI supply voltage. Since it has a typical high threshold (V_{ITH}) of 1.75V and a typical low threshold (V_{ITL}) of 0.75V, with little variation with temperature (Figure 18,Figure 19), and a wide hysteresis (V_{ITHYS}) of 1V for good noise immunity and stable operation, MD18023A/B/C-Q1 is conveniently driven by PWM control signals derived from 3.3V and 5V digital power-controller devices. Although the internal pull-down resistors force the input port to pull it low while remaining open (See Functional Block Diagram), it is recommended to tie the input pins to the ground if it is not being used. Furthermore, Since the input side of the MD18023A/B/C-Q1 is isolated from the output driver, and the input control is independent of VCCI, the input signal amplitude can be greater or less than VCCI as long as the recommended operating limits are not exceeded. When integrated with a control source in the system, greater flexibility can be maintained and users can select the most efficient VDD for the gate overdrive voltage of their choice.

9.5 Output Stage

The output stage of MD18023A/B/C-Q1 features the PMOS as pull up structure and the pull-down structure with NMOS. PMOS provides the pull up capability when Input is 'HIGH'. and the R_{OH} parameter is a DC measurement which is representative of the on-resistance of the P-Channel device. N-MOS provides the pull-down capability when Input is 'LOW', the R_{OL} parameter is a DC measurement which is representative of the on-resistance of the N-Channel device. Both outputs of the MD18023A/B/C-Q1 can deliver 4-A peak source and 7-A peak sink current pulses. The output voltage swings between VDD and VSS providing rail-to-rail operations due to the MOS-output stage which achieves very low drop-out. Additionally, the output channel A of the MD18023A/B/C-Q1 is also isolated from output channel B. The output of one channel is effectively protected from interference from the other.

9.6 Programmable Dead Time (DT) Pin

MD18023A/B/C-Q1 allows the outputs to overlap by connecting this pin directly to VCCI. It is recommended to connect this pin to VCCI, which disables dead time feature and achieves better noi se immunity.

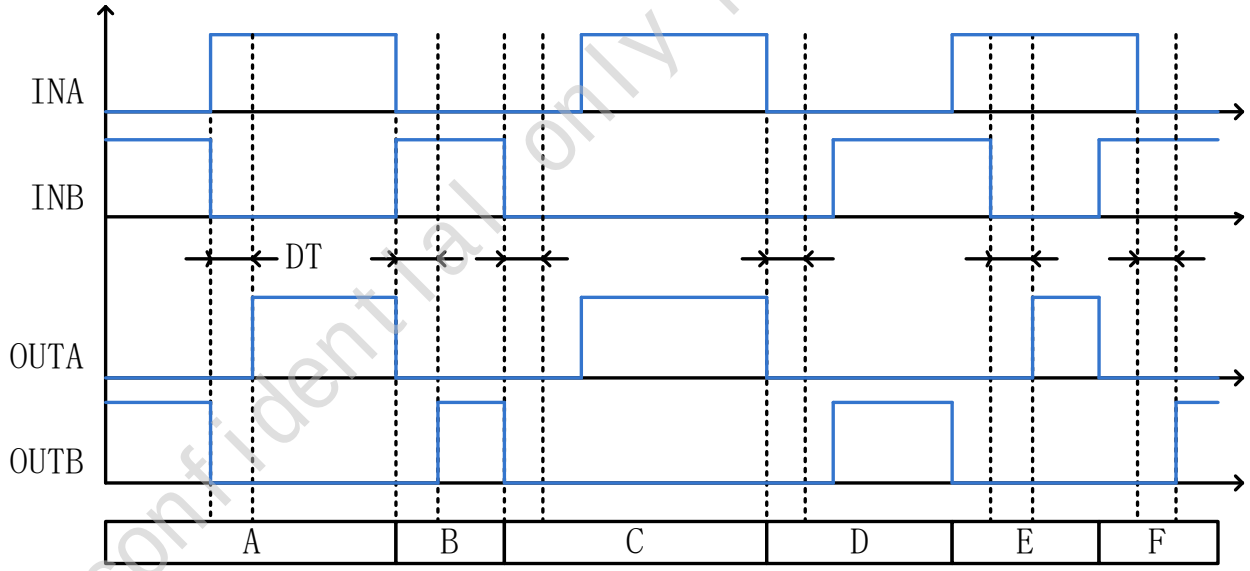
When the DT pin is floating, a large dead time is designed to improve safety and reliability of the system, so as to prevent the dead time from failing due to resistance cold soldering and other reasons. This helps to quickly eliminate the risk of system failure due to too small dead time.

The dead time t_{DT} can be programmed by placing a resistor (R_{DT}) between the DT pin and GNDI. It recommends bypassing this pin with a ceramic capacitor (470 pF or lower) close to DT pin to achieve better noise immunity and better dead time matching between both channels. The appropriate R_{DT} value can be determined from:

$$t_{DT}\ (ns) \approx 12 \times R_{DT}\ (k\Omega)$$

This feature increases the reliability of system, and the recommended value of R_{DT} is between 5kΩ and 200kΩ. When DT pin is shorted to GNDI, MD18023A/B/C-Q1 locks the outputs of both channels with minimum dead time of 40ns.

The programmed deadtime is activated by the input signal's falling edge to prevent shoot-through when the device is designed in an application of high side and low side driver. Various dead time logic operating conditions are illustrated and explained as below.



	Condition	Result
A	INB goes low, INA goes high	INB sets OUTB low immediately and allocates the programmed dead time to OUTA. OUTA is permitted to go high after the programmed dead time has ended.
B	INB goes high, INA goes low	INA sets OUTA low immediately and allocates the programmed dead time to OUTB. OUTB is permitted to go high after the programmed dead time has ended.
C	INB goes low, INA remains low	INB sets OUTB low immediately and allocates the programmed dead time for OUTA. In this case, the inherent dead time of input signal is longer than the programmed dead time. Therefore, when INA goes high, it immediately sets OUTA high.
D	INA goes low, INB remains low	INA sets OUTA low immediately and allocates the programmed dead time to OUTB. In this case, the input signal dead time is longer than the programmed dead time. When INB goes high after the duration of the input signal dead time, it immediately sets OUTB high.
E	INA goes high, INB and OUTB keep high	To avoid overshoot, OUTB is immediately pulled low by the INA and remains OUTA low. After some time INB goes low and allocates the programmed dead time to OUTA. OUTB is already low. After the programmed dead time, OUTA goes high.
F	INB goes high, INA and OUTA keep high	To avoid overshoot, OUTA is immediately pulled low by INA and keeps OUTB low. After some time, INA goes low and allocates the programmed dead time to OUTB. OUTA is already low. After the programmed dead time, OUTB goes high.

10. Application and Implementation

10.1 Application Information

The MD18023A/B/C-Q1 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the MD18023A/B/C-Q1 (with up to 24-V VCCI and 28-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for IGBTs or Si/SiC MOSFETs. With integrated components, advanced protection features (UVLO, dead time, and disable) and optimized switching performance, the MD18023A/B/C-Q1 enable designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

10.2 Typical Application

Figure 27 shows an example which uses two supplies (or single-input-double-output power supply). Power supply V_1 determines the positive drive output voltage and V_2 determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies. However, it provides more flexibility when setting the positive and negative voltage rails.

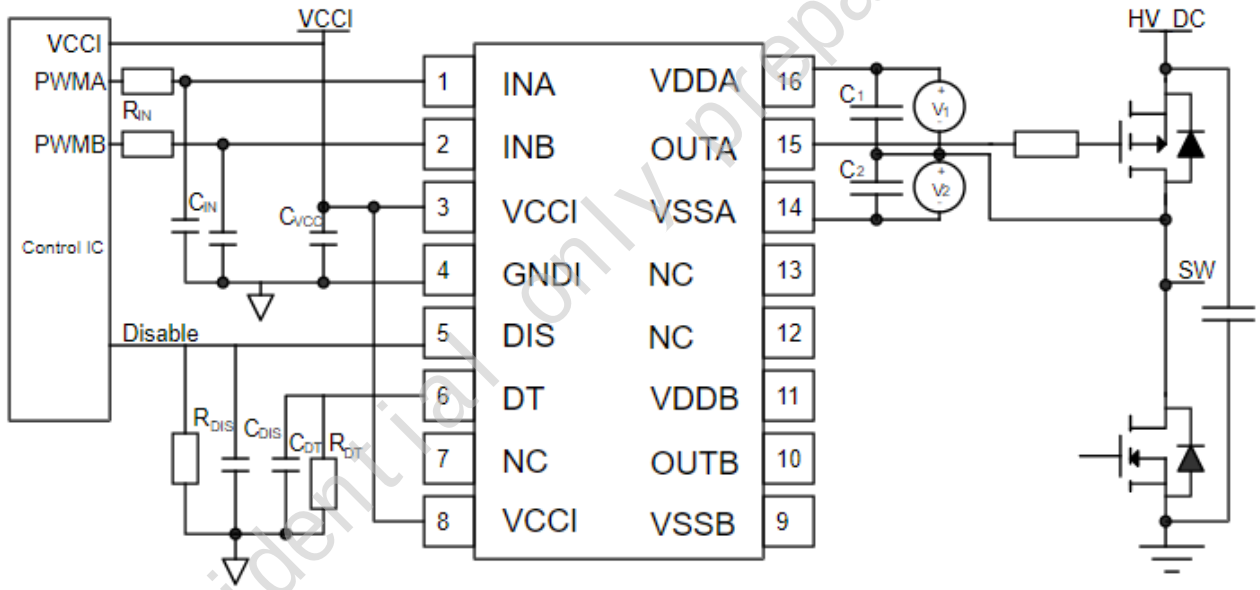


Figure 27. Application Circuit

11. Layout

11.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the MD18023A/B/C-Q1. Some key guidelines are:

• **Component placement:**

– Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GNDI pins and between VDD and VSS pins to suppress switching spikes and to support high peak currents when turning on the external power devices.

– To avoid larger negative transient spikes on the VSS pins connected to the switch node, the parasitic inductances between the source of the top power device and the source of the bottom power device must be minimized.

– It is recommended to place the dead-time setting resistor, R_{DT}, and its bypassing capacitor close to DT pin of the MD18023A/B/C-Q1.

– It is recommended to bypass using a 1nF low ESR/ESL capacitor, C_{DIS}, close to DIS pin when connecting to a micro controller with distance.

• **Grounding considerations:**

– Limiting the high peak currents that charge and discharge the gates of the power devices to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the power devices. The gate driver must be placed as close as possible to the power devices.

• **High-voltage considerations:**

– To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended to prevent contamination that may compromise the isolation performance.

• **Thermal considerations:**

–Increasing the PCB copper connection to the VDD and VSS pins is recommended, with priority on maximizing the connection to VSS. However, the previously mentioned high-voltage PCB considerations must be maintained.

–If the system has multiple layers, we also recommend connecting the VDD and VSS pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no overlapping between traces or coppers from different high voltage planes.

11.2 Layout Example

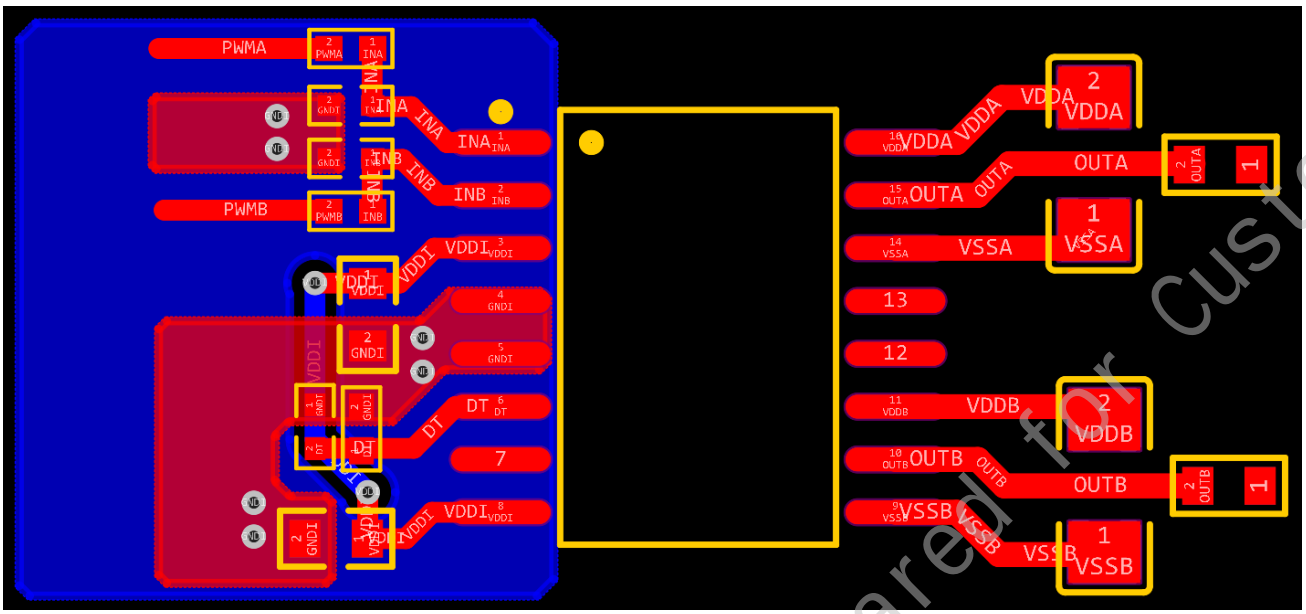


Figure 28. Layout Example

12. Mechanical Data and Land Pattern Data

12.1 SOW16(300mil)

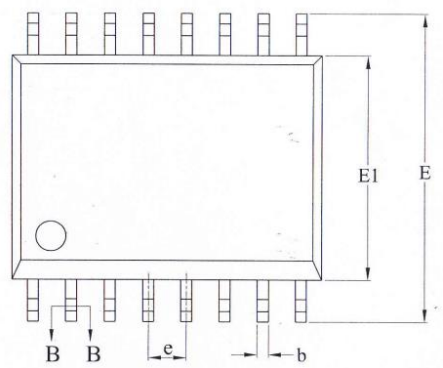


Figure 29. Top View

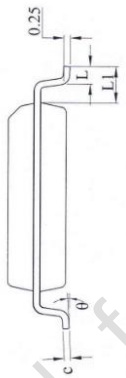


Figure 30. Side View

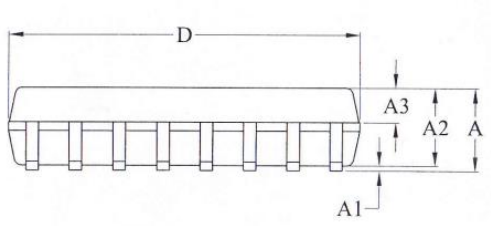


Figure 31. Side View

Symbol	Dimensions In Millimeters	
	MIN	MAX
A	-	2.65
A1	0.10	0.30
A2	2.25	2.35
b	0.35	0.43
c	0.25	0.29
D	10.20	10.40
E	10.10	10.50
E1	7.40	7.60
e	1.27(BSC)	
L	0.55	0.85
θ	0°	8°

12.2 SOP16(150mil)

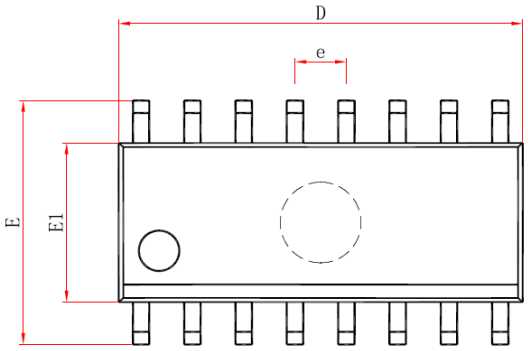


Figure 32. Top View

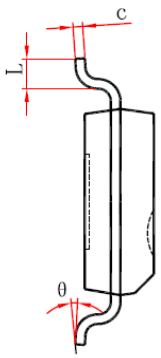


Figure 33. Side View

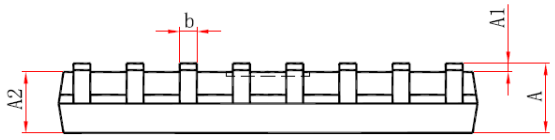


Figure 34. Side View

Symbol	Dimensions In Millimeters	
	MIN	MAX
A	-	1.75
A1	0.10	025
A2	1.30	1.50
b	0.33	0.51
c	0.17	0.25
D	9.80	10.20
E	5.80	6.20
E1	3.80	4.00
e	1.27(BSC)	
L	0.4	1.27
θ	0°	8°

12.3 Land Pattern Data

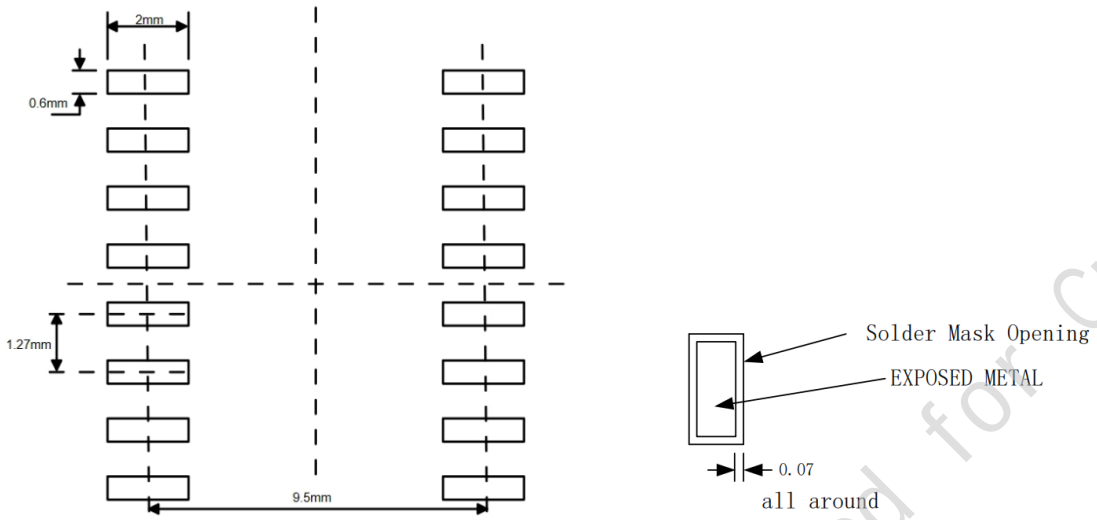


Figure 35. SOW-16 Land Pattern Data

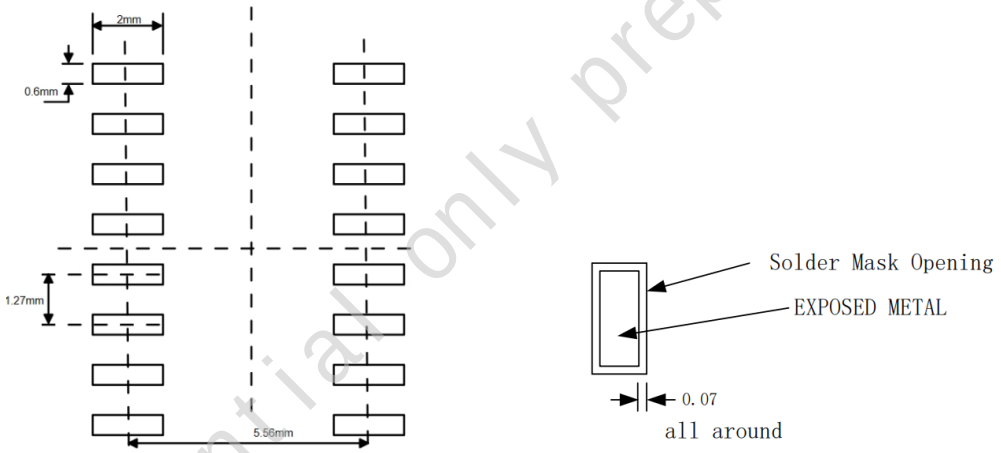


Figure 36. SOP-16 Land Pattern Data

13. Reel and Tape Information

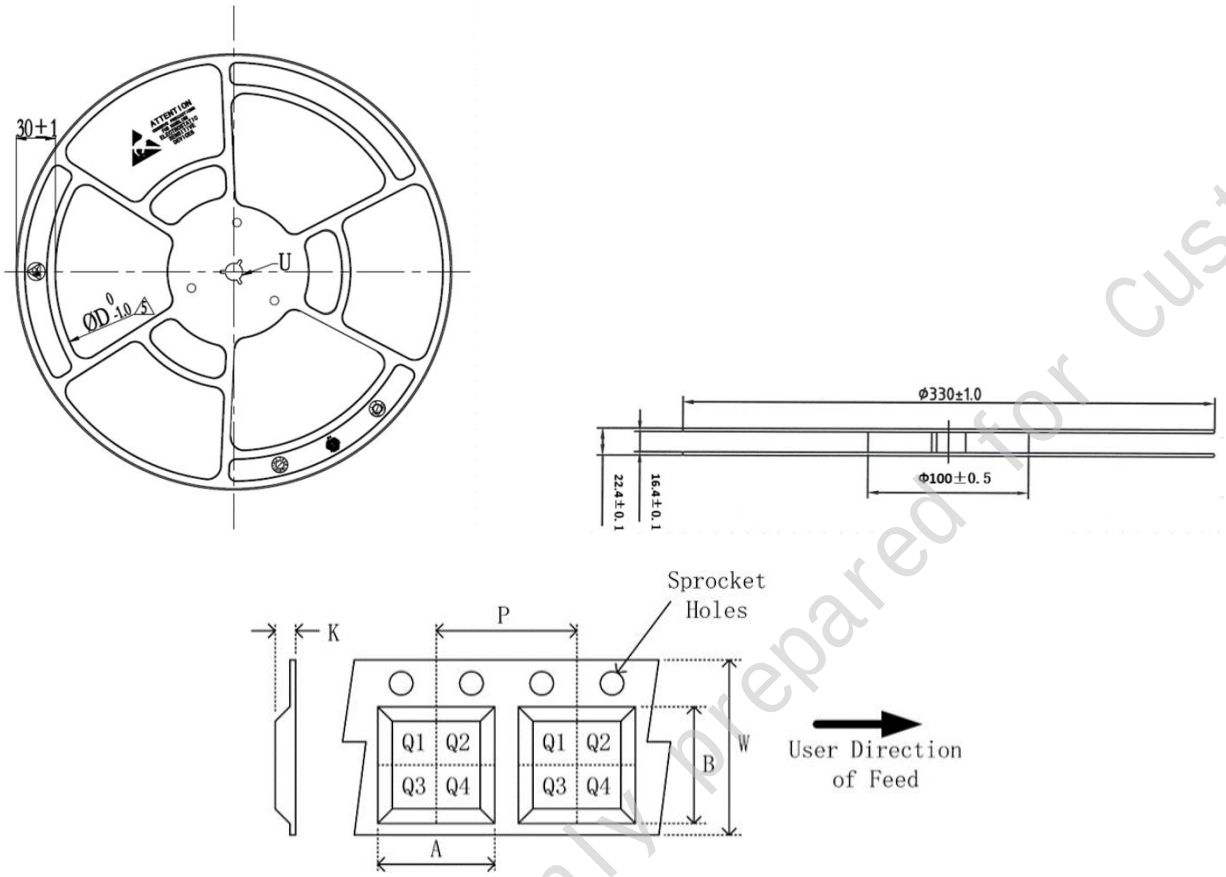


Figure 37. Reel Dimensions

Devise	Package Type	Pins	SPQ (pcs)	A(mm)	B(mm)	K(mm)	P(mm)	W(mm)	Pin1 Quadrant
MD18023A/B/CNAC-Q1	SOP16	16	3000	6.7±0.1	10.4 ±0.1	2.1±0.1	8±0.1	16±0.3	Q1
MD18023A/B/CWAC-Q1	SOW16	16	1500	10.9±0.1	10.8 ±0.1	3.0±0.1	12 ±0.1	16±0.3	Q1

14. Tape and Reel Box Dimensions

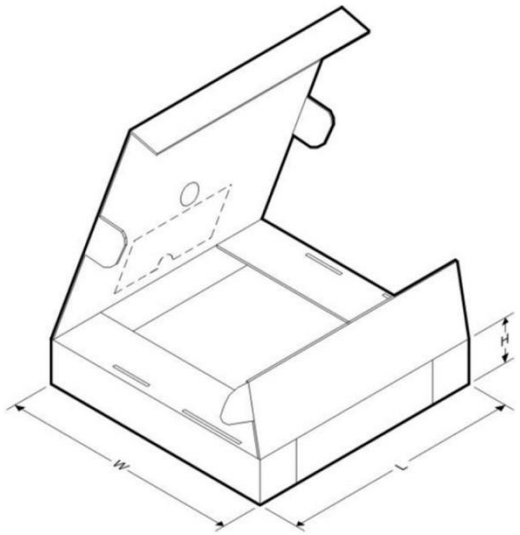


Figure 38. Box Dimensions

Device	Package Type	Pins	SPQ (pcs)	Length(mm)	Width(mm)	Height(mm)
MD18023A/B/CNAC-Q1	SOP16	16	6000	360	360	65
MD18023A/B/CWAC-Q1	SOW16	16	3000	360	360	65