Ultra-Fast Turn-off Synchronous Rectifier Controller

1. Description

The MK91816 is a compact secondary side synchronous rectifier controller and driver for high frequency and high-performance flyback converters. It is compatible with DCM, CCM and QR operations.

The MK91816 generates its own supply while used in high-side rectification, which eliminates the need of external supply generated by auxiliary winding of the transformer.

The extremely low 10ns turn−off propagation delay time and high sink current (~4A) capability of the driver improve SR V_{DS} stress at CCM mode.

The unique VG clamping circuit works well to prevent VG from turning on by fast rising at VD pin with no VCC, that avoids the shoot through between primary side and secondary side during system startup even if the SR VCC is still below 2V.

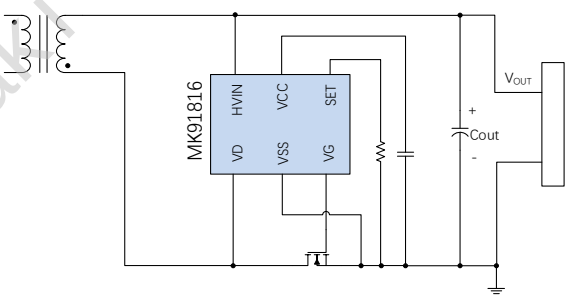
2. Typical Applications

- AC/DC Adapters for Mobile Phone and Notebook
- High Power density AC/DC Power Supplie

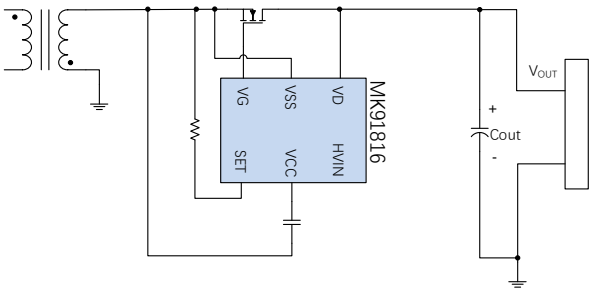
3. Features

- Operates in a Wide Output Voltage Range Down to Zero Voltage
- Self-supply for Operation with Low Output Voltage and/or High–side Rectification without an Auxiliary Winding
- Gate Drive Clamp Voltage is Up to 9.5V
- 10ns Fast Turn-off and 25ns Turn-on Delay
- Programable Minimum on time to support wide frequency range
- VD/HVIN Pin Supports Negative Voltage Spikes Down to -3V
- VG Clamping Circuit works well for low Vth Value of MOSFET
- Optimized for up to 1MHz Frequency
- Supports Active Clamp Flyback with GaN FET or Super-junction MOSFET at Primary Side
- Supports DCM, QR and CCM Operations
- Supports both High-side and Low-side Rectification
- Adaptive Gate Drive for Maximum Efficiency
- SOT23-6 Package Available

4. Simplified Application



Used in low side rectification

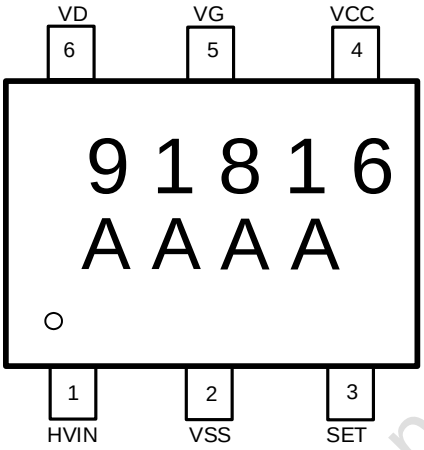


Used in high side rectification

5. Ordering Information

Ordering No.	Description
MK91816CSA	SOT23-6, 3000 pcs/reel

6. Pin Configuration and Marking Information



AAAA: Lot Code

SOT23-6

Absolute Maximum Ratings (1)

VCC, VG, SET to VSS ..... –0.3V to +20V
VD to VSS..... –1V to +155V
HVIN to VSS ..... –1V to +115V
VD to VSS..... –3V to +165V (2)
HVIN to VSS……-3V to 120V (2)
Operating Junction Temperature…-40 to +150℃
Lead Temperature…….. +260℃
Storage Temperature…….. -65℃ to +150℃

Recommended Operation Conditions

VCC to VSS…..... ……. .3.6V to 10V
VD to VSS……..-0.7V to 150V
HVIN to VSS……-0.7V to 100V
Maximum Junction Temp. (T_J) .....+125°C

Thermal Resistance (3)

	Θ_{JA}	Θ_{JC}
SOT23-6.....	100	66 °C/W

Notes:

(1) Exceeding these ratings may damage the device.

(2) Repetitive pulse< 200ns

(3) Measured on JESDSD51-7, 4 layers PCB

7. Electrical Characteristics

T_A=25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Management						
VCC UVLO Rising	$VCC_{\_ON}$		4.44	4.7	4.94	V
VCC UVLO Falling	$VCC_{\_OFF}$		3.9	4.1	4.25	V
VCC UVLO Hysteresis	$VCC_{\_HYST}$		0.54	0.6	0.7	V
VCC Maximum Charging Current	I_{VCC}	VCC=8V, VD=0V, HVIN=20V	70			mA
		VCC=5V, HVIN=0V, VD=20V	40			mA
VCC Regulation Voltage	$VCC_{\_REG}$	VD= 0V, HVIN=14V	8.3	9.2	9.9	V
		VD= 10V, HVIN=0V	6	6.4	6.8	
Operating Current	I_{CC}	VCC=9V, C_{LOAD}=2.2nF, F_{SW}=100kHz	2.25	2.4	2.9	mA
		VCC=6.5V, C_{LOAD}=2.2nF, F_{SW}=100kHz	1.65	1.8	2.1	mA
Quiescent Current	$I_{q(VCC)}$	VCC=6.5V	140	190	230	μA
Mosfet Voltage Sensing						
V_D–V_{SS} Adjusting Voltage	V_{DS_reg}		-55	-40	-16	mV
Turn-On Threshold (V_D–V_{SS})	V_{ON_th}		-300	-250	-200	mV
Turn Off Threshold (V_D–V_{SS})	V_{OFF_th}		-19	0	15	mV
Turn-On Propagation Delay	T_{D_on}	C_{LOAD} = 0nF, VD step down from 3V to -0.5V in 5ns, measure VG rising to 1V	10	25	40	ns
Turn-Off Propagation Delay	T_{D_off}	C_{LOAD} = 0nF, VD step up from -0.5V to 3V in 5ns, measure VG falling to 90% of V_{G-H}	4	10	15	ns
Turn On Blanking Time	T_{B_ON}	R_{SET}=0ohm, C_{LOAD} = 2.2nF	0.35	0.45	0.56	us
	T_{B_ON}	R_{SET}=VCC, C_{LOAD} = 2.2nF	0.9	1.05	1.2	us
Turn Off Blanking V_{DS} Threshold in T_{B_ON}(1)	V_{B_OFF}			2		V
Turn Off Blanking Time	T_{B_OFF}	C_{LOAD} = 2.2nF	250		350	ns
Gate Driver						
V_G (Low)	VG_L	ILOAD= 100mA		0.1	0.3	V

V_G (High)	VG_H	ILOAD= 100mA	VCC-0.6	VCC-0.3		V
Maximum Source Current(1)	IVG_H			1		A
Maximum Sink Current(1)	IVG_L			4		A
Pull Down Impedance(1)	R_{SINK}	ILOAD= 100mA		0.53		Ω

Note:

(1) Values are verified by characterization on bench, not tested in production

8. Pin Functions

Pin #	Name	Description
1	HVIN	HV Linear Regulator Input
2	VSS	Ground, also used as FET source sense reference for VD
3	SET	Programming for GATE minimum turn on time
4	VCC	Linear Regulator Output, supply MK91816
5	VG	Gate drive output
6	VD	FET drain voltage sense; HV pulse LDO input

9. Block Diagram

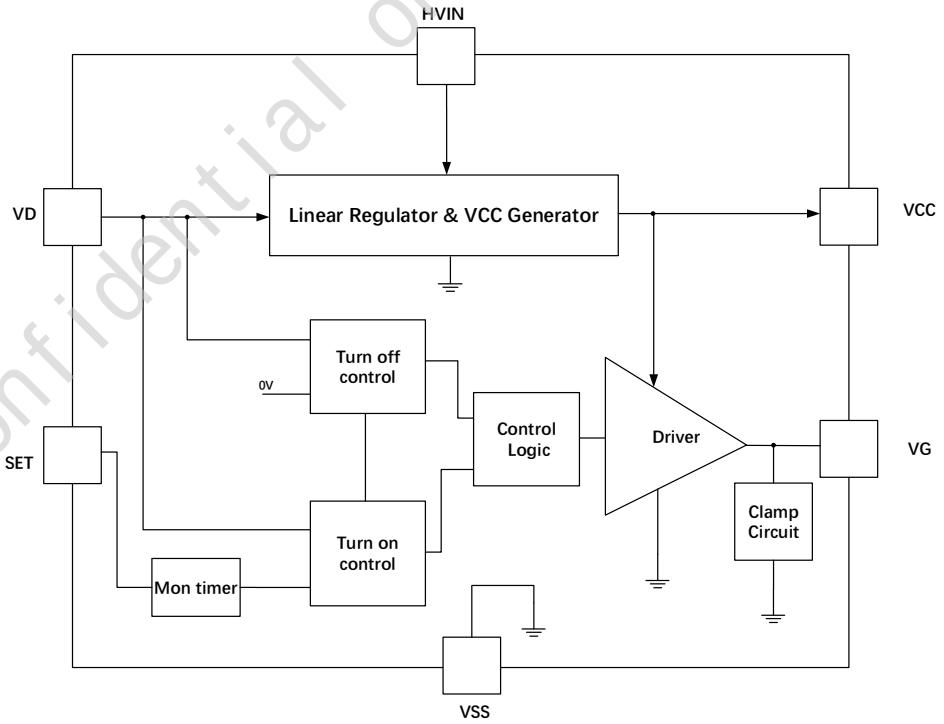


Figure 1. Functional Block Diagram

10. Operation Descriptions

The MK91816 is an advanced secondary side synchronous rectifier controller and driver for high frequency and high performance flyback converters, which supports DCM, CCM and QR operations. The extremely low 10ns turn−off propagation delay time and high sink current (~4A) capability of the driver improve SR V_{DS} stress at CCM mode, particularly at the conditions of startup and V_{OUT} shorting to ground. The unique VG clamping circuit works well to prevent VG from turning on by fast rising at VD pin with no VCC, that avoids the shoot through between primary side and secondary side during system startup.

Vcc and Startup

In order to reduce switching and conduction loss with wide range of voltage threshold Vth of MOSFETs, MK91816 provides the flexibility of different VG voltage. VCC is regulated at 9.5V which supplies MK91816 including VG when connect HVIN pin to a voltage source higher than 9.8V. Here the source for HVIN pin can be a DC voltage such as V_{OUT} for low side rectification or an AC voltage such as the DRAIN of SR MOSFET. The average maximum charging current is 62mA while VCC is regulated from HVIN voltage source. Be noted the voltage applied to HVIN pin is self-limited with <100mA DC and 1A pulse after exceeding 120V, and VD pin is self-limited with <100mA DC and 1.5A pulse after exceeding 160V.

When the voltage on HVIN pin is below 9.5V but above 6.2V, VCC follows HVIN with dropout voltage depending on the load current at VCC, until HVIN drops to around 6.2V. Once HVIN drops around 6.2V, a 45mA current source from VD starts charging up VCC and regulating it at 6.2V.

The typical system implementations with different bias connections are shown below. A 0.1uF to 1uF bypass capacitor is suggested at VCC pin.

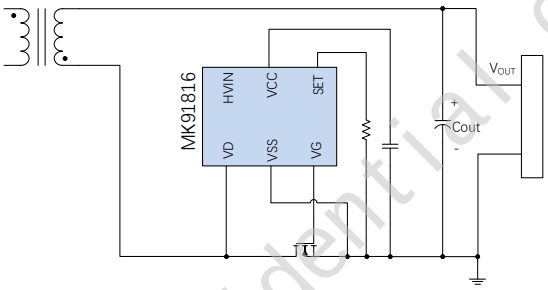


Figure 2. Low-side Rectification 2, $VCC_{\_REG}$=6.2V

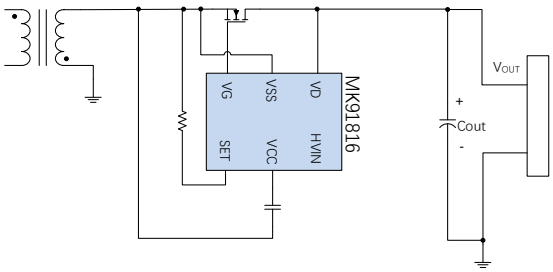


Figure 3. High-side Rectification 2, $VCC_{\_REG}$=6.2V

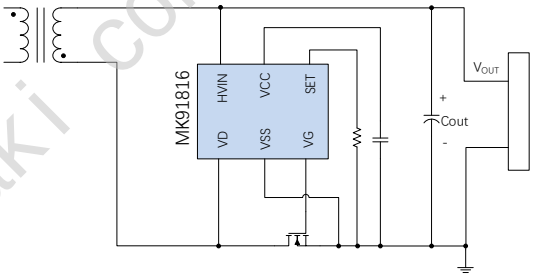


Figure 4. Low-side Rectification 3, $VCC_{\_REG}$=6.2V to 9.5V[1]

Note:

(1) In Low-side Rectification 4, VCC is supplied by VD and regulated at 6.2V if V_{OUT} is lower than 6.2V; VCC is regulated at 9.5V through HVIN if V_{OUT} voltage is larger than 9.8V; VCC is close to V_{OUT} while V_{OUT} is between 6.2V and 9.5V, which generated by HVIN path.

Pay attention to the voltage stress when connecting HVIN to Drain of SR MOS, as HVIN pin withstands less voltage rating than VD pin. To achieve 9V VCC, and lower HVIN voltage stress, below connections should be considered.

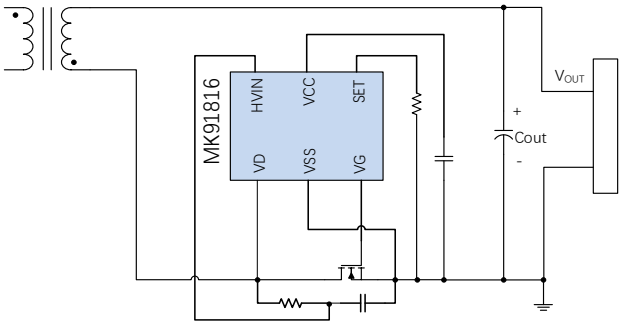


Figure 5. Low-side Rectification, $VCC_{\_REG}$=9V

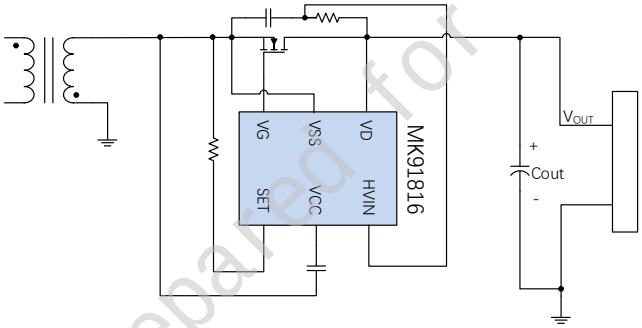


Figure 6. High-side Rectification, $VCC_{\_REG}$=9V

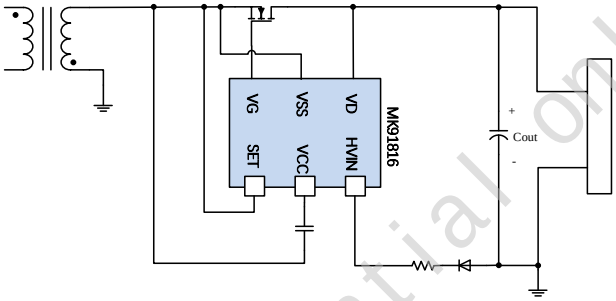


Figure 7. High-side Rectification, $VCC_{\_REG}$=9V

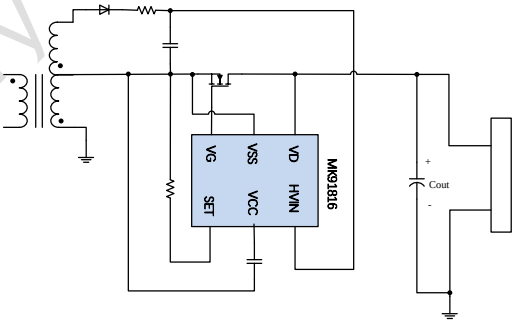


Figure 8. High-side Rectification, $VCC_{\_REG}$=9V

Conduction Phase

After SR VG turns on, a minimum blanking time T_{B_ON} is required to prevent the parasitic ringing from falsely turning off SR VG. The minimum turn-on blanking time programed by Rset for MK91816, during which the turn off threshold is increased to 2V. Right before T_{B_ON} timer expires, MK91816 starts monitoring V_{DS} against a -40mV value to determine if VG needs to be slowly discharged. This operation adjusts V_{DS} of SR MOSFET to be around -40mV until the current through SR MOSFET drops to zero. In CCM mode, VG is prepositioned to be lower than VCC so that VG is turned off even faster; In DCM/QR mode, this V_{DS} adjusting design makes V_{DS} cross 0V exponentially faster, which combines with the 10ns turn-off propagation delay to make turn-off timing more accurately regardless of the accuracy of turn-off threshold.

Turn Off Phase

Within the minimum turn-on blanking time T_{B_ON}, V_{DS} turn-off threshold is 2V which is the same as V_{B_OFF}. After the minimum turn-on blanking time T_{B_ON}, the turn-off threshold is decided by $T_{B\_ON,}$ that combines with extremely fast 10ns turn-off propagation delay and 4A VG pull-down (sinking) current, synchronous rectifier is able to be turned off not too early which causes more SR FET body diode conduction time and more negative turn-off ringing, or not too late which creates risk of shoot through between primary side and SR side in CCM mode.

Minimum On Time Programming

The turn on blanking time (T_{B_ON}) is programmed by SET pin, T_{B_ON} =(20/3)*(Rset(k)+60) ns, where Rset is in the range of 10k to 310k. Rset is connected between SET pin and VSS pin. when Rset is smaller than 10k, T_{B_ON} is fixed to 400ns. when Rset is 310k, T_{B_ON} is ~2.5us. If SET PIN is floating(or Rset≥340k), then T_{B_ON} is around 1us.

11. PCB Layout Recommendations

The PCB layout guidance are shown below:

1. The trace from VG pin to the GATE of SR MOSFET needs to be as short as possible. The VSS pin to the SOURCE of SR MOSFET needs to route with short and wide trace
2. The sense loop (VD pin and VSS pin) is as small as possible
3. In two-layer boards, avoid fast dv/dt traces underneath MK91816, such as the DRAIN of SR MOSFET network

12. Package Information (SOT23-6)

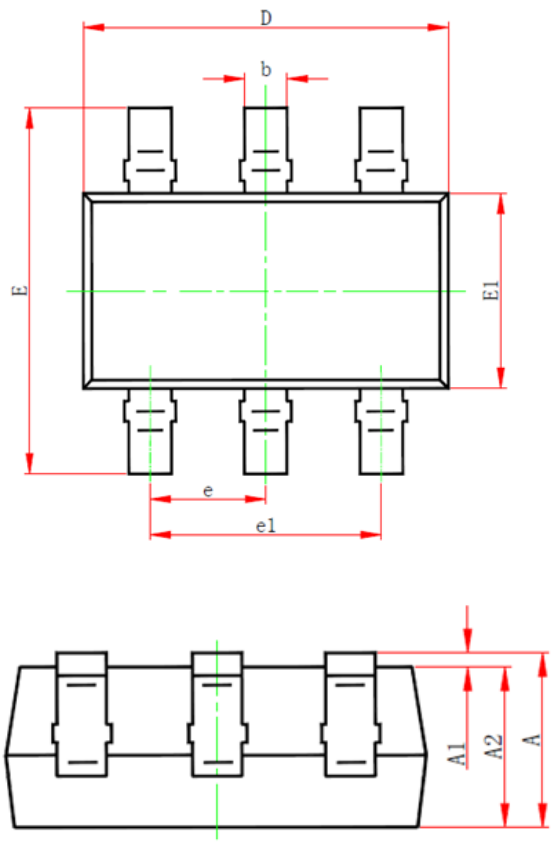


Figure 9. Package Information

Symbol	Dimensions In Millimeters	
	MIN	MAX
A	1.05	1.25
A1	0.00	0.10
A2	1.05	1.15
b	0.30	0.50
c	0.10	0.20
D	2.82	3.02
E	2.65	2.95
E1	1.50	1.70
e	0.95(BSC)	
L	0.30	0.60
θ	0°	8°

13. Tape and Reel Information

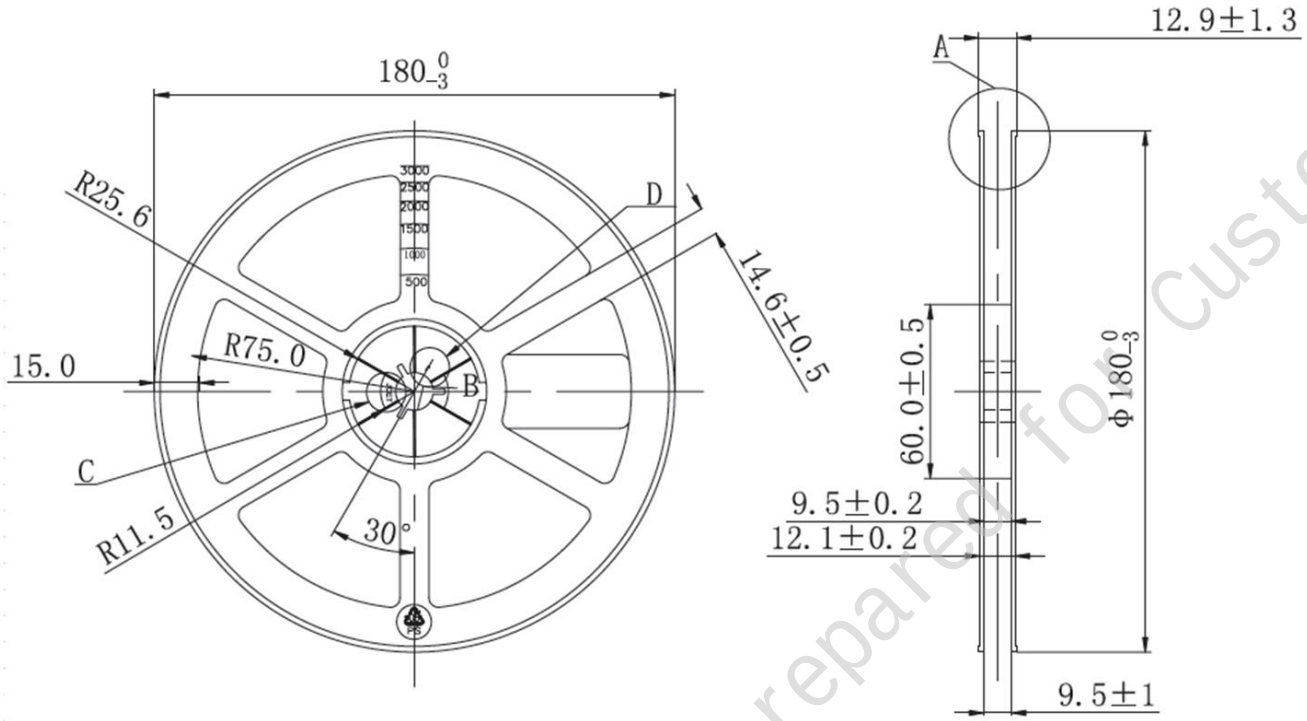


figure 10. reel dimensions

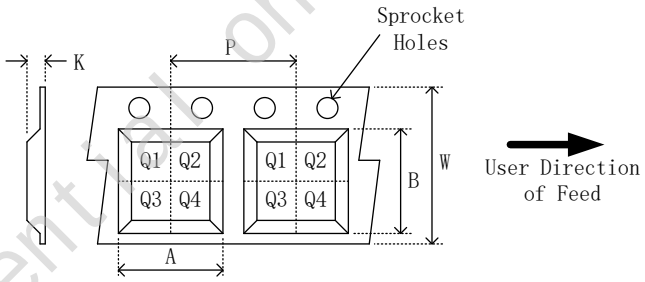


Figure 11. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	W (mm)	Pin1 Quadrant
MK91816CSA	SOT-23-6L	6	3000	3.23±0.1	3.17±0.1	1.37±0.1	4±0.1	8±0.1	Q3

14. Tape and Reel Box Dimensions

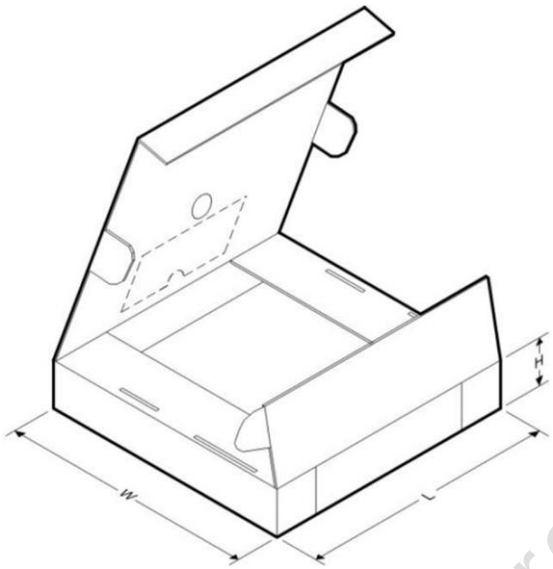


Figure 12. Box Dimensions

Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MK91816CSA	SOT-23-6L	6	30000	203	203	195