Single-Channel Smart High-Side Power Switch

1. Description

The MS1810-Q1 is a Smart High-Side Power Switch, which has built-in over load protection function, over temperature protection function, open load detection function and under voltage lockout function.

An enable pin controls whether diagnostics are turned on or not. A high-precision current sensor ensures that the load current can be satisfied in the range of 100mA-10A.

The MS1810-Q1 is offered in eTSSOP-20 packages.

2. Typical Applications

- All types of Automotive resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Driving capability suitable for 10A loads and high inrush current loads such as 4 x P21W lamps or equivalent electronic loads (e.g. LED modules)

3. Features

- High-Side Switch with Diagnosis and Embedded Protection
- Qualified for automotive applications. Product validation according to AEC-Q100 Grade 1.
- On-state resistance:15mΩ
- Absolute and dynamic temperature limitation with controlled restart
- Over load protection (tripping) with Intelligent Restart Control
- VS under voltage shutdown
- VS over voltage protection
- Proportional load current sense
- Diagnosis of Open Load in OFF state

4. Typical Application Circuit

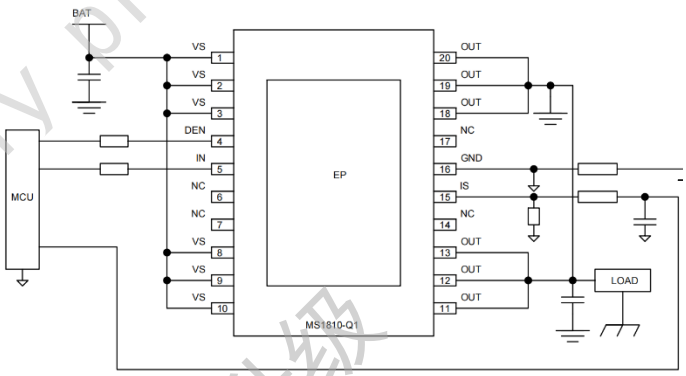

Figure 1. Typical Application Diagram

5. Ordering Information

Order Code	Package	Pins	Description
MS1810AAL-Q1	ETSSOP-20	20	MSL-3,4500 pcs/ reel

6. Package Reference and Pin Functions

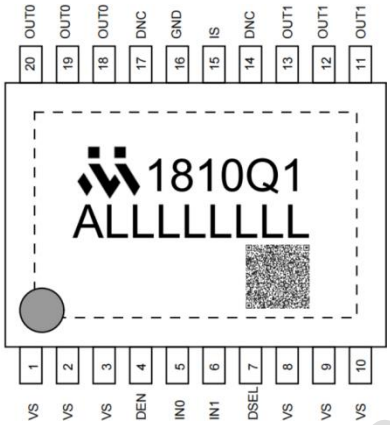

Figure 2. Pin Function (top view)

Pin #	Name	Description
EP	\	**Thermal Pad** Connect to Power ground
1,2,3,8,9,10	VS	**Supply Voltage** Battery voltage
4	DEN	**Diagnostic Enable** Digital signal to enable device diagnosis (“high” active) and to clear the protection counter of the selected channel by DSEL pin If not used: recommend to connect with a 10 kΩ resistor to module ground
5	IN	**Input Channel** Digital signal to switch ON Channel (“high” active) If not used: recommend to connect with a 10 kΩ resistor to module ground
6,7,14,17	NC	Not connected, internally not bonded
11,12,13,18,19,20	OUT	**Output** Protected high-side power output of Channel
15	IS	**Sense current & Fault output** Analog/digital signal for diagnosis If not used: left open
16	GND	**Ground** Signal ground

7. Specifications

7.1 Absolute Maximum Ratings

Parameter		Min	Max	Units
Power Supply Voltage	VS-GND	-16	35 (2)	V
Reverse Polarity Voltage	$-V_{S(REV)}$	-	16	V
Voltage at DI Pin	V_{DI} (1)	-16	35 (2)	V
Voltage at IS Pin	V_{IS}	-1.5	V_S	V
Current through GND Pin	I_{GND}	-25	25	mA
Current through IS Pin	I_{IS}	-25(2)	15	mA
Load Current	$\|I_L\|$	-	10	A
Maximum Energy Dissipation Single Pulse	E_{AS}	-	38	mJ
Maximum Energy Dissipation Repetitive Pulse	E_{AR}	-	18	mJ
Operating Junction Temperature (T_J)		-40	150	°C
Storage Temperature		-55	150	°C

Notes:

(1) Logic & control pins (Digital Input = DI), DI = IN, DEN, DSEL

(2) Continues time t<2min

7.2 Recommend Operation Conditions (1)

Parameter		Min	Max	Units
Power Supply Voltage	V_S	6	28	V
Supply Voltage Range for Normal Operation	$V_{S(NOR)}$	6	18	V
Digital Input	IN, DEN, DSEL	2.5	5.5	V
Operating Junction Temperature (T_J)		-40	150	°C
Storage Temperature		-55	150	°C

Note:

(1) The device is not guaranteed to function outside of its operating conditions.

7.3 Thermal Resistance

Parameter		Value	Units
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient	28.4	°C/W
$R_{\theta JC\_BOT}$	Thermal Resistance Junction-to-Case (simulated at exposed pad)	1.3	°C/W
$R_{\theta JC\_TOP}$	Thermal Resistance Junction-to-Case	27	°C/W

Note:

(1) According to Jedec JESD51-2, JESD51-5, JESD51-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 × 35 μm copper layers. Simulation done at T_A = 105° C，$P_{DISSIPATION}$ = 1W

7.4 ESD Ratings

		Value	Units
Electrostatic discharge V_{ESD}	ESD Susceptibility all Pins (HBM) (1)	±2000	V
	ESD Susceptibility all Pins (CDM) (2)	±2000	V
	ESD Susceptibility Corner Pins (CDM) (2)	±750	V

Notes:

(1) ESD susceptibility, Human Body Model "HBM", according to AEC Q100-002.

(2) ESD susceptibility, Charged Device Model "CDM", according to AEC Q100-011.

7.5 Electrical Characteristics

Unless otherwise noted, all typical values are at V_S=13.5V, T_J=25℃. All min and max specifications are at recommended operating conditions V_S=6V to 18V, T_J =–40°C to 140°C. Typical resistive loads connected to the outputs for testing (unless otherwise specified): R_L = 3.3 Ω, C_L=0uF.

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply Voltage						
Power Supply Undervoltage Shutdown	$V_{S(UV)}$	3.5	3.8	4.1	V	V_S decreasing IN = "high" From V_{DS} ⩽ 0.5 V to V_{DS} = V_S See **Figure 9**
Power Supply Minimum Operating Voltage	$V_{S(OP)}$	4.4	4.7	5.0	V	V_S increasing IN = "high" From V_{DS} = V_S to V_{DS} ⩽ 0.5 V See **Figure 9**
Power Supply Undervoltage Shutdown Hysteresis	$V_{S(HYS)}$	-	0.9	-	V	$V_{S(OP)}$ – $V_{S(UV)}$ See **Figure 9**
Power Supply Undervoltage Recovery Time	$t_{DELAY(OP)}$	-	50	100	µs	dV_S/dt ⩽ 3 V/µs See **Figure 9**
Reverse Polarity Voltage	$-V_{BAT(REV)}$	-	-	16	V	t < 2min R_L = 3.3Ω See **Figure 20**
Supply Current						
Power Supply Current Consumption in Sleep Mode	$I_{VS(SLEEP)\_25℃}$	-	7	9	µA	V_S = 18V@25℃ DEN = IN = "low"
Operating Current in Active Mode (all Channels ON)	$I_{GND(ACTIVE)}$	-	4.0	6.5	mA	V_S = 13.5V DEN = IN = "high"
Operating Current in Standby Mode	$I_{GND(STBY)}$	-	4.0	6.5	mA	V_S = 13.5V DEN = "high" IN = "low"

Digital Input						
Digital Input Voltage Threshold	$V_{DI(TH)}$	0.8	1.3	1.8	V	See **Figure 4**
Digital Input Hysteresis	$V_{DI(HYS)}$	-	0.3	-	V	See **Figure 4**
Digital Input Current ("high")	$I_{DI(H)}$	-	10	15	uA	V_{DI} = 2 V
Digital Input Current ("low")	$I_{DI(L)}$	-	2	10	uA	V_{DI} = 0.8 V
Switching Characteristics						
Switch-ON Delay	$t_{ON(DELAY)}$	10	35	60	µs	V_S = 13.5 V, DEN = high From IN=$V_{DI(TH)}$ to V_{OUT} = 10% V_S See **Figure 11**
Switch-OFF Delay	$t_{OFF(DELAY)}$	10	25	50	µs	V_S = 13.5 V, DEN = high From IN=$V_{DI(TH)}$ -$V_{DI(HYS)}$ to V_{OUT} = 90% V_S See **Figure 11**
Switch-ON Time	t_{ON}	30	60	110	µs	V_S = 13.5 V, DEN = high From IN=$V_{DI(TH)}$ to V_{OUT} = 90% V_S See **Figure 11**
Switch-OFF Time	t_{OFF}	25	50	100	µs	V_S= 13.5 V, DEN = high From IN=$V_{DI(TH)}$ -$V_{DI(HYS)}$ to V_{OUT} = 10% V_S See **Figure 11**
Switch-ON/OFF Matching t_{ON} - t_{OFF}	Δt_{SW}	-20	10	40	µs	V_S =13.5 V
Switch-ON Slew Rate	$(dV/dt)_{ON}$	0.3	0.6	0.9	V/µs	V_{OUT} = 30% to 70% of V_S See **Figure 11**
Switch-OFF Slew Rate	$-(dV/dt)_{OFF}$	0.3	0.6	0.9	V/µs	V_{OUT} = 70% to 30% of V_S See **Figure 11**
Slew Rate Matching $(dV/dt)_{ON}$ - $(dV/dt)_{OFF}$	$\Delta(dV/dt)_{SW}$	-0.1	0	0.2	V/µs	V_S = 13.5 V
ON-State Resistance						
ON-State Resistance in Cranking	$R_{DS(ON)\_CRANK}$	-	16	30	mΩ	V_S = 4V I_L = 2.8A

ON-State Resistance at T_J = 25℃	$R_{DS(ON)\_25℃}$	-	15	18	mΩ	V_S =13.5V T_J = 25℃, I_L = 2.8A
ON-State Resistance at T_J = 150℃	$R_{DS(ON)\_150℃}$	-	24	28	mΩ	2) V_S =13.5V T_J = 150℃, I_L = 2.8A
Drain Source Diode Voltage	$V_{DS(DIODE)}$	-	0.7	1	V	I_L = 190mA T_J = 150℃
Current Sense Ratio						
Current Sense Ratio at I_L = 100mA-500mA	k_{ILIS1}	-10%	5200	+10%		See **Figure 6**
Current Sense Ratio at I_L = 500mA-1A	k_{ILIS2}	-5%	5200	+5%		See **Figure 6**
Current Sense Ratio at I_L = 1A-10A	k_{ILIS3}	-3%	5200	+3%		See **Figure 6**
Protection Characteristics						
Thermal Shutdown Temperature (Absolute)	$T_{J(ABS)}$	160	175	190	℃	1) 2) See **Figure 6**
Thermal Shutdown Hysteresis (Absolute)	$T_{HYS(ABS)}$	-	30	-	℃	1) 2) See **Figure 6**
Thermal Shutdown Temperature (Dynamic)	ΔT_J	60	70	80	℃	1) See **Figure 6**
Thermal Shutdown Hysteresis (Dynamic)	ΔT_{HYS}	-	30	-	℃	1) See **Figure 6**
Over load Detection Current at T_J = -40°C-85°C	I_{LOL1}	-	90	-	A	1) V_{DS} < 4V T_J = -40℃~85℃ See **Figure 17**
Over load Detection Current at T_J = -40°C-85°C	I_{LOL2}	-	50	-	A	1) V_{DS} > 6V T_J = -40℃~85℃ See **Figure 17**
Over load Detection Current at T_J = 150°C	I_{LOL3}	-	80	-	A	1) V_{DS} < 4V T_J = 150℃ See **Figure 18**
Over load Detection Current at T_J = 150°C	I_{LOL4}	-	40	-	A	1) V_{DS} > 6V T_J = 150℃ See **Figure 18**
VS-OUT Clamping Voltage	$V_{DS(CLAMP)}$	30	33.5	37	V	Digital Input =LOW I_{OUT} = 5 mA

OUT-GND Clamping Voltage	$V_{OUT(CLAMP)}$	-	-19	-	V	[2] Digital Input =HIGH I_{OUT} = 5 mA
VS-IS Clamping Voltage	$V_{IS(CLAMP)}$	32	36	40	V	Digital Input =LOW I_{IS} = 5 mA
Counter Reset Delay Time after Fault Condition（DEN）	$t_{RETRY(DEN)}$	70	100	130	us	[2] DEN = “high” See **Figure 23**
Counter Reset Delay Time after Fault Condition（INn）	$t_{RETRY(IN)}$	50	60	70	us	[2] DEN = “low” See **Figure 22**
Diagnosis Characteristics						
SENSE Fault Current	$I_{IS(FAULT)}$	4	5	6.5	mA	See **Figure 5**
SENSE Open Load in OFF Current	$I_{IS(OLOFF)}$	2	2.5	3.5	mA	See **Figure 19**
SENSE Delay Time at Channel Switch ON after Last FaultCondition	$t_{IS(FAULT)\_D}$	-	420	-	us	See **Figure 5**
SENSE Open Load in OFF Delay Time	$t_{IS(OLOFF)\_D}$	100	130	160	us	V_{OUT}>3.5V from IN falling edge to $I_{IS} = I_{IS(OLOFF)}$ See **Figure 19**
Open Load V_{OUT} Detection Threshold in OFF State	$V_{(OLOFF)}$	2	3	3.5	V	See **Figure 19**
SENSE Settling Time with Nominal Load Current Stable	$t_{sIS(ON)}$	-	10	30	us	From DEN rising edge to 0.9*I_{IS}, $I_{IS} = I_L /(k_{ILIS})$ See **Figure 7**
SENSE Disable Time	$t_{sIS(OFF)}$	-	10	30	us	From DEN falling edge to 0.1*I_{IS}, $I_{IS} = I_L /(k_{ILIS})$ See **Figure 7**
SENSE Settling Time after Load Change	$t_{sIS(LC)}$	-	10	40	us	From $I_L = I_{L(CAL)}$ to $I_L = I_{L(CAL)\_H}$ See **Figure 7**

Notes:

（1）Not subject to production test, guarantee by design

（2）Functional test only

8. Detailed Description

8.1 Overview

The MS1810-Q1 is a Smart High-Side Power Switch featuring built-in over load protection, over temperature protection, open load detection and under voltage lockout functions.

An enable pin controls whether diagnostics are turned on or not. A high-precision current sensor ensures accurate sensing of load current within the range of 100mA-10A.

8.2 Block Diagram

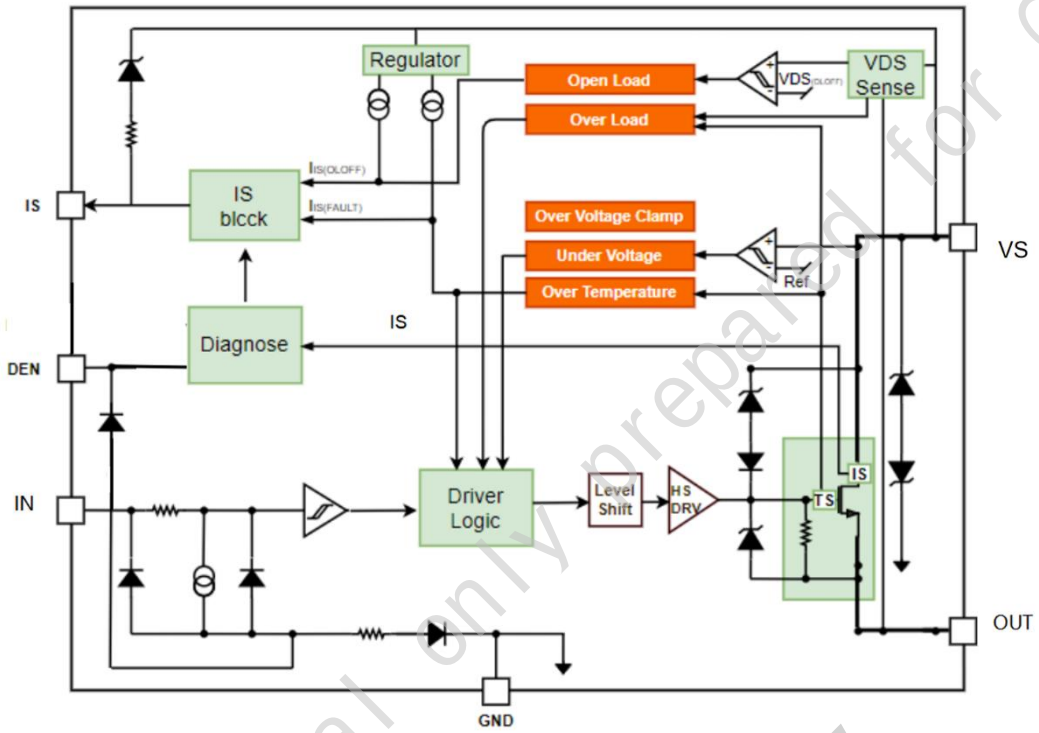

Figure 3. Block Diagram

8.3 Input Pin

In a system with a comparator with hysteresis, the hysteresis helps to prevent rapid switching between the "high" and "low" states when the input signal is close to the threshold voltage. This is achieved by having two distinct threshold voltages for the "high" and "low" states.

The relationship between the two threshold voltages, $V_{DI(TH)}$ and $V_{DI(HYS)}$, can be understood as follows (as shown in **Figure 4**).

When the Digital input voltage V_{DI} is below $V_{DI(TH)}$ - $V_{DI(HYS)}$, the output will be in the "low" state.

When the Digital input voltage V_{DI} is above $V_{DI(TH)}$, the output will be in the "high" state.

When the Digital input voltage V_{DI} is between $V_{DI(TH)}$ - $V_{DI(HYS)}$ and $V_{DI(TH)}$, the output will remain in its current state until the Digital input voltage crosses the other threshold.

The output channel is activated based on the input signals received at IN pin.

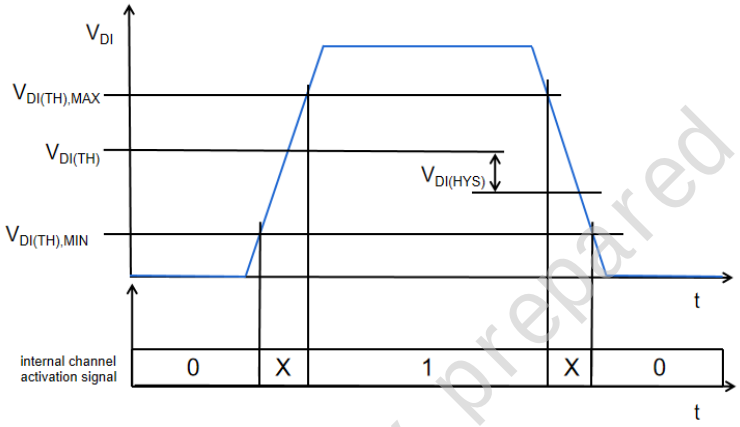

Figure 4. Input Threshold Voltages and Hysteresis

8.4 Diagnosis Enable Pin

When the DEN pin is set to "high", the diagnostic circuitry and protection circuitry are enabled.
When the DEN pin is set to "low", the diagnostic circuitry is disabled, and the IS pin is set to high impedance.
After this period, the I_{IS} is calculated using the formula: $I_{IS} = I_L / k_{ILIS}$, where I_L is the load current and k_{ILIS} is a constant factor (as shown in **Figure 5**).
As long as "hard" failure mode occurs (such as short circuit to GND, over load, over temperature, or open load), $I_{IS(FAULT)}$ is provided by the IS pin if the DEN pin is set to "high".

Table 1. Sense Signal Truth Table

DEN	IS
Low	Z
High	Sense output

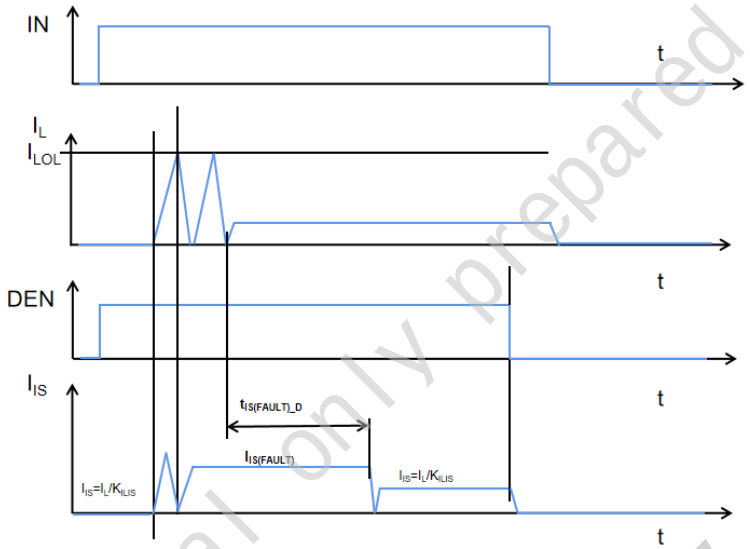

Figure 5. $I_{IS(FAULT)}$ at over load

8.5 Diagnosis Output Pin

The MS1810-Q1 provides a SENSE current denoted as I_{IS} at the IS pin. As long as no "hard" failure mode occurs (such as short circuit to GND, over load, over temperature, or open load), a signal proportional to the load current I_L is provided. The ratio $k_{ILIS} = I_L / I_{IS}$ provides the relationship between the load current and the sensed current. Variations in temperature and load current can affect the accuracy of the sensed current.

When the diagnostic circuitry is disabled by setting the DEN pin to "low", the IS pin is set to high impedance. A sense resistor R_{SENSE} must be connected between the IS pin and module ground if the current sense diagnosis is used. The typical value for R_{SENSE} is 1.0 kΩ. This value is chosen to minimize power loss in the sense circuit and to protect the IS block with current limiting in the event of reverse input.

It is not recommended to connect the IS pin to the sense current output of other devices if they are supplied by a different battery feed. This is due to the internal connection between the IS pin and VS supply voltage.

Refer to **Figure 3** for internal structure information related to the IS pin and its connections.

Refer to **Figure 6** for more detailed information on the accuracy and behavior of the SENSE current with respect to load current.

In summary, the connection of the sense resistor R_{SENSE} and the behavior of the IS pin in relation to diagnostic enabling and load current sensing are crucial aspects of the system operations. Proper consideration of these factors is essential for accurate current sensing and protection in the circuit.

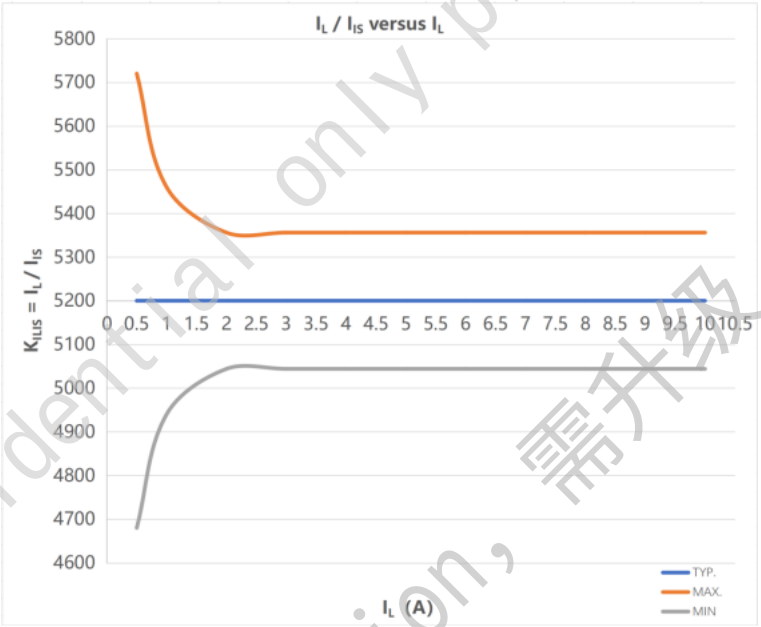

Figure 6. Current Sense accuracy for Nominal Load

Table 2. SENSE Signal, Function of Application Condition

Application Condition	Input Level	DEN Level	VOUT	Diagnostic Output
Normal operation	"low"	"high"	GND	Z
Short circuit to GND			GND	Z
Short circuit to V_S			V_S	$I_{IS(OLOFF)}$
Open Load			V_{OUT} <2V V_{OUT} >3.5V	Z $I_{IS(OLOFF)}$
Inverse current			V_{OUT} >V_S	$I_{IS(OLOFF)}$
Normal operation	"high"		V_S	$I_{IS} = I_L / k_{ILIS}$
Short circuit to GND			GND	$I_{IS(FAULT)}$
Over temperature			GND	$I_{IS(FAULT)}$
Short circuit to V_S			V_S	$I_{IS} < I_L / k_{ILIS}$
Open Load			V_S	0
Inverse current			$V_S = V_{OUT} > V_S$	Z
All conditions	n.a.	"low"	n.a.	Z

The settling time ($t_{sIS(ON)}$) is the duration taken for the SENSE signal to reach a stable and accurate representation of the load current after the DEN pin is enabled. During this settling time, the system may not provide a proper signal as the SENSE signal is still stabilizing.
The disabling time ($t_{sIS(OFF)}$) is required for the SENSE signal to deactivate or become unreliable after the DEN pin is disable.
The settling timing ($t_{sIS(LC)}$) is from a change in load current to the SENSE signal to reach a stable and accurate representation of the load current (as shown in **Figure 7**).

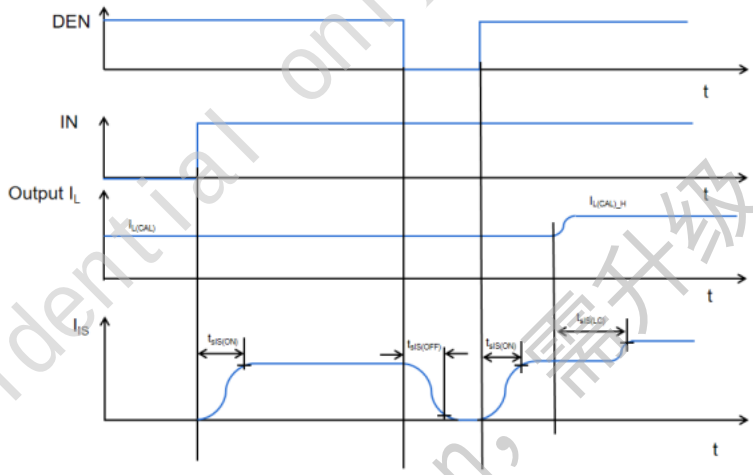

Figure 7. SENSE Settling / Disabling Timing and Load Change

8.6 Operation Mode

MS1810-Q1 has the following operating modes:

• Sleep Mode: In this mode, the device is in a low-power state, and the output channels are disabled. The current consumption at the VS pin is measured by $I_{VS(SLEEP)}$.

• Stand-by Mode: This mode represents a state between Sleep and Active modes, where the device is partially active but not fully operational. The current consumption at the VS pin is measured by $I_{GND(STBY)}$.

• Active Mode: This mode indicates that the device is fully operational and actively processing signals. The current consumption at the VS pin is measured by $I_{GND(ACTIVE)}$.

The logic levels at the IN pin and DEN pin can be used to configure the device for different modes of operation. Specific combinations of logic levels at the IN pin and DEN pin can trigger the device to switch between modes such as Sleep mode, Active mode, or Stand-by mode.

The state diagram including the possible transitions is shown in **Figure 8**.The behavior of MS1810-Q1 as well as some parameters may change in dependence from the operation mode of the device.

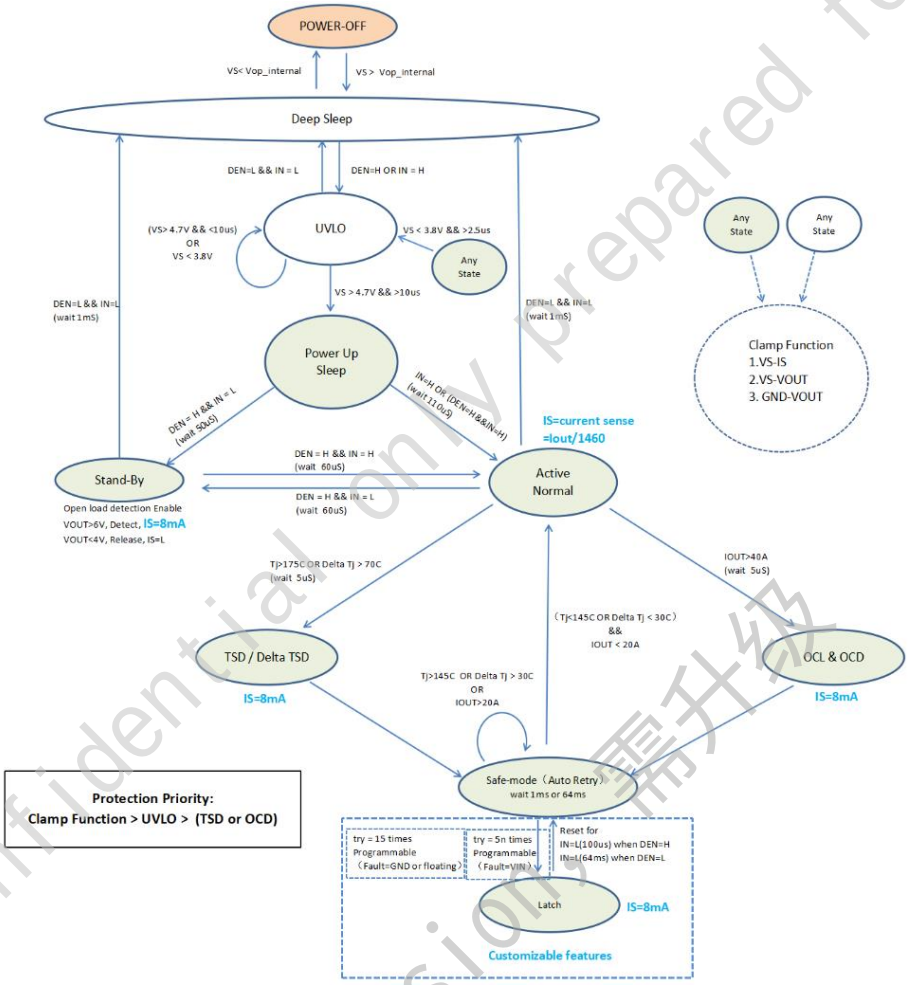

Figure 8. Operation Mode State Diagram

8.6.1 Sleep Mode

The device enters Sleep mode when all Digital Input pins (IN, DEN) are set to "low".
In Sleep mode, output is turned OFF to save power. The current consumption is at a minimum level when the device is in Sleep mode, indicating low power consumption. The device can only transition to Sleep mode if the protection mechanisms (over temperature or over load) are not active. If any of the protection mechanisms are active, the device cannot enter Sleep mode until the protection conditions are resolved.

8.6.2 Stand-by Mode

The device remains in Stand-by mode as long as the DEN pin is set to "high" while the IN pin is set to "low". In Stand-by mode, the output is turned off, indicating that the device is in a low-power state.
Only open load diagnosis is enabled in Stand-by mode, which means that the device can detect an Open Load condition when the channel is turned off. The device's ability to handle diagnostic scenarios even in Stand-by mode indicates a level of monitoring and protection features present to ensure safe and reliable operation.

8.6.3 Active Mode

The device transitions to Active mode as soon as IN pin is set to "high" while the DEN pin is also set to "high". This indicates that the device is ready to operate and respond to input signals. In Active mode, the device is fully operational and ready to perform its intended functions based on the input signals received at the IN pin.
The combination of protection features, diagnosis capabilities, and normal operation in Active mode ensures that the device operates efficiently as well as maintains system integrity.

8.7 Power Supply

The MS1810-Q1 device is powered by the VS. VS is essential for the proper functioning of the device, providing the necessary voltage levels for operations.

8.7.1 Unsupplied

In both scenarios (unsupplied state or voltage below undervoltage threshold), the MS1810-Q1 device will not function as intended. The device will not be able to carry out its normal operations, such as driving external loads or performing diagnostic functions.

8.7.2 Power-up

The MS1810-Q1 device goes through a series of states during power-up, from the initial application of supply voltage to the activation of internal signals, with the transition through the undervoltage range. The power-up condition is entered when the supply is above $V_{S(UV)}$. As the supply voltage continues to rise, there is a range between $V_{S(OP)}$ and $V_{S(UV)}$ where the undervoltage mechanism is triggered. During this phase, the device is in a transitional state where precautions should be taken due to the supply voltage still within the undervoltage range.

The undervoltage mechanism ensures that the device does not operate at under voltage conditions that could lead to improper functioning or potential damages. If the device is already operational and the supply voltage drops below the undervoltage threshold, the internal logic takes action to switch OFF the output channel, maintaining the device's integrity and preventing operations under inadequate voltage conditions.

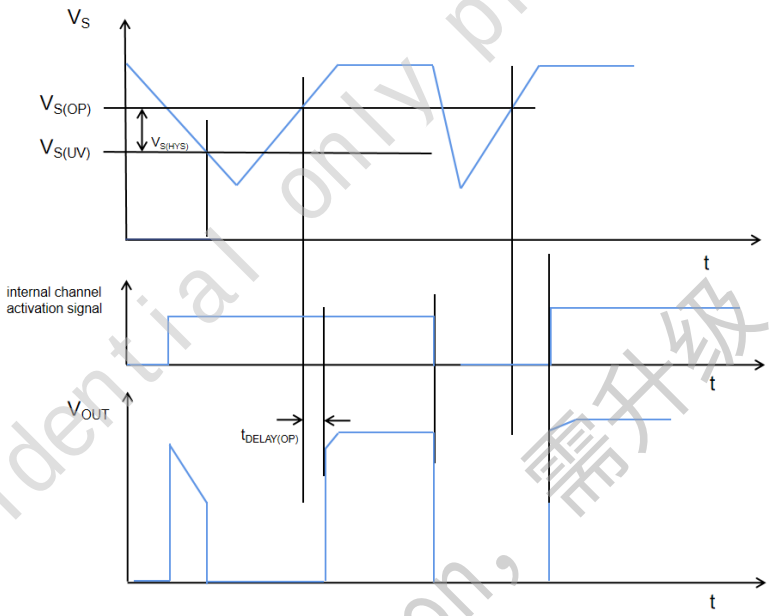

Figure 9. VS undervoltage behavior

8.8 Power Stage

The ON-state resistance $R_{DS(ON)}$ of a MOSFET typically decreases with an increase of the V_{GS}, because the gate voltage V_G and the supply voltage V_S are linked by the charge pump, so this state ends when the supply voltage exceeds the lower limit of the recommended voltage. Therefore, a higher supply voltage allows for better saturation of the MOSFET, leading to lower resistance in the ON state. Additionally, the junction temperature (T_J) of the MOSFET also affects the ON-state resistance $R_{DS(ON)}$. See **Figure 10** for more detail.

As the junction temperature increases, the ON-state resistance $R_{DS(ON)}$ of the MOSFET also tends to increase due to higher thermal effects on the device's characteristics. The high-side power stages are built using a N-channel Power MOSFET with charge pump.

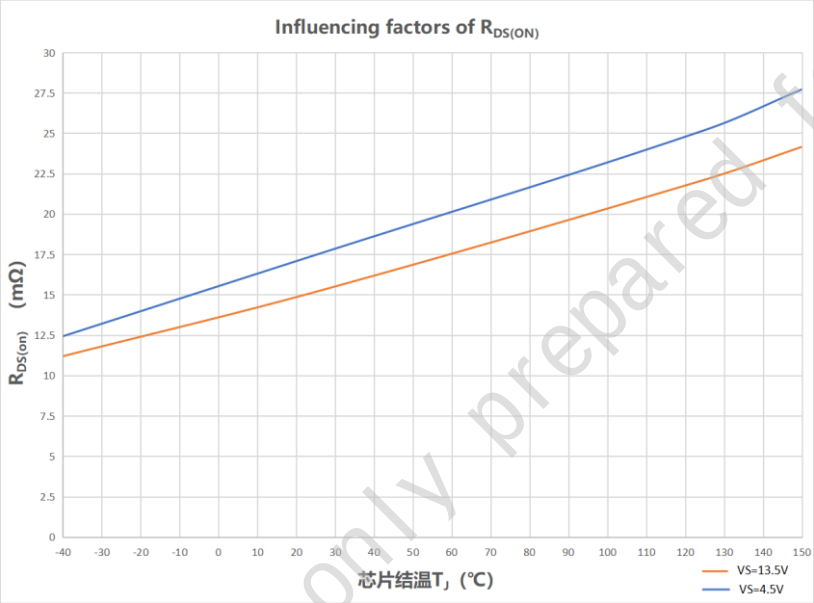

Figure 10. Typical ON-State Resistance

9. FUNCTIONAL Description

9.1 Switching Resistive Loads

Figure 11 shows the timing when switching with resistive load.
The Switch-ON slew rate ($(dV/dt)_{ON}$) is the rate of changing in time when the output voltage rises from 30% to 70% of the input voltage, and the Switch-OFF slew rate ($(dV/dt)_{OFF}$) is the rate of changing in time when the output voltage drops from 70% to 30% of the input voltage.
The Switch-ON time (t_{ON}) is defined as the time from the threshold of the digital input voltage ($V_{DI(TH)}$) to the output voltage rises to 90% of the input voltage. Conversely the Switch-OFF time (t_{OFF}), which is the time it takes from the shutdown threshold of the digital input voltage ($V_{DI(TH)}$-$V_{DI(HYS)}$) to the output voltage dropping to 10% of the input voltage.

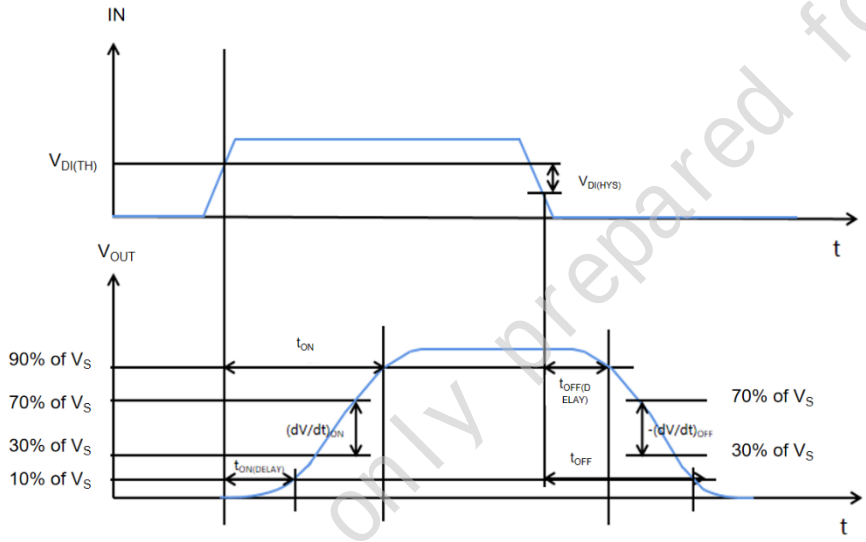

Figure 11. Switching a Resistive Load

9.2 Protection

The MS1810-Q1 is protected against over temperature, over load, Reverse Battery and over voltage clamp. Over temperature and over load protections are active when the device is not in Sleep mode. Over voltage clamp protection works in all operation modes. Reverse Battery protection works when the GND and VS pins are reverse supplied.

9.2.1 Over Voltage Clamp Protection

When switching off inductive loads with high side switches, it is crucial to consider the voltage spikes that can occur due to the load's inductance. If the device drives inductive load, the output voltage reaches a negative value during turn off. This can lead to destructive voltage spikes that may damage the device.
To address this issue and prevent the destruction of the device by avalanche breakdown due to high voltages, a voltage clamp mechanism is implemented. This mechanism limits the negative output voltage to a specific level, which is typically defined as (V_S - $V_{DS(CLAMP)}$). Please refer to **Figure 13** and **Figure 14** for details. By clamping the voltage, the device is protected from excessive negative voltages that could potentially cause damages.
In addition to the output clamp for inductive loads, there is also a clamp mechanism available for over-voltage clamp protection for both the logic and the output pins. This mechanism monitors the voltage between the VS and IS pins and limits IS pin to a certain level ($V_{IS(CLAMP)}$) to protect the device from over-voltage conditions.

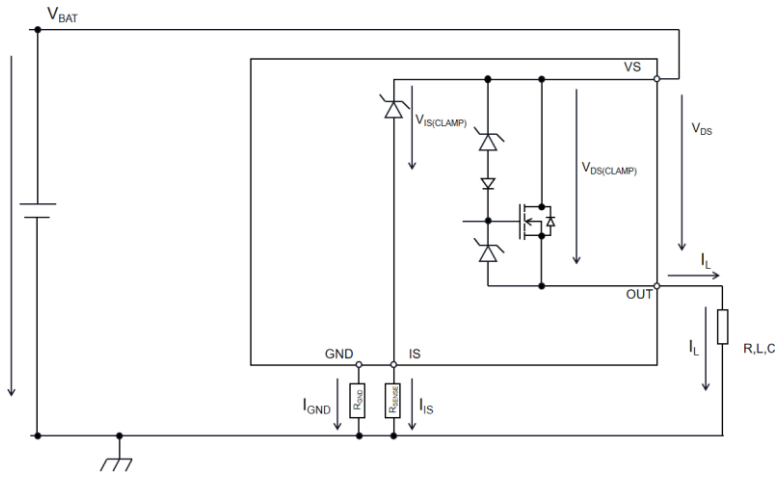

Figure 12. Clamp concept

The voltage clamp structure is designed to protect the device in all operation modes, ensuring that the device remains safe even when switching off inductive loads with high side switches. However, it's important to note that the maximum allowed load inductance is limited to prevent the device from being exposed to excessive stress.

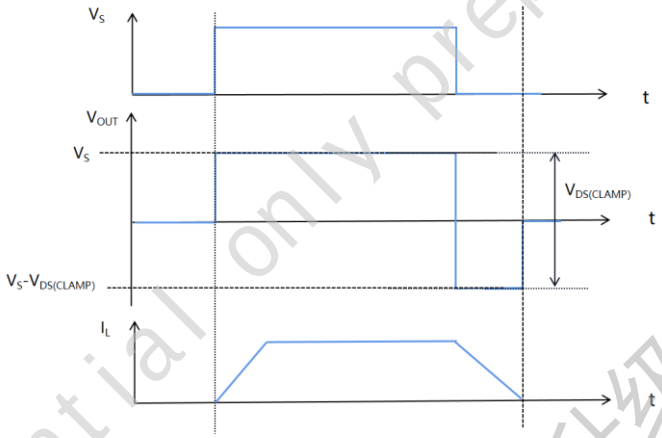

Figure 13. Switching an Inductive load Timing

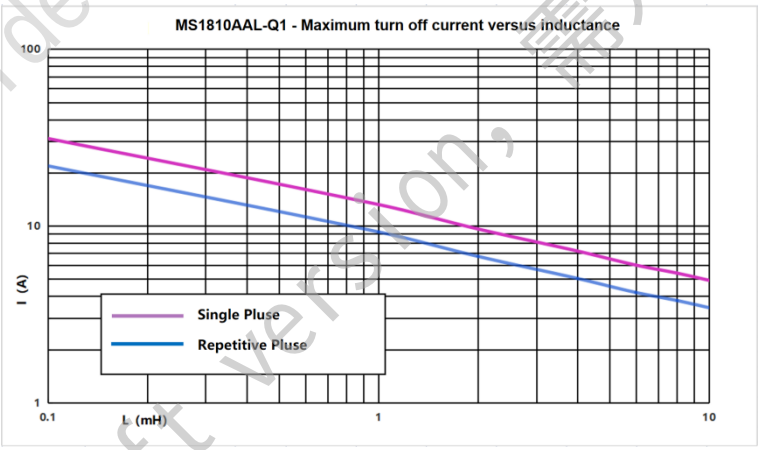

Figure 14. Maximum turn off current versus inductance

9.2.2 Over Temperature Protection

The MS1810-Q1 has three temperature sensors: T_{sensor_chip}, $T_{sensor0}$, and $T_{sensor1}$.These sensors are used to monitor the temperature conditions within the device.

$T_{J(ABS)}$ represents the absolute junction temperature above which the absolute over temperature protection mechanism is triggered. When T_{sensor_chip} exceeds $T_{J(ABS)}$, output is turned off.

The MS1810-Q1 continuously monitors the temperatures measured by $T_{sensor0}$ and $T_{sensor1}$. When the difference between these two temperatures is greater than the predefined relative threshold ΔT_J, the MS1810-Q1 detects an over temperature condition and shuts down the output.

The output remains switched off until the junction temperature reaches the "Restart" condition, indicating that the temperature has decreased to a safe level for operation.

The behavior is shown in **Figure 15** (Absolute Over Temperature Protection) and **Figure 16** (Dynamic Over Temperature Protection).

Condition	Status	"Restart" Condition
$T_{sensor}0/1 - T_{sensor\_chip} > \Delta T_J$	shuts down the output	$T_J < T_{J(ABS)}$ and $(T_{sensor}0/1 - T_{sensor\_chip}) < \Delta T_J$ (including hysteresis)
$T_{sensor\_chip} > T_{J(ABS)}$	shuts down the output	$T_J < T_{J(ABS)}$ (including hysteresis) and $(\lvert T_{sensor}0 - T_{sensor}1\rvert) < \Delta T_J$ (including hysteresis)

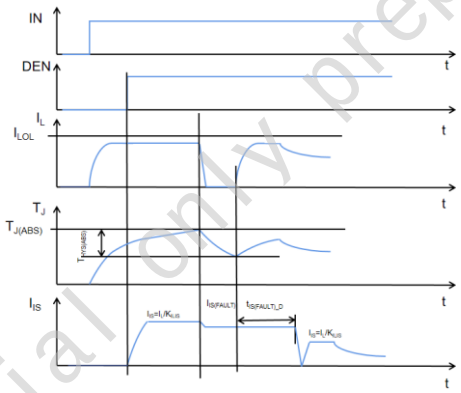

Figure 15. Over Temperature Protection (Absolute)

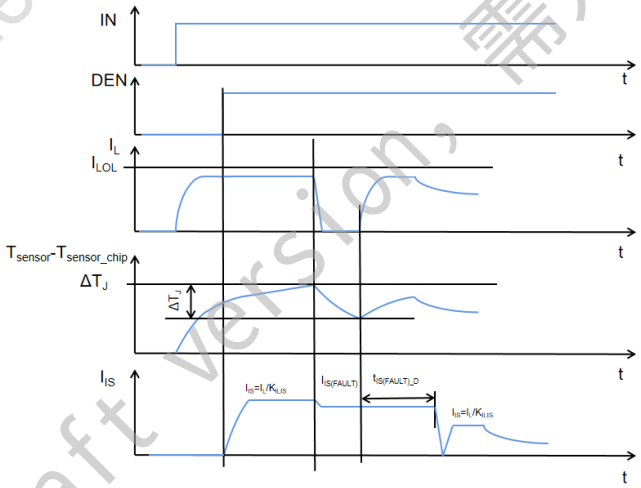

Figure 16. Over Temperature Protection (Dynamic)

9.2.3 Over Load Protection

The MS1810-Q1 device features two defined over load thresholds, namely I_{LOL1} and I_{LOL2}, which are automatically selected based on the V_{DS} voltage across the power MOS (see **Figure 17**).

When the voltage V_{DS} is less than 4V, the device selects the I_{LOL1} threshold for over load protection.

When the voltage V_{DS} exceeds 6V, the device switches to the I_{LOL2} threshold for over load protection. The automatic selection of the overload thresholds I_{LOL1} and I_{LOL2} based on the V_{DS} voltage ensures that the device adapts its protection mechanism according to the operating conditions and voltage levels.

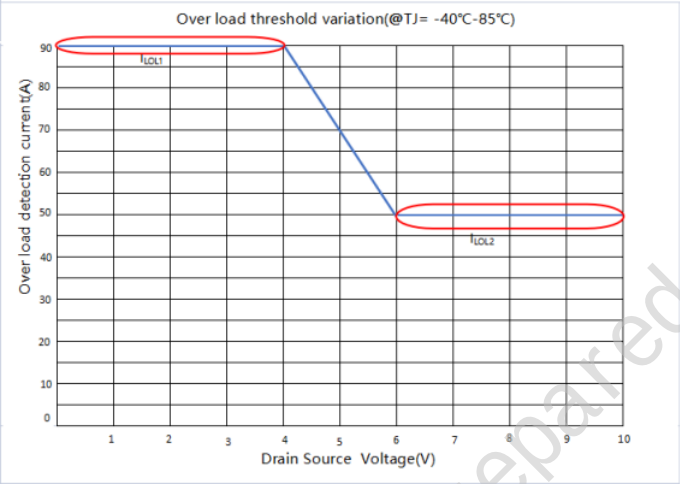

Figure 17. Over load Current Thresholds variation with V_{DS}

Despite the temperature-dependent variation in the over load threshold, the I_{LOL1} and I_{LOL2} typical value remains relatively constant up to a junction temperature of +85°C.

This stability in the I_{LOL1} and I_{LOL2} threshold up to +85°C ensures consistent protection against overload conditions within this temperature range, providing a reliable safeguard for the device and the connected system.

At low ambient temperatures, the over load threshold is set to its maximum value to accommodate the higher load inrush typically experienced during startup in cold conditions.

By maximizing the over load threshold at low temperatures, the device can safely handle the temporary surge in current without triggering unnecessary protection mechanisms (see **Figure 18**).

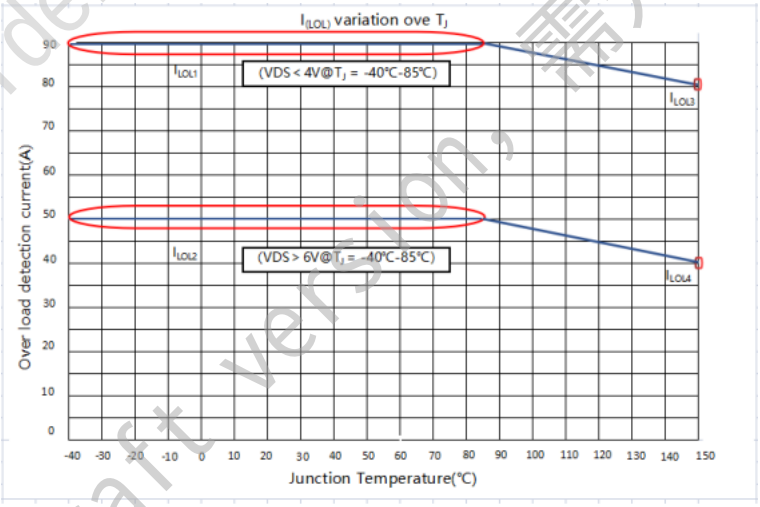

Figure 18. Over load Current Thresholds variation with T_J

9.2.4 Open Load

When the load is disconnected, the falling edge of the input pin initiates the open load detection process. When DEN is high, an open load protection is triggered when the IN becomes low, the time $t_{IS(OLOFF)\_D}$ must be observed before sensing at IS pin to allow the internal comparator to settle and provide a valid detection result.

The diagram in **Figure 19** illustrates the sequence of events and the required settling time for accurate open load detection during OFF diagnosis.

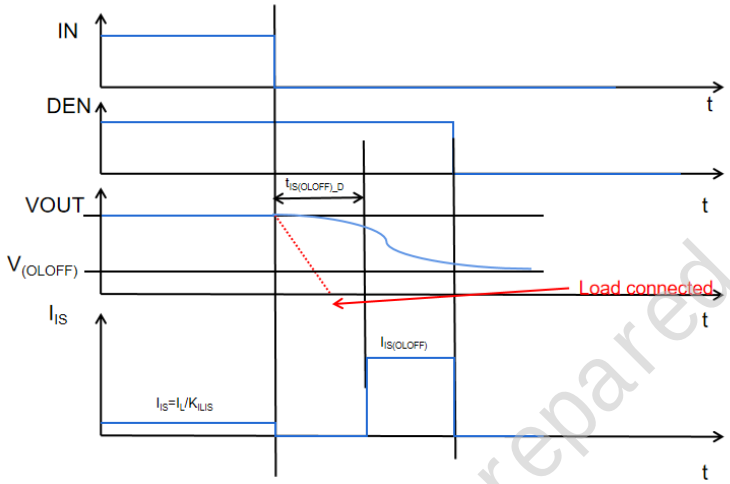

Figure 19. Open Load Timings - load disconnected

9.2.5 Reverse Battery Polarity Protection

In case of reverse battery polarity, the current of the body diode in NMOS is limited by the load itself. In addition, the current entering the ground path and logic pins must be limited to the maximum current range by external resistors. A current flowing into GND pin ($-I_{GND}$) during Reverse Polarity condition is necessary to activate ReverseON, therefore a resistive path between module ground and device GND pin must be present. **Figure 20** shows a typical application diagram.

R_{IN} and R_{DEN} used for limiting current in the input stage and ESD protection, can also offer some level of protection in the case of reverse polarity. The recommended value for R_{DEN} = R_{IN} = 4.7 KΩ.

The value of R_{SENSE} is chosen based on the desired current limit for the sense transistor. It acts as a current-sensing resistor that helps prevent excessive current from flowing through the sense transistor, which could potentially damage the transistor or other components. The recommended value for R_{SENSE} = 1 KΩ.

The value of the R_{GND} resistor is selected based on the desired current limiting characteristics of the clamping protection circuit. By choosing an appropriate resistor value, the current through the clamping diodes can be restricted to a safe level, ensuring the protection circuit operates effectively without being overloaded. During battery polarity reversed, no other protection functions are available.

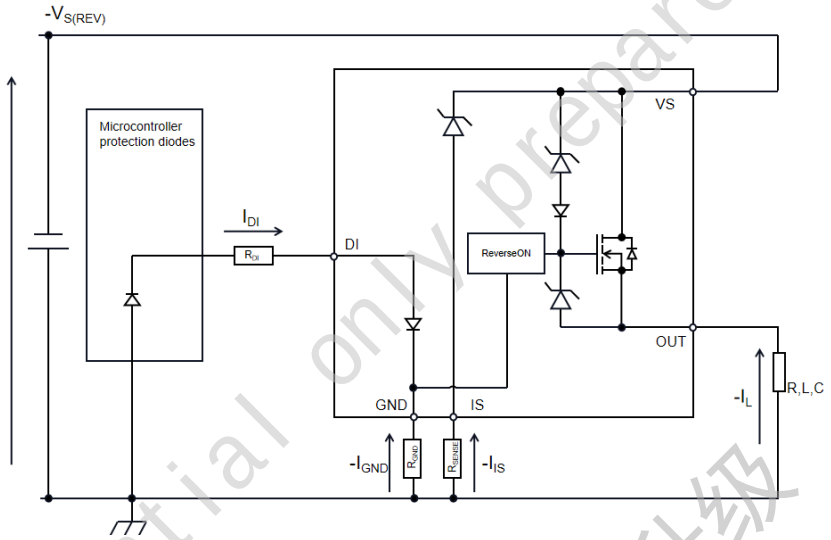

Figure 20. Reverse Battery Protection (application example)

9.2.6 Loss of Ground Protection

If there is a loss of ground connection in the module while the load remains connected to ground, the device (MS1810-Q1) has a built-in protection mechanism. It will automatically turn OFF (if it was previously ON) or remain OFF of the switch, irrespective of the voltage applied on the IN pin.

This protection feature ensures that the device does not operate in unsafe conditions when the ground connection is compromised, preventing potential damage to the device and the connected load.

It is recommended to use input resistor between the microcontroller and the MS1810-Q1.

9.3 Retry Strategy

When the fault protection is triggered, it will first try to restart 5 times, each time with an interval of 1ms. After 5 restarts, again 5 restarts are performed at intervals of 64ms to complete a retry cycle. This reset cycle is repeated all the time, but the number of cycles can be set from 1 to 16 cycles as needed, and then it enters the latched state and repeat until the fault is released.
The retry strategy is shown in **Figure 21**.

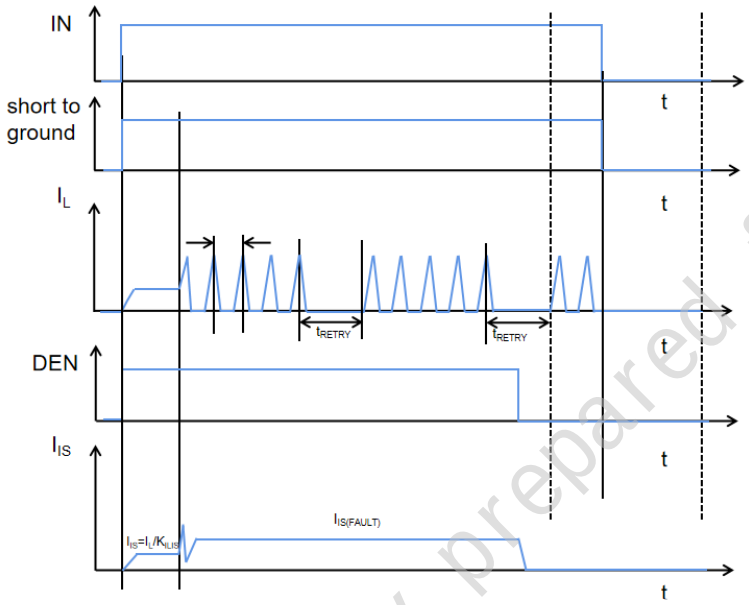

Figure 21. Retry Strategy Timing Diagram

After n consecutive “retry” cycles, the channel latches OFF (set as needed). The latched-off channel resumes after the input pin IN remains "low" for $t_{RETRY(IN)}$ time (the DEN pin remains “low”), which is shown in **Figure 22**. The latched-off channel resumes after the input pin IN remains "low" for $t_{RETRY(DEN)}$ time (the DEN pin remains “high”), which timing diagram is shown in **Figure 23**.

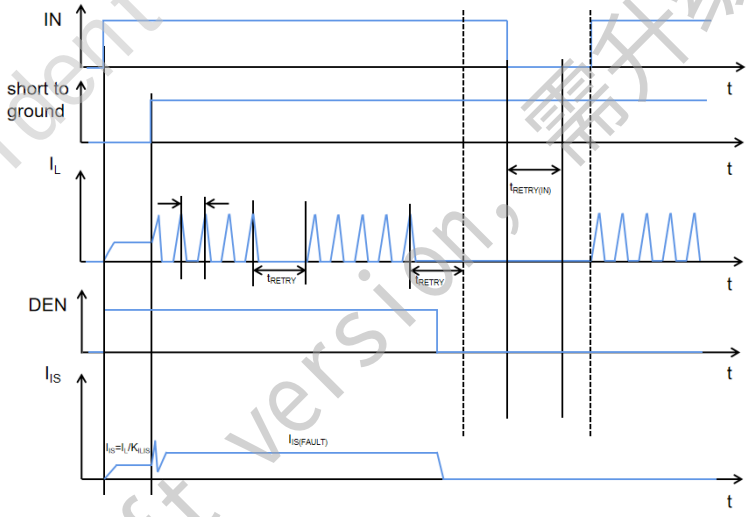

Figure 22. Retry Strategy Timing Diagram with Forced Reset (DEN = “L”)

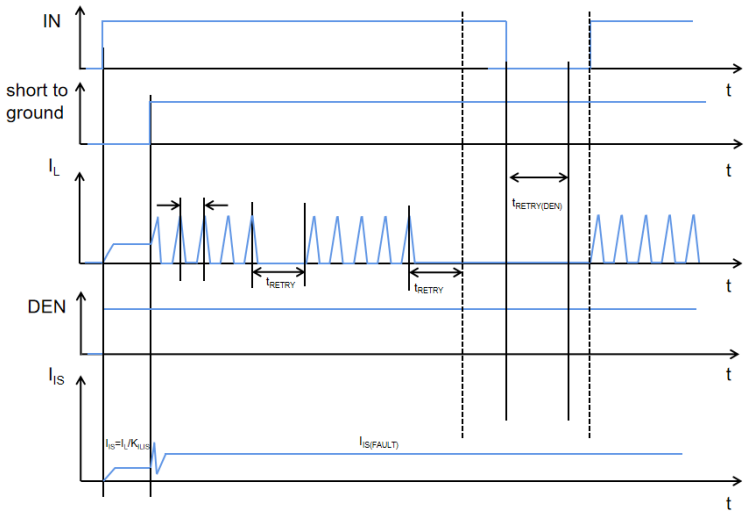

Figure 23. Retry Strategy Timing Diagram with Forced Reset (DEN = "H")

10. Application and Implementation

10.1 Typical Application

The normal operating range of the MS1810-Q1's power supply voltage recommended to be 6V to 18V, and the voltage range of the Digital Input is recommended to be 2.5V to 5.5V.
Its main application is for Body Control Module and it is capable of driving resistive, inductive, and capacitive loads. It has an output current reporting accuracy of better than 3%, the load status diagnosis function can provide real-time feedback on the load status to the control system. At the same time, it has the functions of dynamic over temperature protection, short-circuit protection with 2μs reaction time and reverse battery protection, which is extremely suitable for new energy vehicles with high safety requirements.

10.2 Typical Circuit

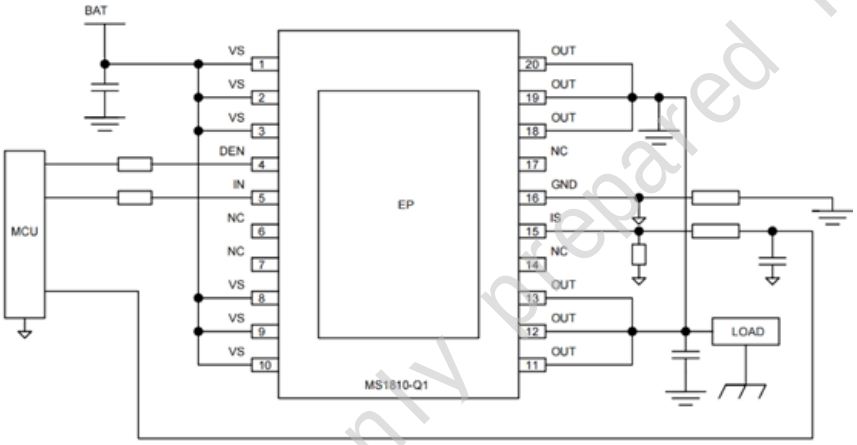

Figure 24. Application Circuit

11. Layout

11.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the MS1810-Q1. Some key guidelines are:

- **Component placement:**

– Low-ESR and low-ESL capacitors must be connected close to the device between the VS and GND pins to suppress switching spikes and to support high peak currents when turning on the external power devices.

– It is recommended to place the current limiting resistor, R_{GND}, close to GND pin of the MS1810-Q1.

- **Thermal considerations:**

If the system has multiple layers, we also recommend connecting the VS and GND pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

11.2 Layout Example

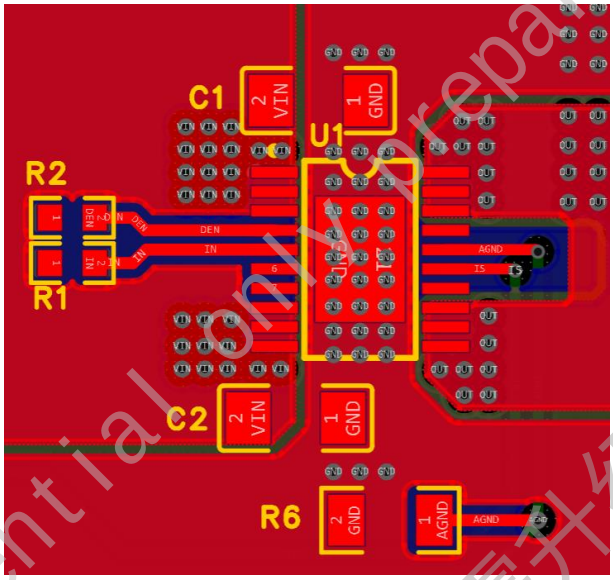

Figure 25. Layout Example

12. Package Size

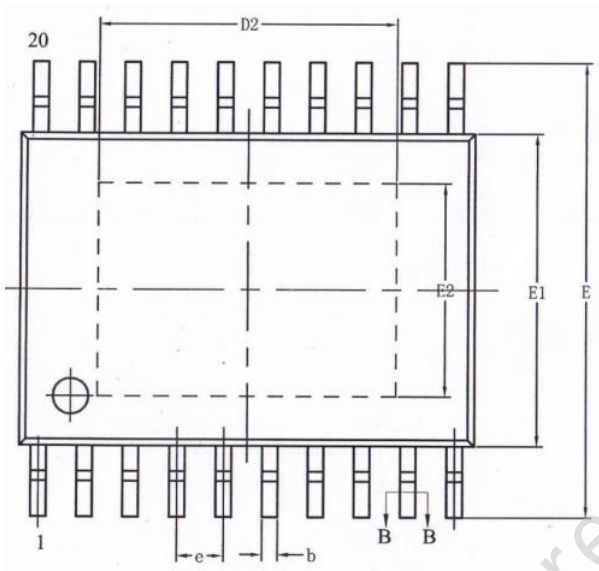

Figure 26. Top View

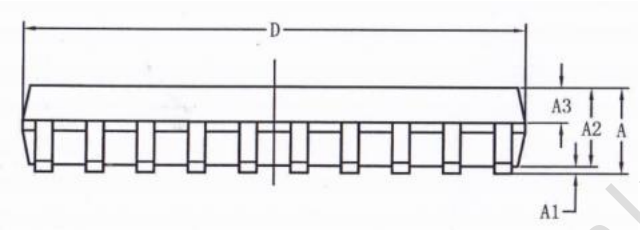

Figure 27. Side View

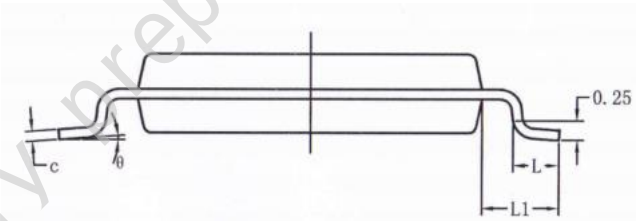

Figure 28. Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
D2	4.10	4.20	4.30
E2	2.90	3.00	3.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	8°

Unit: mm

13. Land Pattern Data

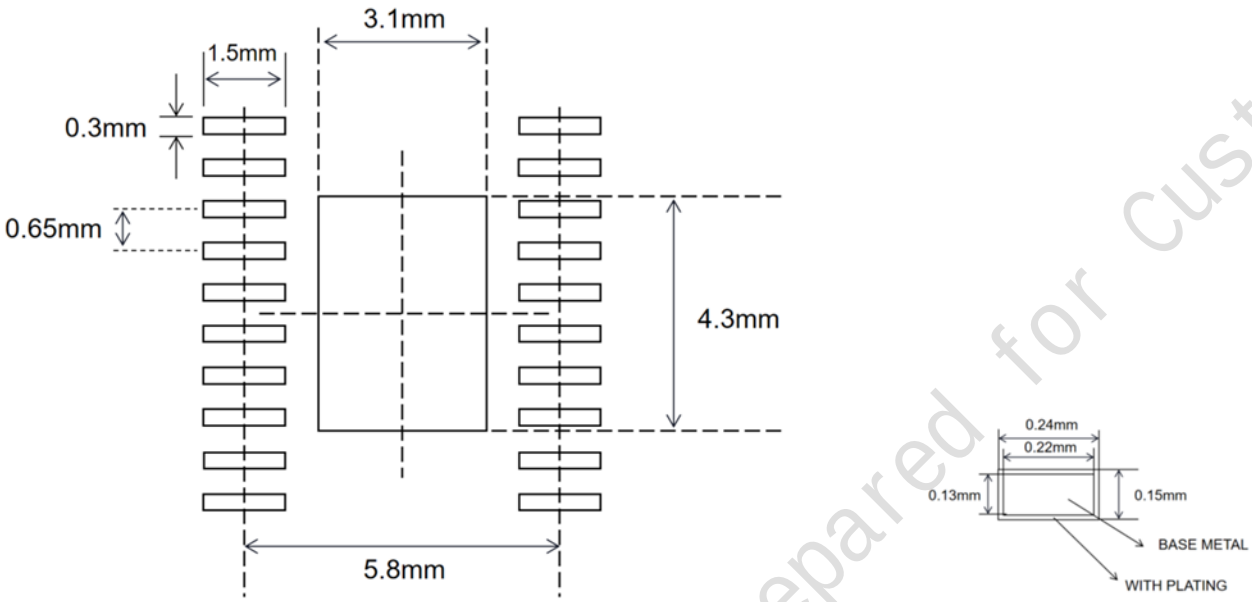

Figure 29. ETSSOP-20 Land Pattern Data

14. Reel and Tape Information

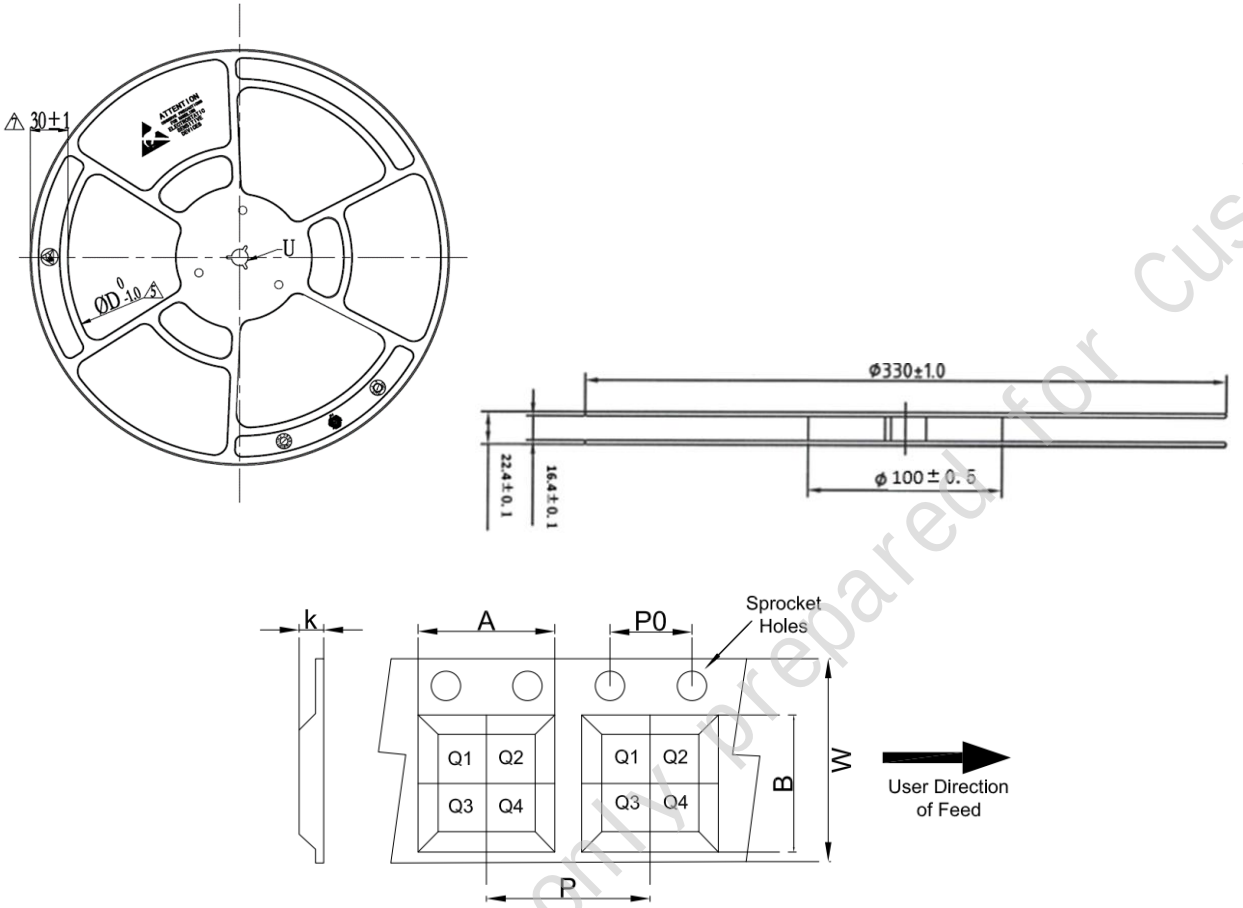

Figure 30. Reel Dimensions

Devise	Package Type	Pins	SPQ (pcs)	A(mm)	B(mm)	K(mm)	P(mm)	P0(mm)	W(mm)	Pin1 Quadrant
MS1810AAL-Q1	ETSSOP20	20	4500	6.8±0.1	6.9±0.1	1.5±0.1	8.0±0.1	4.0±0.1	16.0±0.3	Q1

-

15. Tape and Reel Box Dimensions

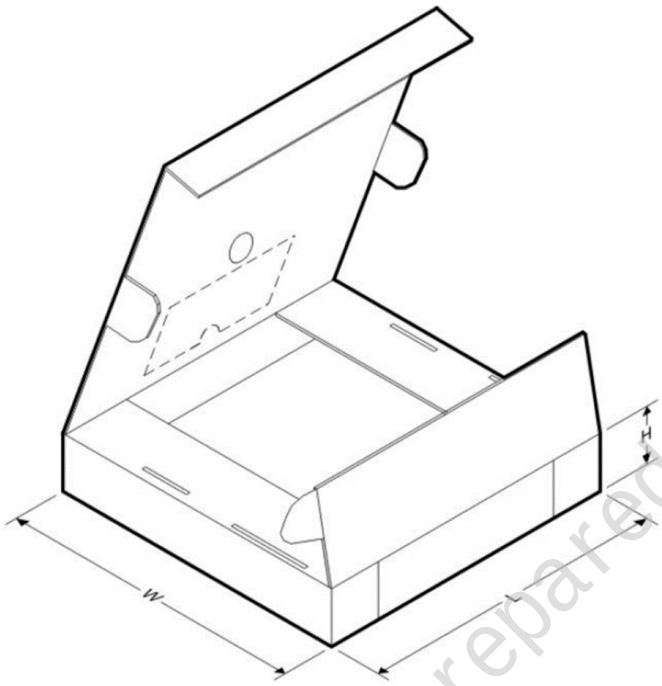

Figure 31. Box Dimensions

Device	Package Type	Pins	SPQ (pcs)	Length(mm)	Width(mm)	Height(mm)
MS1810AAL-Q1	ETSSOP20	20	9000	337	346	60