

Ultra-Fast Turn-off Synchronous Rectifier Controller

1. Description

The MK91806H is a compact secondary side synchronous rectifier controller and driver for high performance flyback converters. It is optimized for both ACF and high frequency QR. It is compatible with DCM, CCM and QR operations.

The MK91806H generates its own supply while used in high-side rectification, which eliminates the need of external supply generated by auxiliary winding of the transformer.

The extremely low 10ns turn-off propagation delay time and high sink current (\sim 4A) capability of the driver improve SR V_{DS} stress at CCM mode.

The unique VG clamping circuit works well to prevent VG from turning on by fast rising at VD pin with no VCC, that avoids the shoot through between primary side and secondary side during system startup even if the SR VCC is still below 2V.

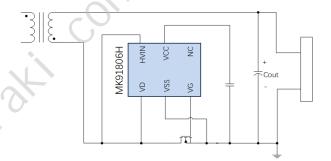
2. Typical Applications

- AC/DC Adapters for Mobile Phone and Notebook
- High Power density AC/DC Power Supplies

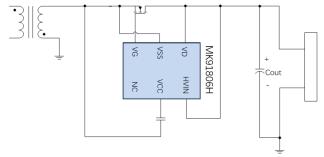
3. Features

- Optimized for <1MHz Frequency
- Supports DCM, QR and CCM Operations
- Supports Active Clamp Flyback with GaN FET or Super-junction MOSFET at Primary Side
- Operates in a Wide Output Voltage Range Down to Zero Voltage
- Self-supply for Operation with Low Output Voltage and/or High-side Rectification without an Auxiliary Winding
- Gate Drive Voltage is Up to 9V
- 10ns Fast Turn-off and 25ns Turn-on Delay
- VD/HVIN Pin Supports Negative Voltage Spikes Down to -3V
- Avoids Potential False Turn-on during DCM
- VG Clamping Circuit Works Well when VCC is Below 2V
- Supports both High-side and Low-side Rectification
- Adaptive Gate Drive for Maximum Efficiency
- SOT23-6 Package Available

4. Simplified Application



Used in low side rectification



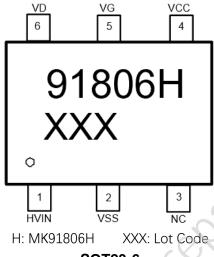
Used in high side rectification



5. Ordering Information

Ordering No.	Description
MK91806HXSA	SOT23-6, 3000 pcs/reel

6. Pin Configuration and Marking Information



SOT23-6

Absolute Maximum Ratings (1)

VCC to VSS	–0.3V to +20V
VG to VSS	0.3V to +20V
VD, HVIN to VSS	–1V to +115V
VD, HVIN to VSS	–3V to +120V (2)
Junction Temperature	+150℃
Lead Temperature	+260℃
Storage Temperature	65℃ to +150℃

Notes:

- (1) Exceeding these ratings may damage the device.
- (2) Repetitive pulse< 200ns
- (3) Measured on JESDSD51-7, 4 layers PCB

Recommended Operation Conditions

VCC to VSS	3.6V to 9.5V
D to VSS	0.7V to 100V
$\label{eq:maximum Junction Temp. (T_J)} Maximum Junction Temp. (T_J)$	40°C to +125°C

Thermal Resistance (3)	$oldsymbol{\Theta}_{JA}$	Θιс	

SOT23-6...... 100 66 °C/W



7. Electrical Characteristics

T_A=25°C, unless otherwise noted.

Parameter Symbol Conditions			Min	Тур	Max	Units
Supply Management						•
VCC UVLO Rising	VCC_on		4.4	4.6	4.9	V
VCC UVLO Falling	VCC_off		3.8	4	4.3	V
VCC UVLO Hysteresis	VCC_HYST		0.25	0.6	0.75	У
VCC Maximum		VCC=8V, VD=0V, HVIN=14V	40	80	100	mA
Charging Current Ivcc		VCC=5V, HVIN=0V, VD=12V	20	40	60	mA
VCC Regulation		VD= 0V, HVIN=14V	8.2	9.1	10	
Voltage	VCC_REG	VD=10V, HVIN=0V	5	6	7	V
0		VCC=9V, C _{LOAD} =2.2nF, F _{SW} =100kHz	3	2.5	3.5	mA
Operating Current	Icc	VCC=6.5V, C _{LOAD} =2.2nF, F _{SW} =100kHz	2	2	2.5	mA
Quiescent Current	I _{q(VCC)}	VCC=6.5V		350	550	μA
Mosfet Voltage Sensin	ıg					
V _D –V _{SS} Adjusting Voltage	V _{DS_reg}		-55	-40	-25	mV
Turn-On Threshold (V _D –V _{SS})	V _{ON_th}	0,	-350	-250	-50	mV
Turn Off Threshold (V _D –V _{SS})	V _{OFF_th}			0	10	mV
Turn-On Propagation Delay	T _{D_on}	C _{LOAD} = 0nF, VD step down from 3V to -0.5V in 5ns, measure VG rising to 1V		25	40	ns
Turn-Off Propagation Delay	T _{D_off}	C _{LOAD} = 0nF, VD step up from -0.5V to 3V in 5ns, measure VG falling to 90% of V _{G-H}		10	15	ns
Turn On Blanking Time	T _{B_ON}	C _{LOAD} = 2.2nF	0.35		0.5	us
Turn Off Blanking V _{DS} Threshold in T _{B_ON} ⁽¹⁾	V _{B_OFF}			2		V
Turn Off Blanking Time	T _{B_OFF}	C _{LOAD} = 2.2nF	250		350	ns
Gate Driver	l			1		I
V _G (Low)	VGL	ILOAD= 100mA		0.1	0.4	V
V _G (High)	VGн	VCC=6.5V, ILOAD= 100mA	VCC- 0.7	VCC- 0.3	VCC- 0.1	V





Current(1) IVGH 1 A Maximum Sink IVGL 4 A Current(1) Pull Down RSINK ILOAD= 100mA 0.53 Ω te: 1 A A A A A A A A A A A A A A A A A A B A<	MERAKI INTEGRATED				MK9	1806H
Maximum Sink IVGL Current ⁽¹⁾ 4 Pull Down R _{SINK} Impedance ⁽¹⁾ 0.53 Ω	Maximum Source	IVGн		1		А
Pull Down Impedance ⁽¹⁾ R _{SINK} ILOAD= 100mA 0.53 Ω ote:	Maximum Sink	IVGL		4		А
	Pull Down Impedance ⁽¹⁾	Rsink	ILOAD= 100mA	0.53	3	Ω
				56g/6g/	6	

Note:

Meraki confidential only



8. Typical Characteristics VS Temperature

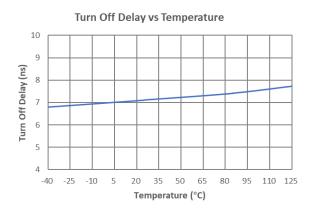


Figure 1. Turn Off Delay vs Temperature

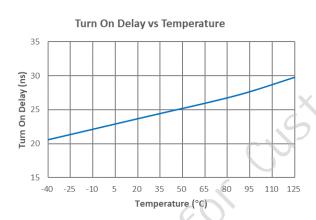


Figure 2. Turn On Delay vs Temperature

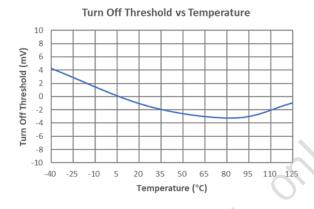


Figure 3. Turn Off Threshold vs Temperature

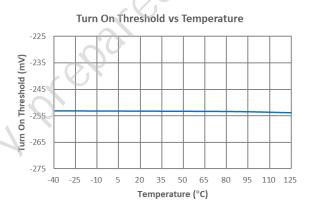


Figure 4. Turn On Threshold vs Temperature

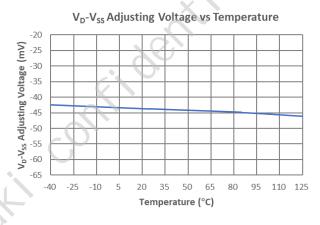


Figure 5. V_D-V_{SS} Adjusting Voltage vs Temperature

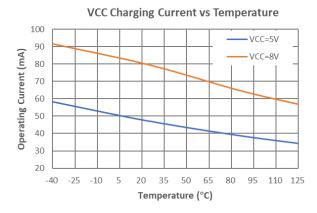
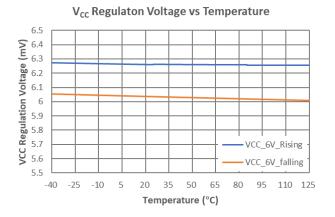


Figure 6. VCC Charging Current vs Temperature





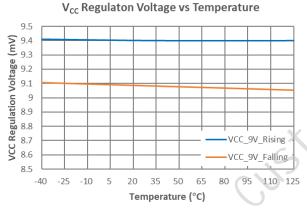


Figure 7. VCC Regulation Voltage vs
Temperature
(VD= 14V, HVIN=0V)

Figure 8. VCC Regulation Voltage vs
Temperature
(VD= 0V, HVIN=14V)

9. Pin Functions



10. Block Diagram

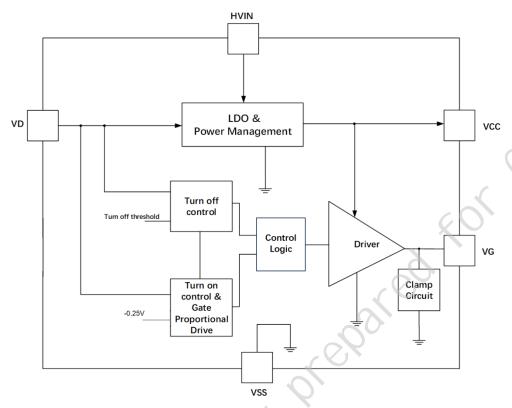


Figure 9. Functional Block Diagram

11. Operation Descriptions

The MK91806H is an advanced secondary side synchronous rectifier controller and driver for high performance flyback converters, which supports DCM, CCM and QR operations. The extremely low 10ns turn-off propagation delay time and high sink current (~4A) capability of the driver improve SR V_{DS} stress at CCM mode, particularly at the conditions of startup and V_{OUT} shorts to ground. The unique VG clamping circuit works well to prevent VG from turning on by fast rising at VD pin with no VCC, that avoids the shoot through between primary and secondary side during system startup even if the SR VCC is still below 2V.

Vcc and Startup

In order to reduce switching loss and be compatible with MOSFETs with different turn-on thresholds Vth, MK91806H provides the flexibility of different VG voltage realized at VCC. VCC is regulated at 9V which supplies MK91806H including VG when connect HVIN pin to a voltage source higher than 9.2V. Here the source for HVIN pin can be a DC voltage such as VOUT for low side rectification or an AC voltage such as the DRAIN of SR MOSFET. The maximum charging current is 80mA while VCC is regulated from HVIN voltage source.

When the voltage on HVIN pin is below 9.2V but above 6V, VCC follows HVIN with dropout voltage depending on the load current at VCC, until HVIN drops to around 6V. Once HVIN drops around 6V, a 40mA current source from VD starts charging up VCC and regulating it at 6V.

The typical system implementations with different bias connections are shown below. A 0.1uF to 1uF bypass capacitor is suggested at VCC pin.



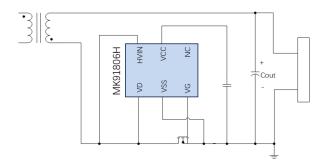
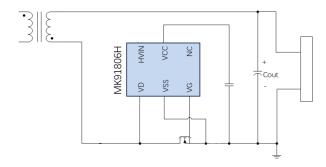


Figure 10. Low-side Rectification 1, $VCC_{REG}=9V$

Figure 11, High-side Rectification 1, VCC_REG=9V



WK91806H

WSS VCC

HVIN

Cout

Cout

Cout

The state of t

Figure 12. Low-side Rectification 2, $VCC_{REG}=6V$

Figure 13. High-side Rectification 2, VCC_REG=6V

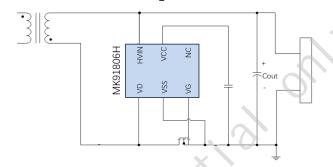


Figure 14. Low-side Rectification 3, VCC_REG=6V to 9V^[1]

Note:

In Low-side Rectification 3, VCC is supplied by VD and regulated at 6V if V_{OUT} is lower than 6V; VCC is regulated at 9V through HVIN if V_{OUT} voltage is larger than 9V; VCC is close to V_{OUT} while V_{OUT} is between 6V and 9V, which generated by HVIN path.

Conduction Phase

After SR VG turns on, a minimum blanking time T_{B_ON} is required to prevent the parasitic ringing from falsely turning off SR VG. The minimum turn-on blanking time is around 1.1us for MK91806H, during which the turn off threshold is increased to 2V. Right before T_{B_ON} timer expires, MK91806H starts monitoring V_{DS} against a -40mV value to determine if VG needs to be slowly discharged. This operation adjusts V_{DS} of SR MOSFET to be around -40mV until the current through SR MOSFET drops to zero. In CCM mode, VG is prepositioned to be lower than VCC by V_{DS} adjusting scheme so that VG is turned off even faster; In DCM/QR mode, this V_{DS} adjusting design makes V_{DS} cross 0V exponentially faster, which combines with the 10ns turn-off propagation delay to make turn-off timing more accurately regardless of the accuracy of turn-off threshold.



Turn Off Phase

MK91806H's turn-off threshold is different at different time. Within the minimum turn-on blanking time T_{B_ON} , V_{DS} turn-off threshold is 2V which is the same as V_{B_OFF} . After the minimum turn-on blanking time T_{B_ON} , the turn-off threshold is around 0V, that combines with extremely fast 10ns turn-off propagation delay and 4A VG pull-down (sinking) current, synchronous rectifier is able to be turned off not too early which causes more SR FET body diode conduction time and more negative turn-off ringing, or not too late which creates risk of shoot through between primary side and SR side.

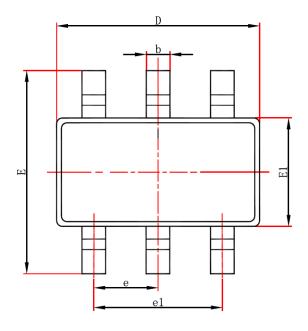
12. PCB Layout Recommendations

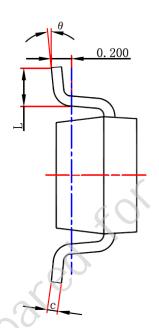
The PCB layout guidance are shown below:

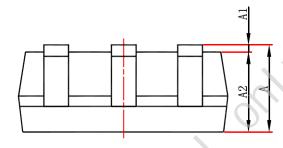
- 1. The trace from VG pin to the GATE of SR MOSFET needs to be as short as possible. The VSS pin to the SOURCE of SR MOSFET needs to route with short and wide trace.
- 2. The sense loop (VD pin and VSS pin) is as small as possible
- In two-layer boards, avoid fast dv/dt traces underneath MK91806H, such as the DRAIN of SR MOSFET network
- 4. The 0.1uf-1uf VCC decoupling capacitor should be located between VCC pin and VSS pin as close as possible to MK91806H with minimal trace length to improve the noise filtering.



13. Package Information (SOT23-6)



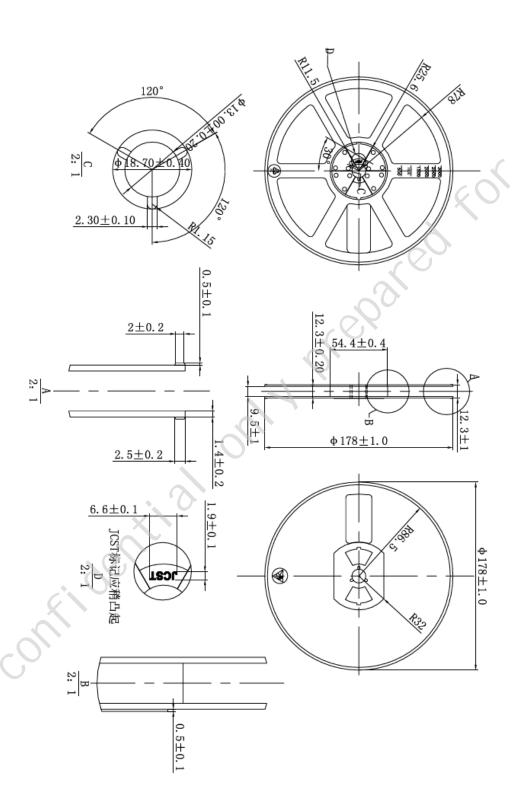




Cb l	Dimensions Ir	n Millimeters	Dimensions	In Inches	
Symbol	Min.	Max.	Min.	Max.	
Α	1.050	1.250	0.041	0.049	
A1	0.000	0.100	0.000	0.004	
A2	1.050	1.150	0.041	0.045	
b	0.300	0.500	0.012	0.020	
C	0.100	0.200	0.004	0.008	
D	2.820	3.020	0.111	0.119	
E1	1.500	1.700	0.059	0.067	
E	2.650	2.950	0.104	0.116	
е	0.950(BSC)		0.037	(BSC)	
e1	1.800	2.000	0.071	0.079	
L	0.300	0.600	0.012	0.024	
θ	0°	8°	0°	8°	

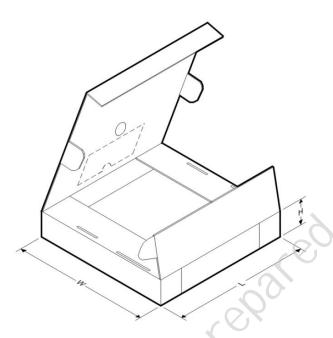


14. Tape and Reel Information





15. Tape and Reel Box Dimensions



Device	Package	Pins	SPQ	Length	Width	Height
	Туре		(pcs)	(mm)	(mm)	(mm)
MK91806HSA	SOT23-6	6	30000	203	203	195

Figure 15. Box Dimensions