4-A Source, 7-A Sink, 5.7-kV$_{RMS}$ Single-Channel Isolated Gate Driver

1. Description

The MD18011A/B/C is an isolated single channel gate driver family designed with 4-A source current and 7-A sink current to drive MOSFET, IGBT and SiC MOSFET.

The device's input is opto-compatible. The input side is isolated from the output side by 5.7kV$_{RMS}$ isolation barrier with a minimum of 200-V/ns common mode transient immunity.

The device's input can handle -16V signal, and VDD of output can handle 30V supply, which increases robustness against ringing from parasitic inductance of long routing traces.

2. Applications

- Isolated AC-DC and DC-DC power supplies
- Sever, telecomm, datacomm, and industrial infrastructures.
- PV Inverters
- HEV and EV battery chargers

3. Features

- Pin-out compatible with general opto isolated gate drivers
- 4-A Source/7-A Sink Peak Current
- CMTI greater than 200V/ns
- Input Pins Can Tolerate -16V
- Recommended maximum 28V output driver supply voltage.
- 80ns (typical) propagation delay
- Safety-related certifications:
  (1) 8000-V$_{PK}$ reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17): 2021-10
  (2) 5.7kV$_{RMS}$ isolation for 1minute per UL1577
  (3) CQC certification per GB4943.1-2022
- Wide body SOW-6 package with >8mm creepage and clearance
- Operating junction temperature: -40 ℃ to 125℃

4. Typical Application

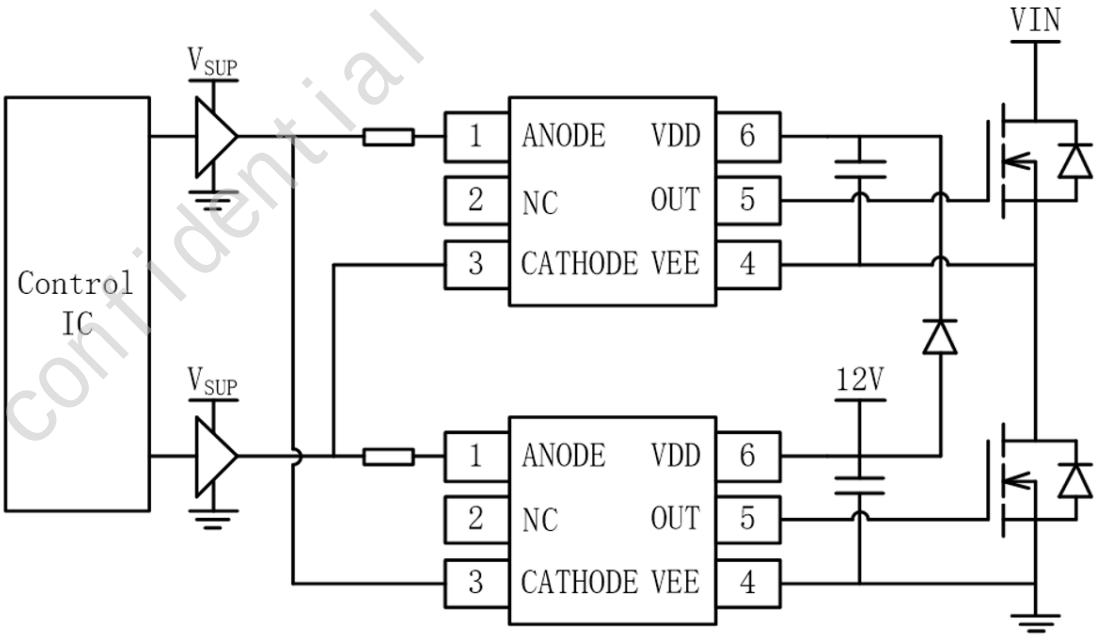
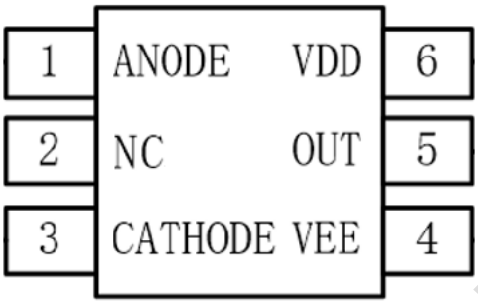


Figure 1.Typical Application Diagram

5. Ordering Information

Order Code	UVLO	Package	Pins	Description
MD18011AWAH	5V	SOW-6	6	MSL-2, 1000 pcs/ reel
MD18011BWAH	8V	SOW-6	6	MSL-2, 1000 pcs/ reel
MD18011CWAH	12V	SOW-6	6	MSL-2, 1000 pcs/ reel

6. Pin Configuration and Functions



SOW-6

Pin #	Name	Description
1	ANODE	Anode
2	NC	No Connection
3	CATHODE	Cathode
4	VEE	Negative output supply rail
5	OUT	Gate-drive output
6	VDD	Positive output supply rail

7. Specifications

7.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted) (1)

Parameter	Symbol	Min	Max	Unit
Average Input Current	$I_{F(AVG)}$		25	mA
Peak Transient Input Current	$I_{F(TRAN)}$ <1us		1	A
Reverse Input Voltage	$V_{R(MAX)}$		16	V
Output supply voltage	VDD-VEE	-0.3	30	V
Output signal voltage	OUT-VEE	-2V@200ns -5V@100ns	VDD + 0.3	V
Junction Temperature (T_J)	T_J	-40	150	°C
Storage Temperature	T_{STG}	-65	150	°C

Note:

(1) Exceeding these ratings may cause permanent damage to the device. The device is not guaranteed to function outside of its operating conditions.

7.2 ESD Ratings

		Value	Unit
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1500	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Output supply voltage	VDD-VEE	UVLO	28	V
Input Diode Forward Current (Diode "ON")	$I_{F(ON)}$	7	16	mA
Anode voltage - Cathode voltage (Diode "OFF")	$V_{F(OFF)}$	-15	0.9	V
Junction Temperature	T_J	-40	150	°C
Ambient Temperature	T_A	-40	125	°C

7.4 Thermal Information (1)

	$R_{\theta JA}$	$R_{\theta JC}$	Unit
SOW-6	98.4	50.1	°C/W

Note:

(1) According to Jedec JESD51-2, JESD51-7 at natural convection on FR4 1s0p board.

7.5 Electrical Characteristics

Unless otherwise noted, all typical values are at T_A = 25°C, VDD=15V,1-μF capacitor from VDD to VEE, C_L=2.2nf. All min and max specifications are at recommended operating conditions T_J =–40°C to 150°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT						
Input Forward Threshold Current Low to High	I_{F_LH}	V_{OUT} > 5 V, C_L = 2.2nF	1	1.5	2	mA
Input Forward Threshold Voltage Low to High	V_{F_LH}	V_{OUT} > 5 V, C_L = 2.2nF	0.92	1.09	1.21	V
Threshold Input Voltage High to Low	V_{F_HL}	C_L = 2.2nF	0.9	1.08	1.21	V
Temp Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T$(1)	I_F = 10mA		0.55		mV/℃
Input Reverse Breakdown Voltage	V_R	I_R = 10uA	16			V
UNDERVOLTAGE LOCKOUT						
VDD rising threshold	V_{DDR}	For MD18011A	5.2	5.5	5.8	V
VDD falling threshold	V_{DDF}		4.9	5.2	5.5	V
VDD threshold hysteresis	V_{DDHYS}			0.3		V
VDD rising threshold	V_{DDR}	For MD18011B	7.7	8.3	8.9	V
VDD falling threshold	V_{DDF}		7	7.6	8.2	V
VDD threshold hysteresis	V_{DDHYS}		0.4	0.7	1	V
VDD rising threshold	V_{DDR}	For MD18011C	10.5	12.0	13.5	V
VDD falling threshold	V_{DDF}		9.5	10.5	11.5	V
VDD threshold hysteresis	V_{DDHYS}		1	1.5	2	V
OUTPUTS (OUTA, OUTB)						
Source peak current	I_{SRC}	I_F = 10 mA, C_{LOAD}=0.1uF		4		A
Sink peak current	I_{SNK}	I_F = 10 mA, C_{LOAD}=0.1uF		7		A
High output voltage	V_{OH}	I_F =10mA, I_{OUT} = 10mA		VDD -12	VDD -20	mV
Low output voltage	V_{OL}	V_F =0V, I_{OUT} = -10mA		6	10	mV
Output pullup resistance	R_{OH}	I_F =10mA, I_{OUT} = 10mA		1.2	2	Ω
Output pulldown resistance	R_{OL}	V_F =0V, I_{OUT} = -10mA		0.6	1	Ω
Output Supply Current (Diode On)	I_{VDD_H}	I_F =10mA, I_{OUT} =0mA		1.45	2.2	mA
Output Supply Current (Diode Off)	I_{VDD_L}	V_F =0V, I_{OUT} =0mA		1.21	2	mA

7.6 Switching Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Rise time	t_R	C_{LOAD}=2.2nF 20%-80% VDD		16	25	ns
Fall time	t_F			8	15	ns
Minimum input pulse width that passes to output	t_{PWMIN}			50	80	ns
Rising propagation delay	$t_{RPDA(B)}$	C_{LOAD}=2.2nF, I_F=10mA		80	110	ns
Falling propagation delay	$t_{FPDA(B)}$			80	110	ns
Pulse width distortion	T_{PWD}				25	ns
VDD power-up time delay	T_{START_VDD}	VDD rising from 0V to 15V		5	10	us
Common mode transient immunity	CMTI (1)			200		V/ns

Notes:

(1) Not subject to production test, guarantee by design

7.7 Typical Characteristics

VDD= 15V, 1-μF capacitor from VDD to VEE, C_{LOAD} = 2.2nF for timing tests and 100nF for I_{OH} and I_{OL} tests, T_J =–40°C to +150°C, (unless otherwise noted)

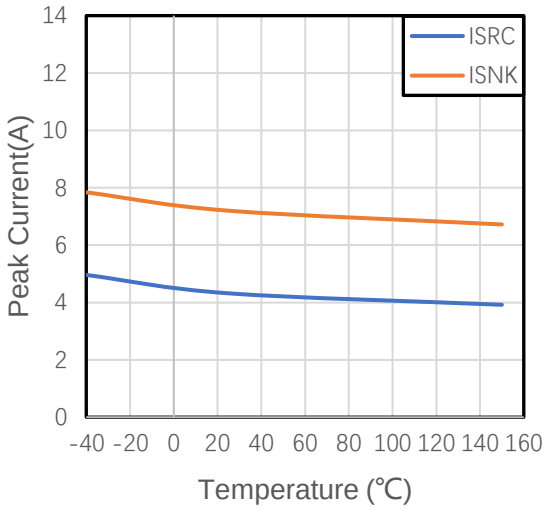


Figure 2 Output Drive currents versus Temperature

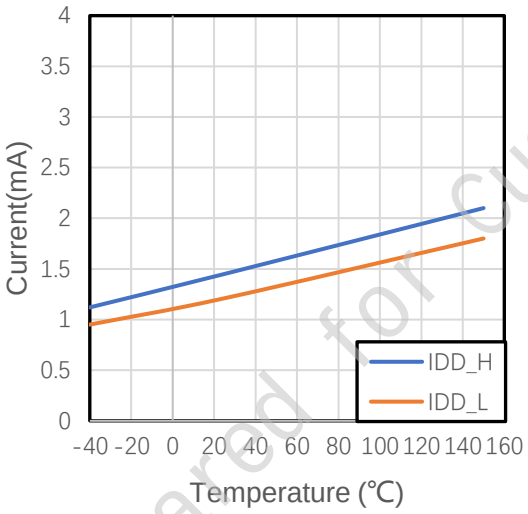


Figure 3 Supply currents versus Temperature

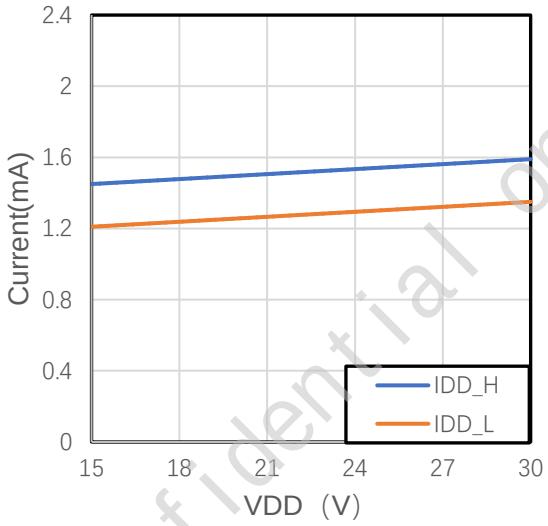


Figure 4 Supply current versus Supply Voltage

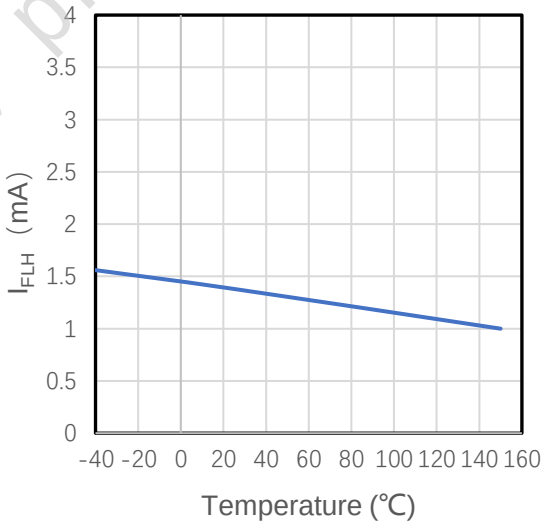


Figure 5 Forward threshold current versus Temperature

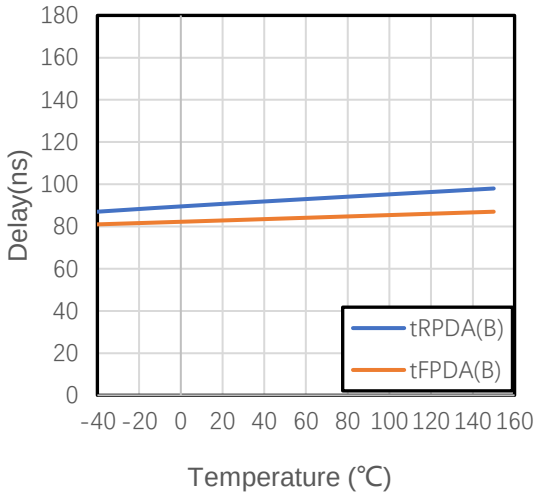


Figure 6 Propagation delay versus Temperature

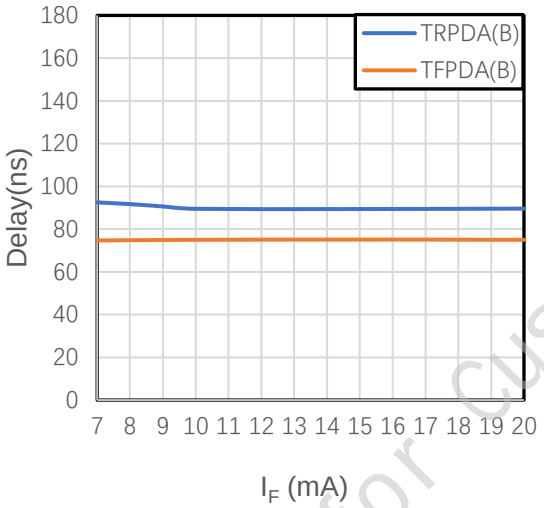


Figure 7 Propagation delay versus Forward Current

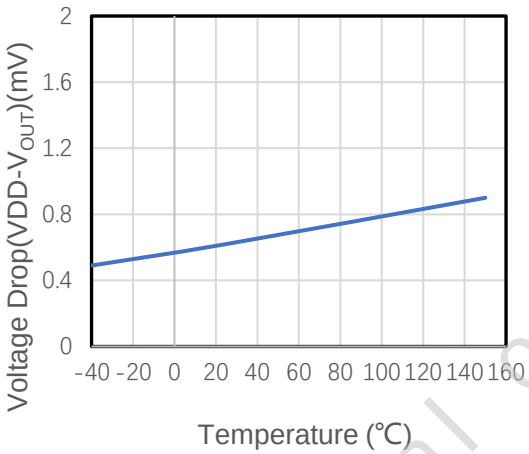


Figure 8 V_{OH} (No Load) versus Temperature

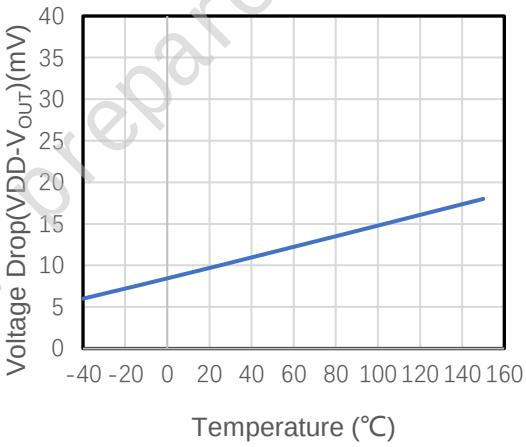


Figure 9 V_{OH} (10mA Load) versus Temperature

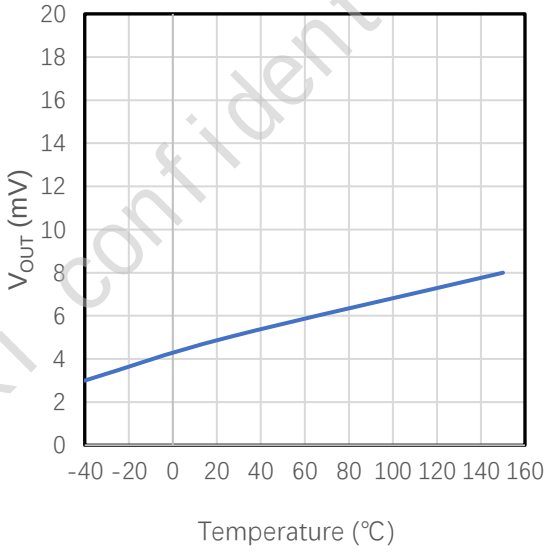
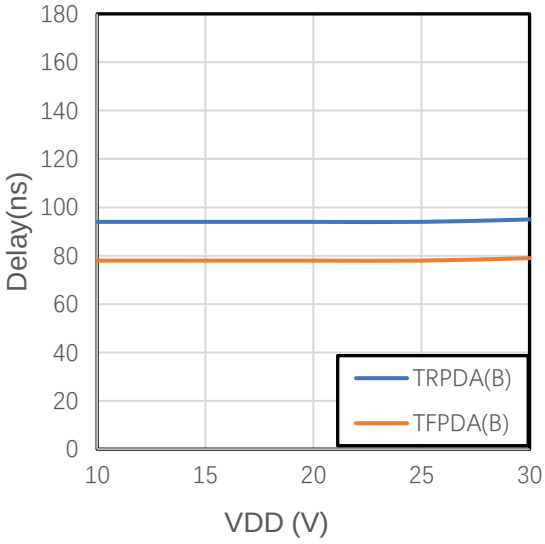
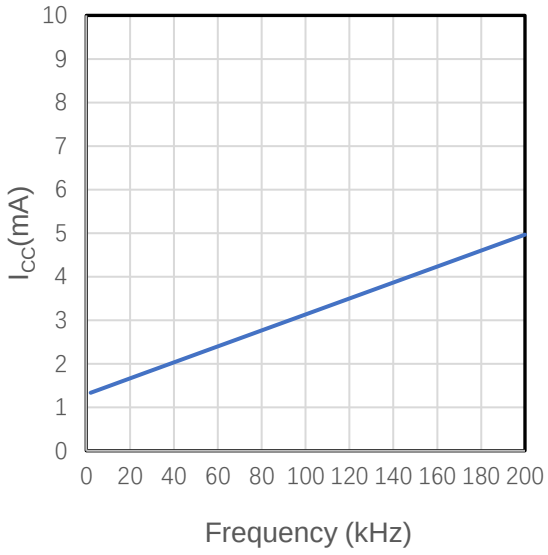


Figure 10 V_{OL} (10mA Load) versus Temperature



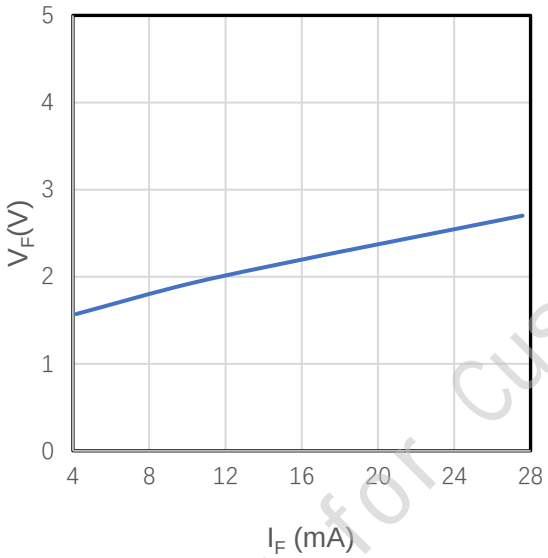
C_{LOAD} = 1nF

Figure 11 Propagation delay versus Supply voltage



C_{LOAD}=1nF

Figure 12 Supply current versus Frequency



C_{LOAD}=1nF

Figure 13 Forward current versus Forward voltage drop

7.8 Power Ratings

		Value	Unit
Power dissipation	VDD =26V，IF= 10mA 1MHz, 50% duty cycle，C_{LOAD} = 2.2nF	750	mW
Power dissipation by input side		10	mW
Power dissipation by output side		740	mW

7.9 Insulation Specifications

Parameter	Symbol	Conditions	Value	Unit
External clearance	CLR	Shortest pin-to-pin distance through air	>8	mm
External creepage	CPR	Shortest pin-to-pin distance across the package surface	>8	mm
Distance through insulation	DTI	Distance through insulation	>100	um
Comparative tracking index	CTI		>600	V
Material group		According to IEC60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage≤600V_{RMS}	I-IV	
		Rated mains voltage≤1000V_{RMS}	I-III	
DIN VDE V 0884-17				
Maximum repetitive peak isolation voltage	V_{IORM}	AC voltage (bipolar)	1768	V_{PK}
Maximum working isolation voltage	V_{IOWM}	AC voltage (sine wave); time dependent dielectric breakdown (TDDB)	1250	V_{RMS}
		DC voltage	1768	
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 sec (qualification) V_{TEST} =1.2×V_{IOTM}, t = 1 s (100% production)	8000	V_{PK}
Maximum surge isolation voltage	V_{IOSM}	Test method per IEC 62368, 1.2/50 us waveform, V_{TEST} = 1.6×V_{IOSM} = 12800 V_{PK} (qualification)	8000	V_{PK}
Apparent charge	Q_{pd}	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2×V_{IORM} = 1500 V_{RMS}, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6×V_{IORM} = 2000 V_{RMS}, t_m = 10 s	≤5	pC

		Method b1: At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2×V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 ×V_{IORM} = 2344 V_{RMS}, t_m = 1 s	≤5	pC
Barrier capacitance, input to output	C_{IO}	V_{IO} = 1V, f = 1 MHz	0.5	pF
Isolation resistance, input to output	R_{IO}	V_{IO}=500V, T_A=25℃	10^{12}	Ω
		V_{IO}=500V, T_A=100℃ to 125℃	10^{11}	Ω
		V_{IO}=500V, T_A=150℃	10^{9}	Ω
Pollution degree			2	
Climatic category			40/125/21	
UL 1577				
Withstand isolation voltage	V_{ISO}	V_{TEST}=V_{ISO}, t=60s (qualification), V_{TEST}=1.2×V_{ISO}, t=1s (100% production)	5700	V_{RMS}

7.10 Safety-limiting Values(1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Safety output supply current	I_S	VDD=15V			50	mA
		VDD=30V			25	mA
Safety supply power	P_S	Input side			10	mW
		Output side			740	mW
		Total			750	mW
Safety temperature	T_S				150	℃

Note:

(1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

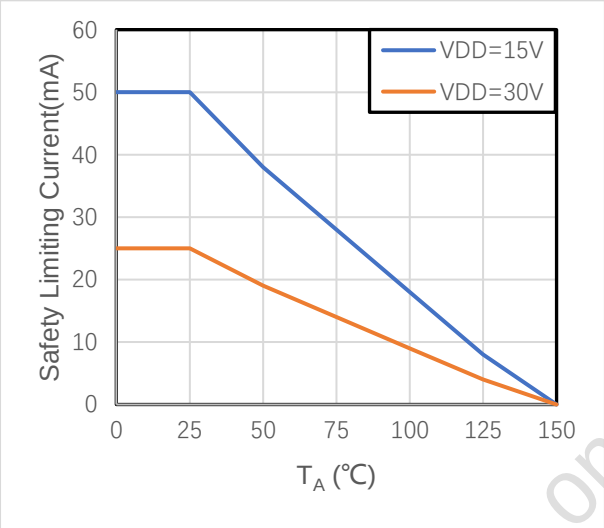


Figure 14 Thermal Derating Curve for Limiting Current per VDE

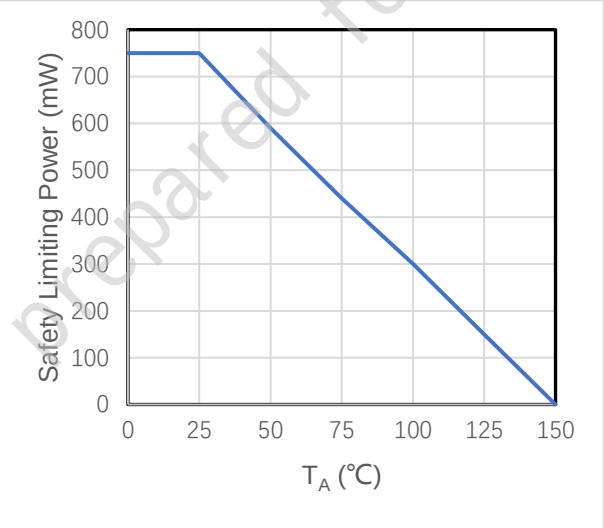


Figure 15 Thermal Derating Curve for Limiting Power per VDE

Note:

(1) The maximum safety temperature (T_S) has the same value as the maximum junction temperature (T_J). The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature (T_A).

7.11 Safety-Related Certifications

VDE	UL	CQC
Certified according to DIN EN IEC 60747-17 (VDE 0884-17): 2021-10	UL 1577 Component Recognition Program	certification per GB4943.1-2022
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 1768 V_{PK}; Maximum surge isolation voltage, 8000 V_{PK}	Single Protection, 5700VRMS Isolation Voltage	Reinforced insulation
40059122	E537168	CQC24001428841

8. Parameter Measurement Information

8.1 Propagation Delay

Figure 16 shows the propagation delay from the input forward current I_F, to V_{OUT}. This figure also shows the circuit used to measure the rise (t_R) and fall (t_F) times and the propagation delays t_{PDLH} and t_{PDHL}.

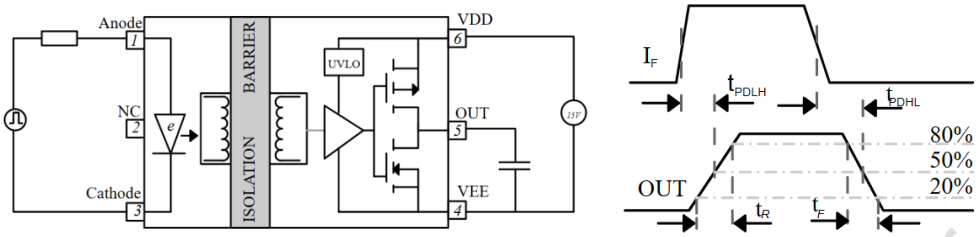


Figure 16 I_F to VOUT Propagation Delay, Rise Time, and Fall Time

8.2 CMTI Testing

Figure 17 is the simplified diagram of the CMTI testing. Common mode voltage is set to 800V. The test is performed with I_F = 7mA (V_{OUT}= High) and I_F = 0mA (V_{OUT} = LOW). The diagram also shows the failing criteria for both cases. During the application on the CMTI pulse with I_F = 7mA, it is considered as a failure if VOUT drops from VDD to ½VDD. With I_F= 0mA, if V_{OUT} rises above 1V, it is considered as a failure.

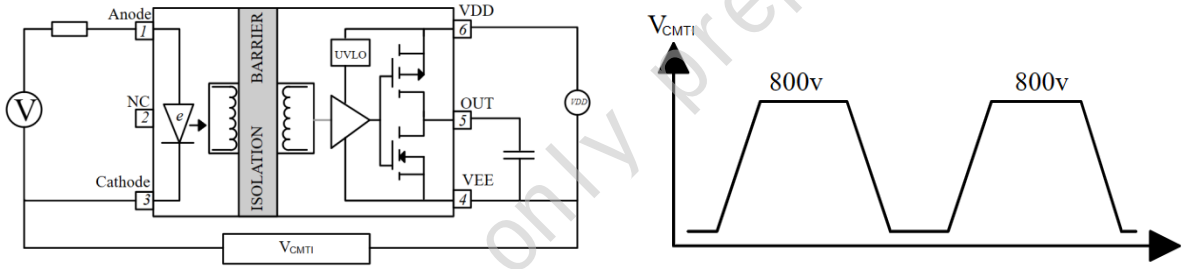


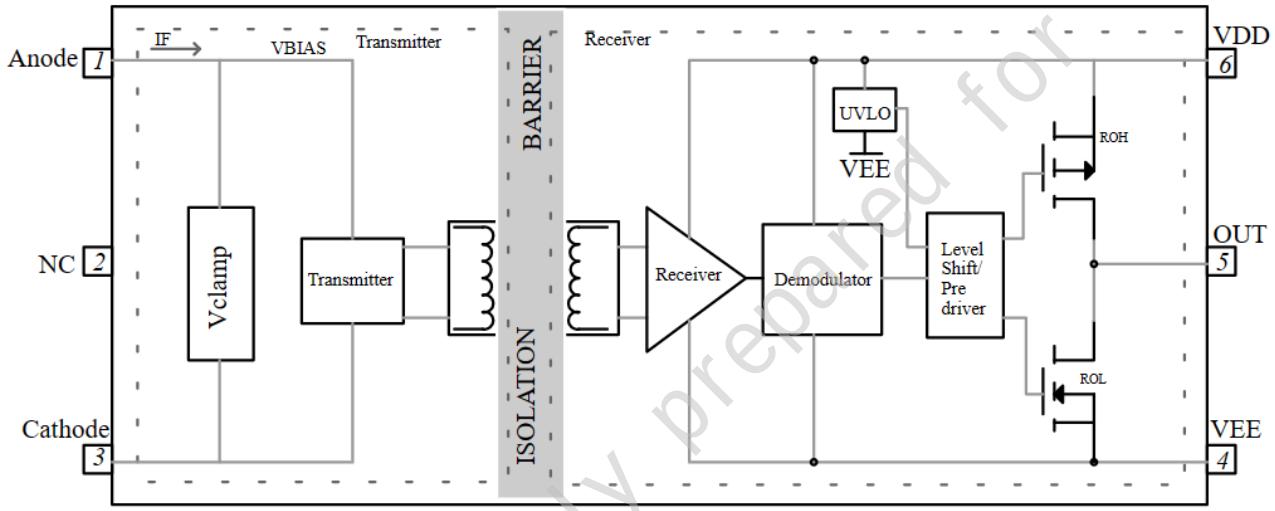
Figure 17 Simplified CMTI Testing Setup

9. Detailed Description

9.1 Overview

The MD18011A/B/C is an isolated single channel gate driver family designed with 4-A source current and 7-A sink current to drive MOSFET, IGBT and SiC MOSFET. The device's input is opto-compatible. The input side is isolated from the output side by 5.7kV$_{RMS}$ isolation barrier with a minimum of 200-V/ns common mode transient immunity. The inputs can handle -16V DC, which increases robustness against ringing from parasitic inductance of long routing traces.

9.2 Functional Block Diagram



9.3 Power supply and Undervoltage Lockout

The input of this device is an emulated diode, so no power supply is needed at the input side. MD18011A/B/C's driver side is powered by VDD pin. When VDD has a lower voltage than V_{DDR} during the VDD ramp up phase or VDD drops below V_{DDF}, the undervoltage lockout function is activated, holding the effected output low until the VDD voltage is greater than V_{DDR} again. The VDD UVLO hysteresis V_{DDHYS} is equal to V_{DDR} - V_{DDF}, which prevents output chattering caused by switching noise and sudden changes on operating current.

When VDD drops below V_{DDF} and the drop time is greater than 2us, T_{START_VDD} occurs on the output when the supply voltage rises above V_{DDR} again.

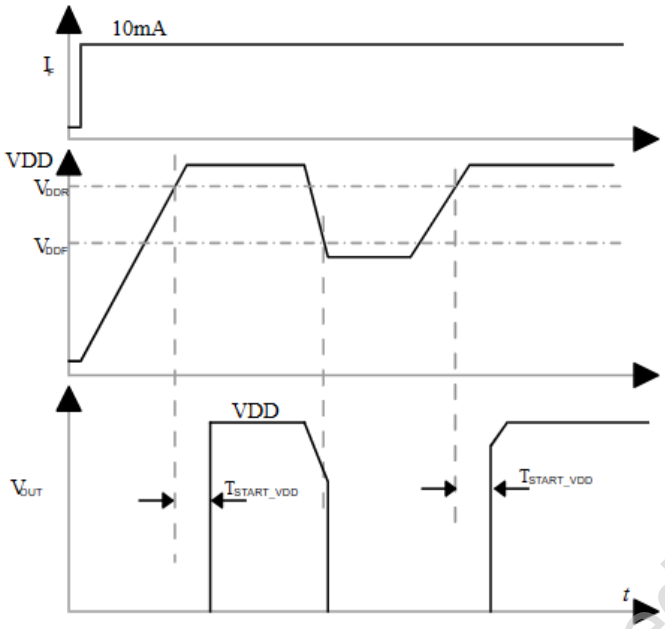


Figure 18 UVLO functionality

9.4 Input Stage

The input stage of MD18011A/B/C can be functionally simplified by an electronic diode with an anode (pin 1) and a cathode (pin 3). Pin 2 has no internal connection and can remain open or connected to ground. There are no power and ground pins in the input stage. When an electronic diode is forward biased by applying a positive voltage to the anode relatively to the cathode, a forward current I_F flows into the electronic diode. The forward voltage drop of the electronic diode is 1.2V. External resistors should be used to limit the forward current. The recommended range for forward current is 7mA to 16mA. When the I_F exceeds the threshold current I_{FLH} (1.5mA typical), the internally generated high-frequency signal is transmitted to the other side of the isolation barrier. The receiver detects the high-frequency signal and V_{OUT} is pulled up. The temperature coefficient of the forward voltage drop of the electronic diode is less than 0.7mV/°C. This results in very good stability of the forward current I_F under all operating conditions. If the anode voltage drops below V_{F_HL} (0.9V min) or is reverse-biased, the gate driver output is pulled low. The reverse breakdown voltage of the electronic diode is greater than 16V. Therefore, for normal operation, reverse bias up to 16V is allowed. The large reverse breakdown voltage of the electronic diode allows the MD18011A/B/C to operate in an interlocked architecture (see the example in **Figure 1**), where the VSUP can be as high as 12V. System designers have the flexibility to choose PWM sources of 3.3V, 5.0V, or up to 12V to drive the input stages of the MD18011A/B/C using the appropriate input resistors. The example shows two gate drivers driving a group of IGBTs. The input connection of the gate driver is shown in the diagram (**Figure 1**) and is driven by two buffers controlled by the MCU. The interlocking architecture prevents both electronic diodes from being "on" at the same time, thus preventing cross conduction in the IGBTs. It also ensures that if both PWM signals are mistakenly held high (or low) at the same time, the output of both gate drivers will be pulled low.

9.5 Output Stage

The output stage of MD18011A/B/C features the PMOS as pull up structure and the pull-down structure with NMOS. PMOS provides the pull up capability when Input is 'HIGH', and the R_{OH} parameter is a DC measurement which is representative of the on-resistance of the P-Channel device. N-MOS provides the pull-down capability when Input is 'LOW', the R_{OL} parameter is a DC measurement which is representative of the on-resistance of the N-Channel device.

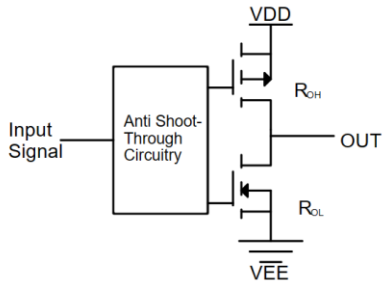


Figure 19 MD18011A/B/C Gate Driver Output Structure

Each output stage in MD18011A/B/C can supply 4-A peak source and 7-A peak sink current capabilities. The output voltage swings between VDD and VEE providing rail-to-rail operation, with very low drop-out due to low R_{OH} and R_{OL}.

10. Application and Implementation

10.1 Application Information

The MD18011A/B/C is a single channel, isolated gate driver with opto-compatible input for power semiconductor devices, such as MOSFETS, IGBTS, or SIC MOSFETS. It is intended for use in applications such as motor control, industrial inverters, and switched-mode power supplies. It differs from standard opto-coupled isolated gate drivers as it does not have a LED input stage, but an emulated diode (e-diode) instead. To turn the e-diode "ON", a forward current in the range of 7mA to 16mA should be driven into the Anode. This will drive the gate driver output High and turn on the power FETs. Typically, MCUs are not capable of providing the required forward current. Hence using a single NMOS and split resistor combination to drive the input stage of MD18011A/B/C (see **Figure 20**). A resistor is needed to limit the input current regardless of the supply voltage and anode (pin1) or between cathode (pin3) and the NMOS. The right value of resistance should be chosen to ensure that the e-diode forward current stays within the recommended range of 7mA to 16mA. The current driven input stage offers excellent noise immunity that is required in high power motor drive systems, especially in cases where the MCU cannot be located close to the isolated gate driver. MD18011A/B/C offers best in class CMTI performance of >200kV/us.

10.2 Typical Application

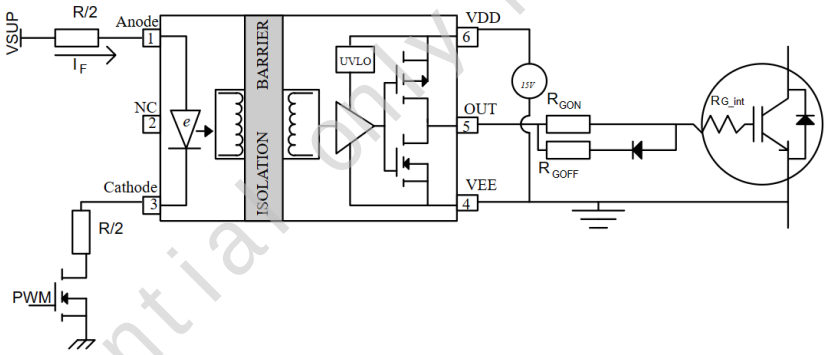


Figure 20 Typical Application Circuit for MD18011A/B/C to Drive IGBT

11. Layout

11.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the MD18011A/B/C. Some key guidelines are:

• Component placement:

– Low-ESR and low-ESL capacitors must be connected close to the device between the VDD and VEE pins to suppress switching spikes and to support high peak currents when turning on the external power devices.

– To avoid larger negative transient spikes on the VEE pins connected to the switch node, the parasitic inductances between the source of the top power device and the source of the bottom power device must be minimized.

• Grounding considerations:

– Limiting the high peak currents that charge and discharge the gates of the power devices to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the power devices. The gate driver must be placed as close as possible to the power devices.

• High-voltage considerations:

– To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended to prevent contamination that may compromise the isolation performance.

• Thermal considerations:

–Increasing the PCB copper connection to the VDD and VEE pins is recommended, with priority on maximizing the connection to VEE. However, the previously mentioned high-voltage PCB considerations must be maintained.

–If the system has multiple layers, we also recommend connecting the VDD and VEE pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no overlapping between traces or coppers from different high voltage planes.

11.2 Layout Example

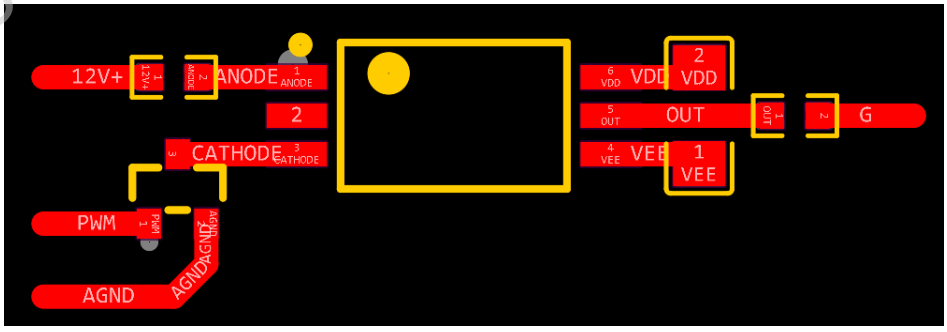


Figure 21 Layout Example

12. Mechanical Data and Land Pattern Data

12.1 Mechanical Packaging Data

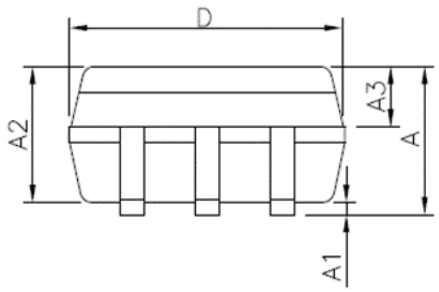


Figure 12.22 Side View

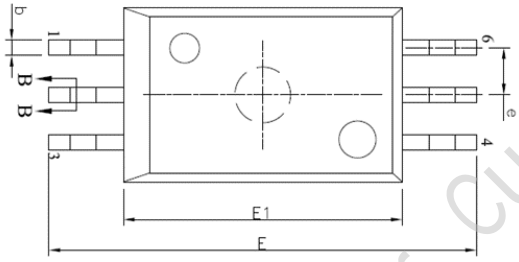


Figure 12.23 Top View

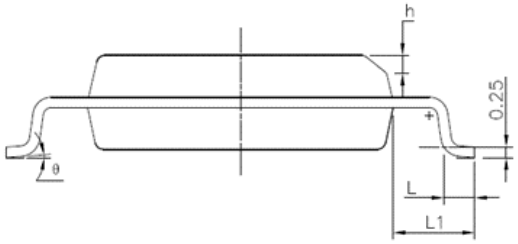


Figure 12.24 Side View

Symbol	Dimensions In Millimeters	
	MIN	MAX
A	-	2.65
A1	0.10	0.30
A2	2.25	2.35
b	0.39	0.47
C	0.25	0.29
D	4.58	4.78
E	11.3	11.7
E1	7.4	7.6
e	1.270(BSC)	
L	0.5	1
θ	0°	8°

Unit: mm

12.2 Land Pattern Data

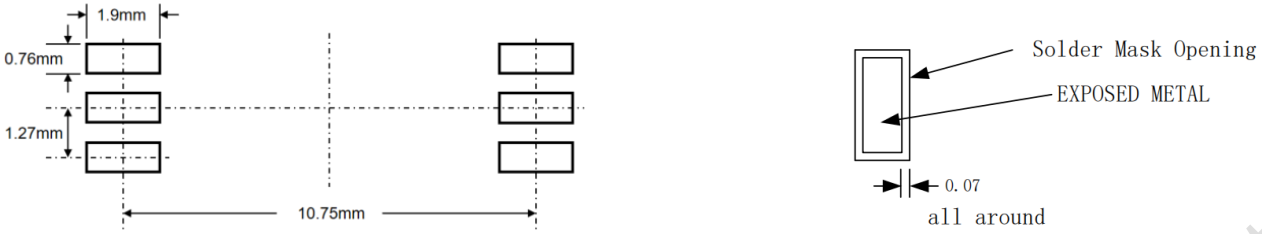


Figure 12.4 SOW-6 Land Pattern Data

13. Pin1 Information

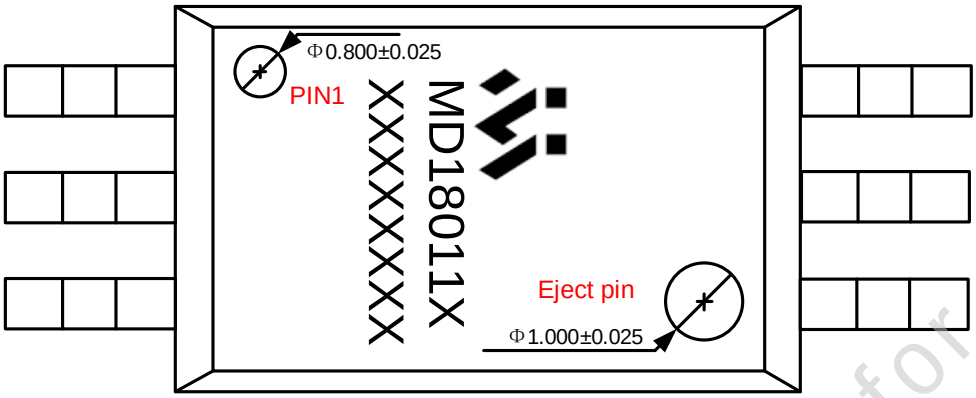


Figure 25 Pin1 information

14. Reel and Tape Information

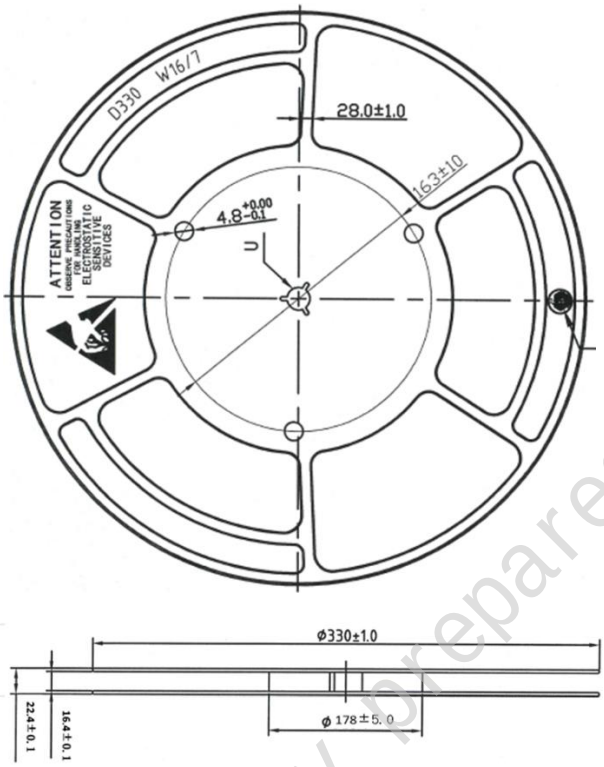
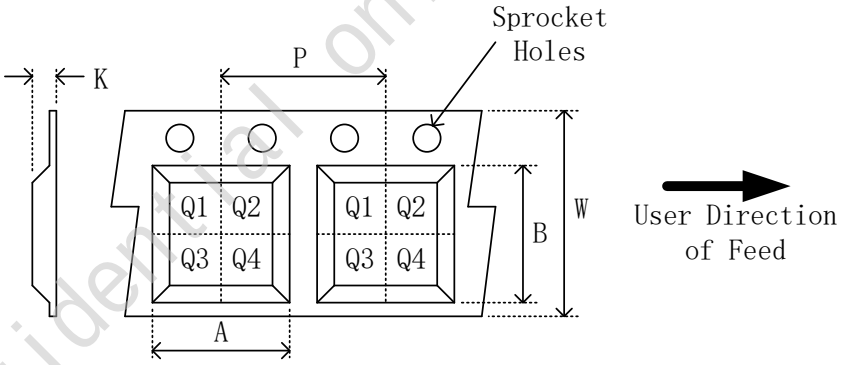


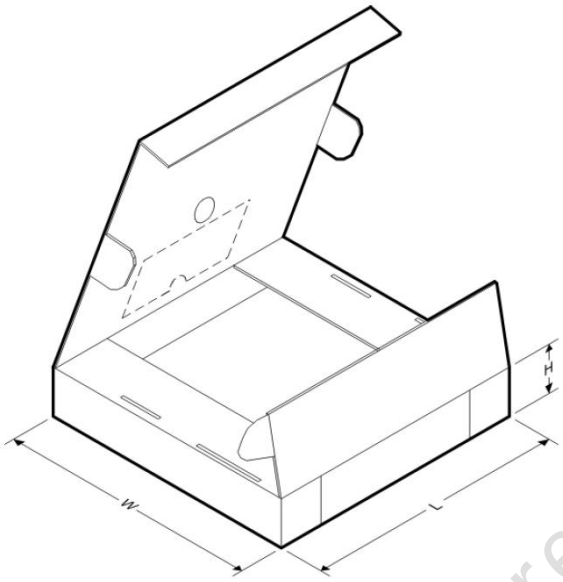
Figure 26 Reel Dimensions



Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	W (mm)	Pin1 Quadrant
MD18011AWAH	SOW-6	6	1000	11.95±0.1	5.1±0.1	3.0±0.1	16.0±0.1	16.0±0.1	Q1
MD18011BWAH	SOW-6	6	1000	11.95±0.1	5.1±0.1	3.0±0.1	16.0±0.1	16.0±0.1	Q1
MD18011CWAH	SOW-6	6	1000	11.95±0.1	5.1±0.1	3.0±0.1	16.0±0.1	16.0±0.1	Q1

Figure 27 Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

15. Tape and reel box dimensions



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MD18011AWAH	SOW-6	6	2000	360	360	65
MD18011BWAH	SOW-6	6	2000	360	360	65
MD18011CWAH	SOW-6	6	2000	360	360	65

Figure 28 Box Dimensions