MD18623 5-A Peak, High Frequency, Dual Low-Side Driver

1. Description

The MD18623 high-frequency gate driver is designed to drive both low-side N-Channel MOSFETs with maximum control flexibility of independent inputs.

Each channel can source and sink 5A peak current along with rail-to-rail output capability. Less than 10ns rise and fall time with 2.2nF load decrease the switching loss of MOSFET.

MD18623 has 11ns rising and falling propagation delay which allows the systems operating at high frequency with less delay matching variations. These delays are very suited for applications requiring dual-gate drivers with critical timing, such as synchronous rectifiers. When connecting two channels in parallel to increase current-drive capability, intelligent stack detection circuit is implemented to add extra 5ns dead-time between the two channels to avoid shoot through current without adding external series resistor.

The inputs can handle -10V to 20V PWM, which increases robustness against ringing from gate transformer and/or parasitic inductance of long routing traces. The input PINs thresholds are fixed and independent of the VDD supply voltage.

The MD18623 is offered in SOP-8 package

2. Typical Applications

- Power Supplies for Telecom, Datacom, and 48V to 72V Battery Powered Systems
- Switch-Mode Power Supplies
- Motor Control, Solar Power

3. Features

- 4.5V to 26V VDD Operating Range, 28V ABS MAX
- Input Pins Can Tolerate -10V to +26V, and are Independent of Supply Voltage Range
- Operating Switching Frequency up to 1MHz
- 5-A Source and Sink Output Peak Currents
- Less than 10ns Rise and Fall Time with 2.2nF Load
- Fast Propagation Delay (11ns Typical)
- Excellent Propagation Delay Matching (1ns Typical)
- TTL and CMOS Compatible Inputs
- Symmetrical Undervoltage Lockout for Channel A and Channel B
- Industry-standard-compatible Pinout
- Available in SOP-8 Package
- Specified from -40°C to 140°C

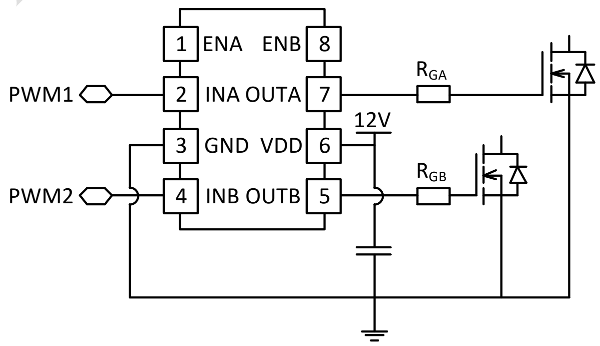
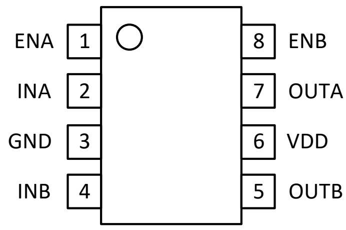


Figure 1. Typical Application Diagram

4. Order Information

Order Code	Package	Pins	SPQ (pcs)
MD18623GAA	SOP-8	8	4000

5. Package Reference And Pin Functions



SOP-8 (top view)

Pin Number	Name	Description
1	ENA	Enable input for Channel A: ENA biased LOW Disables Channel A output regardless of INA state, ENA biased HIGH or floating Enables Channel A output
2	INA	Inverting Input of Channel A
3	GND	Negative supply for the device that is generally grounded. All signals of the device are referenced to this ground
4	INB	Inverting Input of Channel B
5	OUTB	Output of Channel B
6	VDD	Positive gate drive supply. Locally decouple to VSS using low ESR/ESL capacitor located as close to the device as possible
7	OUTA	Output of Channel A
8	ENB	Enable input for Channel B: ENB biased LOW Disables Channel B output regardless of INB state, ENB biased HIGH or floating Enables Channel B output

6. Absolute Maximum Ratings [1]

VDD .... –0.3V to +28V
INA, INB, ENA, ENB .... –10V to +28V
OUTA, OUTB DC .... –0.3V to VDD+0.3V
Repetitive pulse [2] .... –2V to VDD+0.3V
Repetitive pulse [3] .... –5V to VDD+0.3V
Output continuous source/sink current 0.3A
Junction Temperature .... 150°C
Lead Temperature (Solder) .... 260°C
Storage Temperature .... –65°C to +150°C

7. Recommend Operation Conditions [4]

VDD .... 4.5V to 26V
INA, INB, ENA, ENB .... –5V to 26V
Maximum Junction Temp. (T_J) .... +140°C

8. Thermal Resistance [5]

	Θ_{JA}	Θ_{JC}	
SOP-8	130.9	80.0	°C/W

Notes:

(1) Exceeding these ratings may cause permanent damage to the device.

(2) Repetitive pulse ≤200ns. Verified at bench characterization.

(3) Repetitive pulse ≤100ns. Verified at bench characterization.

(4) The device is not guaranteed to function outside of its operating conditions.

(5) Measured on JEDEC, 1S0P PCB.

9. ESD Ratings

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [2]	±1000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

10. Electrical Characteristics

VDD=12V, T_A=T_J=-40°C to 140°C, 1uF capacitor from V_{DD} to GND. unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
VDD Start current	$I_{DD(off)}$	VDD = 3.4V INA = INB = VDD	20.7	38.7	56.6	uA
		VDD = 3.4V INA = INB = GND	20.8	38.6	56.4	uA
INPUTS(INA, INB, ENA, ENB)						
Input voltage rising threshold	V_{ITH}		1.94	2.14	2.34	V
Input voltage falling threshold	V_{ITL}		1.08	1.23	1.38	V
Input voltage hysteresis	V_{ITHYS}		0.74	0.91	1.08	V
UNDERVOLTAGE LOCKOUT						
VDD rising threshold	V_{DDR}		3.95	4.24	4.46	V
VDD falling threshold	V_{DDF}		3.66	3.93	4.14	V
VDD threshold hysteresis	V_{DDHYS}		0.21	0.31	0.41	V
OUTPUTS(OUTA, OUTB)						
Sink/Source peak current	I_{SNK} /I_{SRC}	C_{LOAD} = 0.22uF, F_{SW} = 1kHz		±5		A
High output voltage	V_{OH}	I_{OUT} = -10mA	VDD- 0.02		VDD	V
Low output voltage	V_{OL}	I_{OUT} = 10mA			0.016	V
Output pullup resistance	R_{OH}	I_{OUT} = -10mA	0.5	1	2	Ω
Output pulldown resistance	R_{OL}	I_{OUT} = 10mA	0.4	0.8	1.6	Ω
PROPAGATION DELAYS						
IN to OUT turn-on propagation delay	T_{D1}	C_{LOAD}=2.2nF, 5V input pulse	5	11	20	ns
IN to OUT turn-off propagation delay	T_{D2}	C_{LOAD}=2.2nF, 5V input pulse	5	11	20	ns
EN to OUT turn-on propagation delay	T_{D3}	C_{LOAD}=2.2nF, 5V EN pulse	5	11	20	ns
EN to OUT turn-off propagation delay	T_{D4}	C_{LOAD}=2.2nF, 5V EN pulse	5	11	20	ns
Delay matching between 2 channels	t_M	INA = INB, OUTA and OUTB at 50% transition point		1	4	ns
OUTPUT RISE AND FALL TIME						
Rise time	t_R	C_{LOAD}=2.2nF, from 10% to 90%		7.6	19	ns
Fall time	t_F			6.2	11	ns
MISCELLANEOUS						
Minimum input pulse width that changes the output				10	20	ns

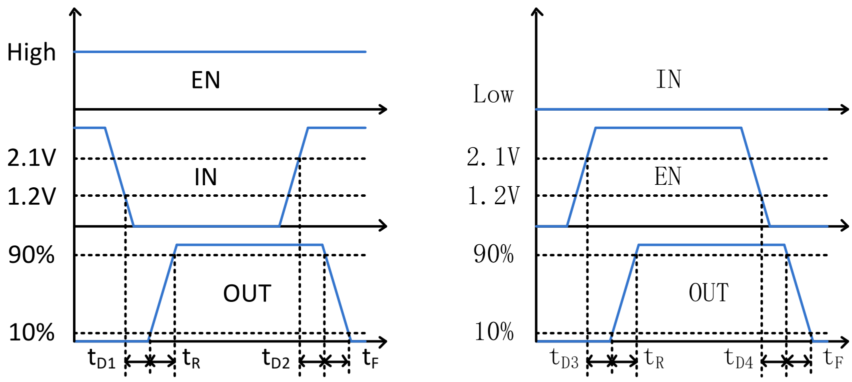


Figure 2. Timing Diagram

11. Typical Characteristics

VDD=3.4V, C_{L_OUTA}= C_{L_OUTB}=470pF

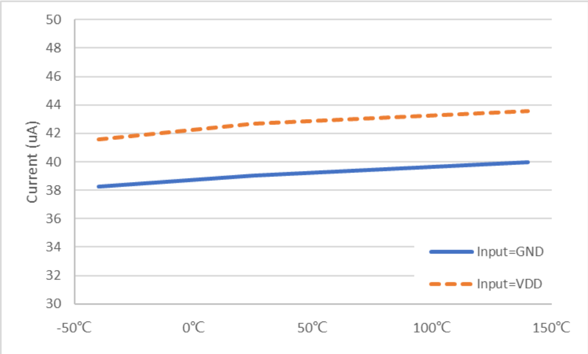


Figure 3. VDD Start Current vs Temperature

VDD=12V, f_{SW}=500kHz, C_{L_OUTA}= C_{L_OUTB}=470pF

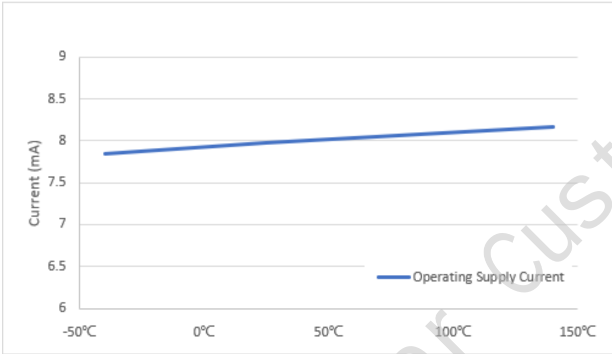


Figure 4. Operating Supply Current vs Temperature (Outputs Switching)

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=470pF

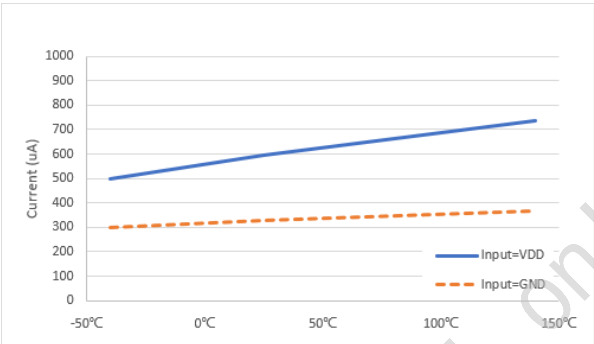


Figure 5. Operating Supply Current vs Temperature (Outputs No Switching)

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=470pF

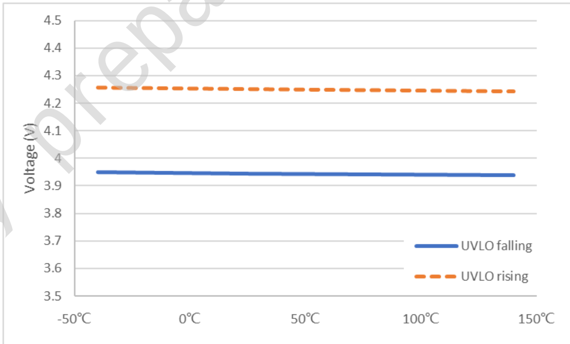


Figure 6. UVLO Threshold vs Temperature

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

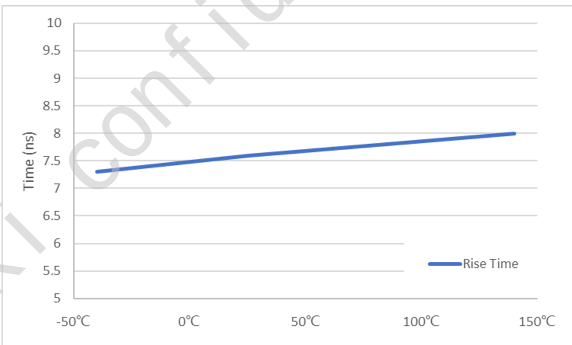


Figure 7. Output Rise Time vs Temperature 25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

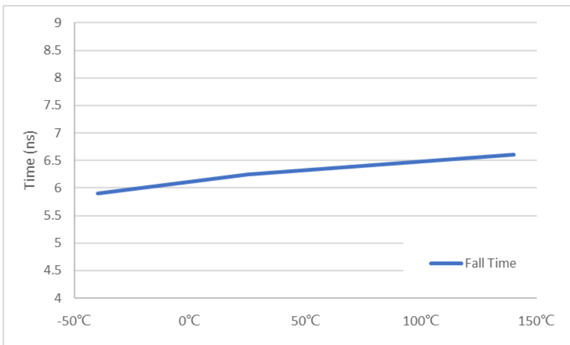


Figure 8. Output Fall Time vs Temperature VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

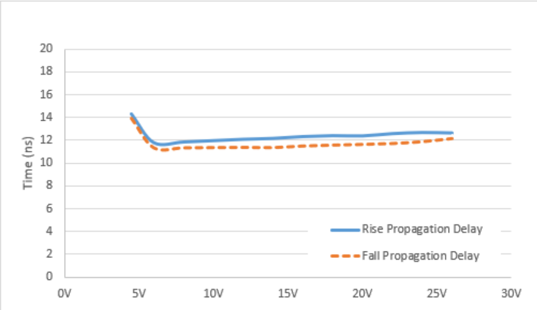


Figure 9. Input to Output Propagation Delays vs VDD Voltage

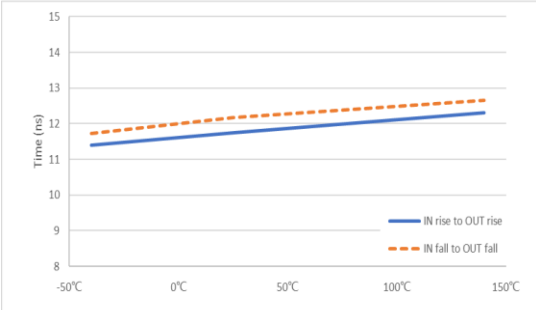


Figure 10. Input to Output Propagation Delay vs Temperature

25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

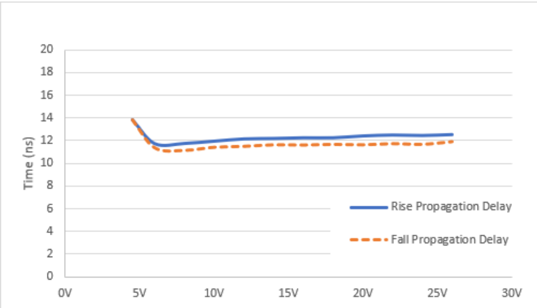


Figure 11. Enable to Output Propagation Delays vs VDD Voltage

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

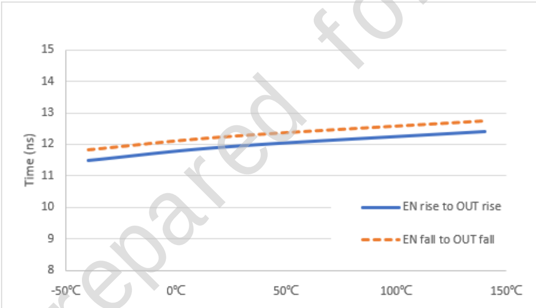


Figure 12. Enable to Output Propagation Delays vs Temperature

25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

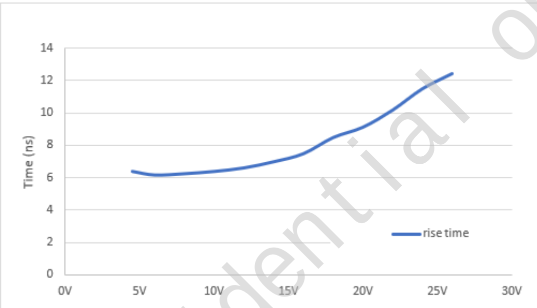


Figure 13. Output Rise time vs VDD Voltage

25℃, C_{L_OUTA}= C_{L_OUTB}=2.2nF

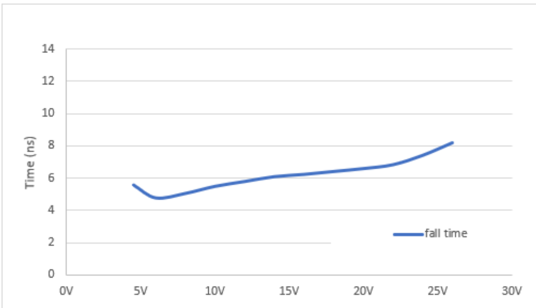


Figure 14. Output Fall time vs VDD Voltage

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

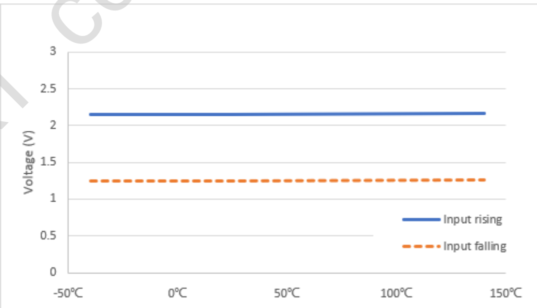


Figure 15. Input Threshold vs Temperature

VDD=12V, C_{L_OUTA}= C_{L_OUTB}=2.2nF

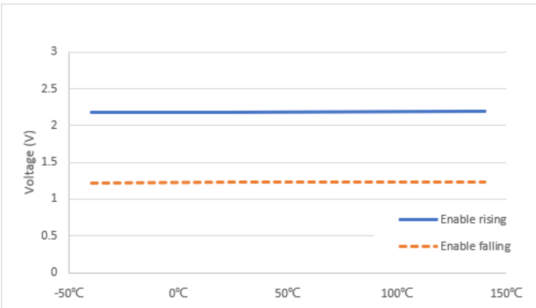


Figure 16. Enable Threshold vs Temperature

12. Block Diagram

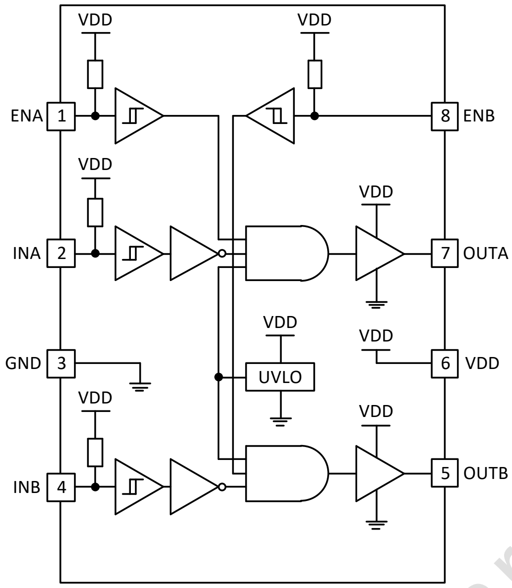


Figure 17. Functional Block Diagram

13. Operation

13.1 Overview

MD18623 is a dual-channel high-speed low-side driver with supporting up to 26V wide supply voltage. Each channel can source and sink 5A peak current along with the minimum propagation delay 11ns from input to output. The 1ns delay matching and 7ns switching time support higher switching frequency and driving capability. The ability to handle -10V DC input increases the noise immunity of driver input stage. The 26V rail-to-tail outputs can drive both MOSFET and IGBT.

13.2 Functional Modes

MD18623 operates in normal mode and UVLO mode. In the normal mode, the output state is dependent on states of the input pins. See as below:

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	H	H
H	H	L	H	H	L
H	H	H	L	L	H
H	H	H	H	L	L
L	L	Any	Any	L	L
Any	Any	X(1)	X(1)	L	L
X(1)	X(1)	L	L	H	H
X(1)	X(1)	L	H	H	L
X(1)	X(1)	H	L	L	H
X(1)	X(1)	H	H	L	L

Note: X = Floating condition

13.3 VDD power supply and Undervoltage Lockout (UVLO)

MD18623 operates with the supply voltage from 4.5V to 26V. This feature makes MD18623 be capable of driving both MOSFET and IGBT. For the best performance, Using a typical 0.1uF decoupling cap as close as possible between VDD and GND pins of MD18623. VDD bypass capacitor (1uF to 10uF) in parallel is also recommended to reduce noise ripple during switching.

MD18623 has internal UVLO protection feature In the VDD supply circuit blocks. When VDD is rising and the voltage is still below UVLO threshold, the outputs 'LOW', regardless of the status of the inputs. The UVLO is typically 4.2V with 0.3V hysteresis. This hysteresis prevents VDD from noise problem.

For example, at powering up, MD18623 output remains 'LOW' until the VDD voltage reaches the VDD rising threshold regardless of the status of inputs. At powering off, MD18623 also outputs low after the VDD voltage falls below VDD falling threshold.

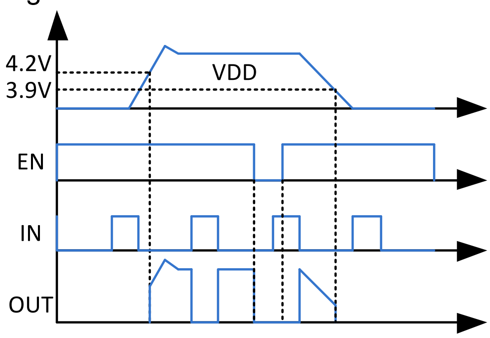


Figure 18. MD18623 operation sequence

13.4 Input Function

The input pins of MD18623 gate-driver device are based on a TTL and CMOS compatible input-threshold logic. That is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1.2 V, the logic level thresholds are conveniently driven by PWM control signals derived from 3.3-V and 5-V digital power-controller devices.

When the ENA and ENB pins are in a floating condition, Meraki-IC suggests that the ENA and ENB pins short to VDD pin directly.

13.5 Output Stage

The output stage of MD18623 features the pull up structure with P-MOS and the pull-down structure with N-MOS. P-MOS provides the pull up capability when Input is 'HIGH', and the ROH parameter is a DC measurement which is representative of the on-resistance of the P-Channel device. N-MOS provides the pull-down capability when Input is 'LOW', the ROL parameter is a DC measurement which is representative of the on-resistance of the N-Channel device.

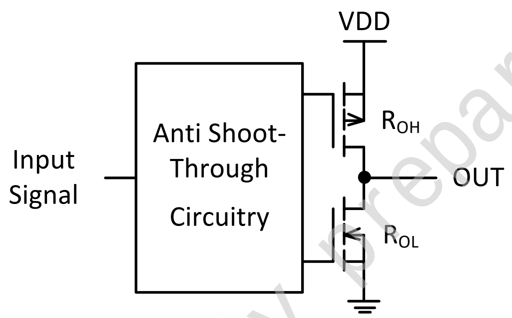


Figure 19. MD18623 Gate Driver Output Structure

Each output stage in MD18623 can supply 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low drop-out.

The MD18623 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This situation is due to the extremely low drop-out offered by the MOS output stage of MD18623, both during high (VOH) and low (VOL) states along with the low impedance of the driver output stage, all of which alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

MD18623 provides excellent output negative voltage handling capability, thanks to its high peak current driving capability and 4kV HBM and 1kV CDM ESD performance.

13.6 Output Parallel Capability

The MD18623 features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be paralleled when the driven power device required higher driving capability. For example, in the secondary of hard switching full bridge converter, there are two or more power MOSFETs in parallel to support high current output capability. The parallel power MOSFETs are preferred to be driven by a common gate control signal. By using MD18623, the OUTA and OUTB can be connected together to provide the higher driving capability, so does the INA and INB. To support the parallel output, intelligent stack detection is implemented. When two channels are connected together, internal circuit will recognize this parallel application and add extra 5ns dead-time to avoid shoot through.

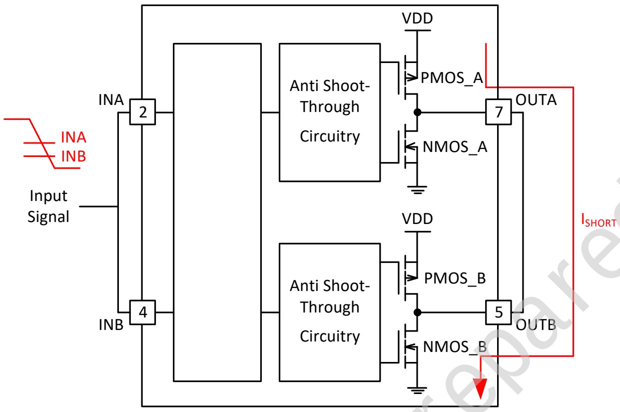


Figure 20. MD18623 Parallel Output Structure

Due to the rising and falling threshold mismatch between INA and INB, shoot through current conduction as shown in Figure 20 when directly connecting OUTA and OUTB pins. To avoid the shoot through current, intelligent stack detection is implemented. Extra 5ns dead-time is added between the two channels to cancel the delay between the two channels when slow dv/dt input signals are employed. No extra dead-time is added when the two channels parallel are not detected, so has no influence to propagation delay under normal operation. With the benefit of the intelligent stack detection circuit, MD18623 can support slow input signal slew rate (20V/us or greater) without external gate resistor in series with OUTA and OUTB, so wider application range and lower BOM count is obtained.

14. Application and Implementation

14.1 Typical Application

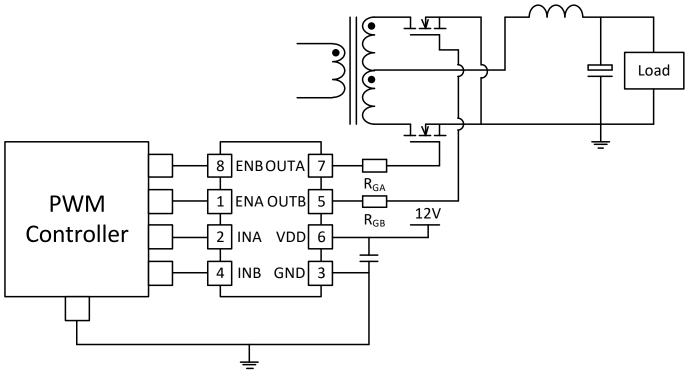


Figure 21. Synchronous Rectification Application

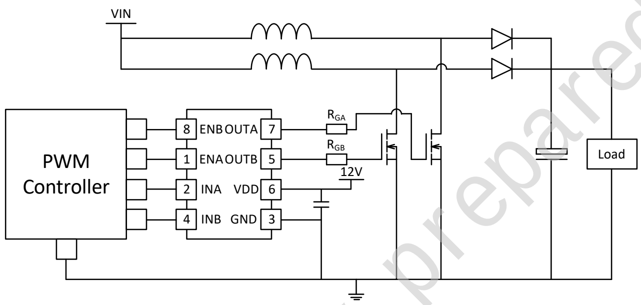


Figure 22. PFC Application

14.2 Driver Power Dissipation

Generally, the power dissipated in the MD18623 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The MD18623 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 1.

$$E_G = \frac{1}{2} \times C_{LOAD} \times V_{DD}^2 \qquad (1)$$

where

CLOAD is load capacitor

VDD is bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by Equation 2.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} \qquad (2)$$

where

fsw is the switching frequency

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge to switch the device under specified conditions. Using the gate charge Qg, the power that must be dissipated when charging a capacitor is determined which by using the Equation 3 to provide Equation 4 for power:

$$Q_G = C_{LOAD} \times V_{DD} \quad (3)$$

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_g \times V_{DD} \times f_{SW} \quad (4)$$

To decrease the stress of MOSFET, adding a gate resistor between output of MD18623 and gate of MOSFET, and the power loss of resistor is given by Equation 5.

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{SW} \times (\frac{R_{OL}}{R_{OL}+R_{GATE}} + \frac{R_{OH}}{R_{OH}+R_{GATE}}) \quad (5)$$

15. Layout

15.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

1) Locate the driver close to the MOSFETs.
2) Locate the VDD-VSS capacitors close to the driver.
3) Connect the VSS pin to thermal pad and use the thermal pad as GND. The GND trace from MD18623 does directly to the source of the MOSFET, but not be in the high current path of MOSFET source current.
4) For system using multiple drivers, the decoupling capacitors need to be located at VDD-VSS for each driver.
5) Avoid placing VDD, INA, INB, ENA, ENB trace close to OUTA, OUTB signals or any other high dV/dT traces that can induce significant noise into the high impedance leads.
6) Use wide trace for INA, INB, ENA, ENB to decrease the influence of switching ringing made by parasitic inductance.
7) For GND, the number of vias must be a consideration of the thermal pad requirements as well as parasitic inductance.

15.2 Layout Example

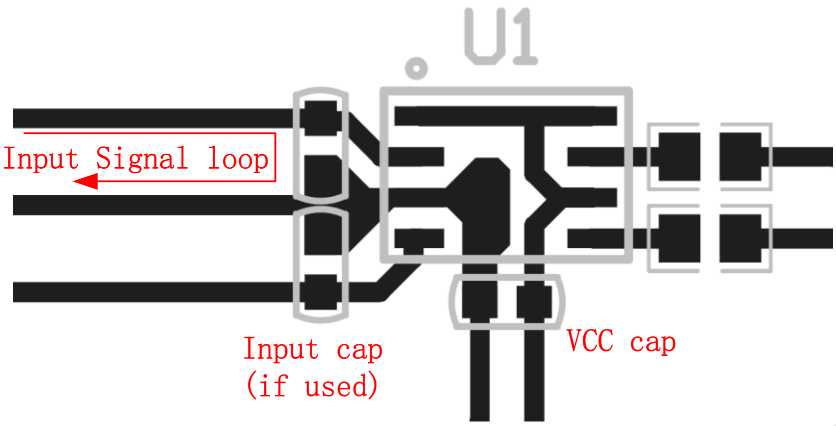


Figure 23. PCB Layout Example for SOP-8 Package

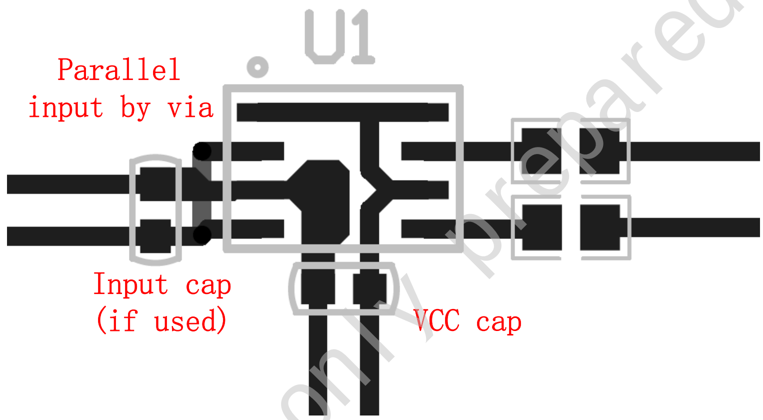


Figure 24. PCB Layout Example with Paralleled Inputs for SOP-8 Package

16. Tape and Reel Information

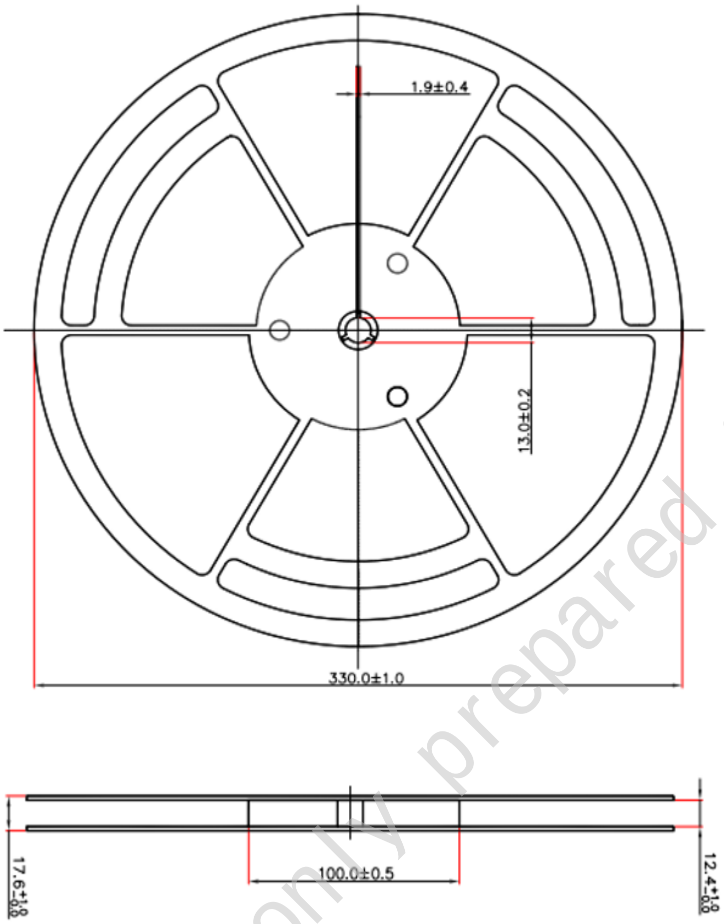
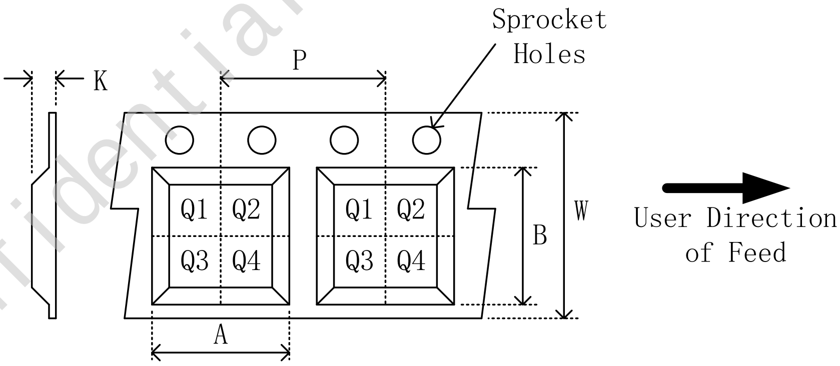


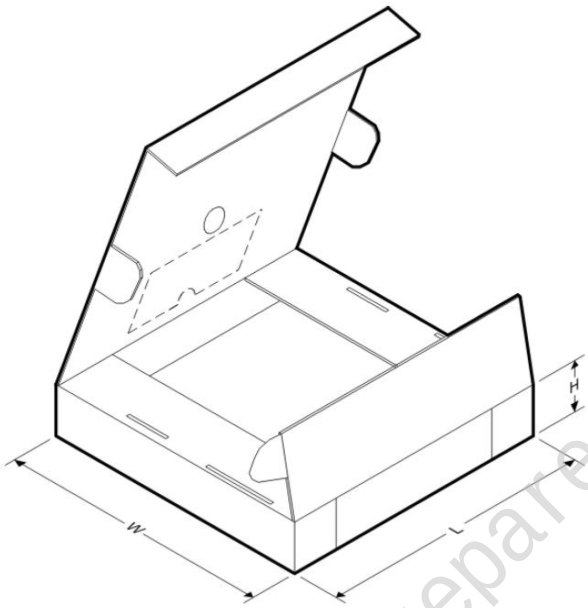
Figure 25. Reel Dimensions



Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	W (mm)	Pin1 Quadrant
MD18623GAA	SOP	8	4000	6.4	5.4	2.1	8.0	12.0	Q1

Figure 26. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

17. Tape and Reel Box Dimensions



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MD18623GAA	SOP-8	8	8000	360	360	65

Figure 27. Box Dimensions

18. Mechanical Data and Land Pattern Data

18.1 SOP-8

18.2 Mechanical Data

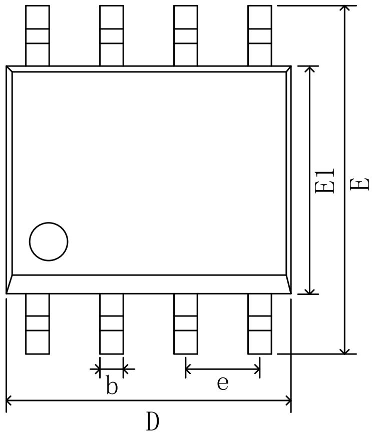


Figure 28. SOP-8 Top View

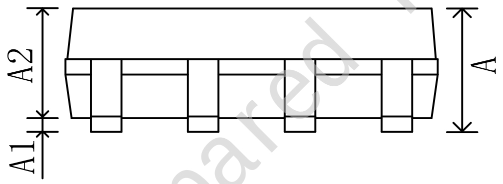


Figure 29. SOP-8 Side View

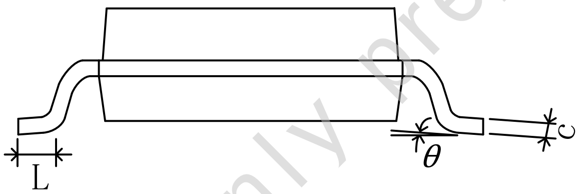


Figure 30. SOP-8 Side View

SYMBOL	Millimeter	
	MIN	MAX
A	1.45	1.75
A1	0.10	0.25
A2	1.35	1.55
b	0.33	0.51
c	0.17	0.25
D	4.70	5.10
E	5.80	6.20
E1	3.80	4.00
e	1.270(BSC)	
L	0.40	1.27
θ	0°	8°

18.3 Land Pattern Data

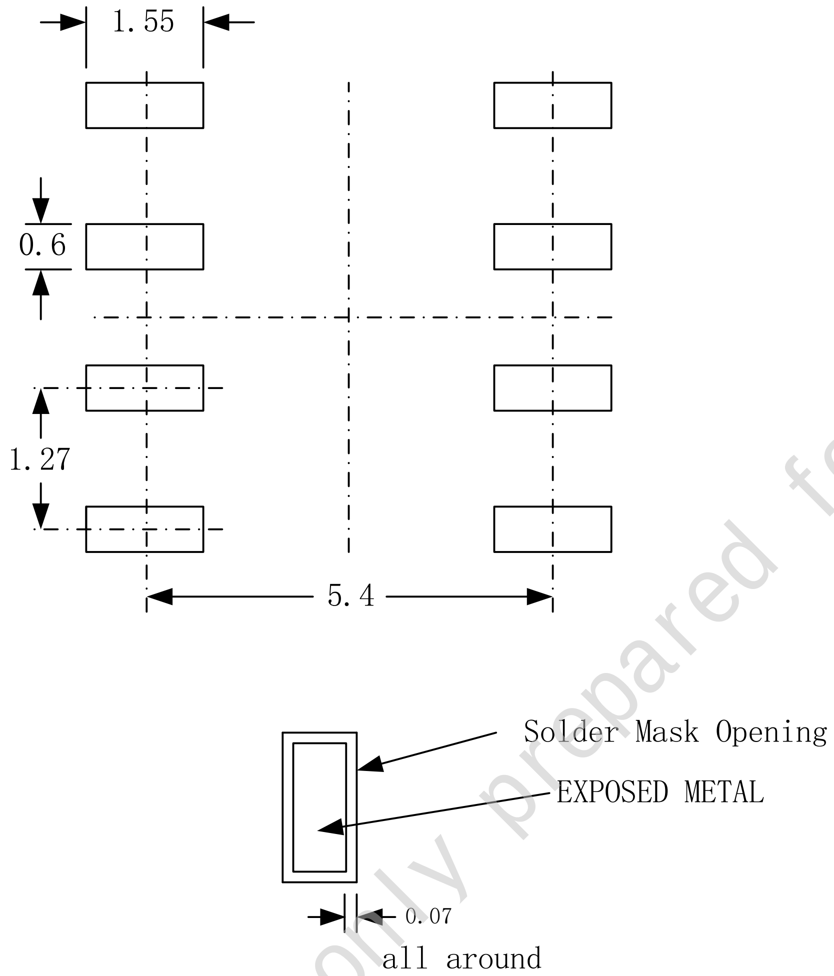


Figure 31. SOP-8 Land Pattern Data