Single-Channel Synchronous Rectifier Controller

1. Description

The MK1170-Q1 is a single-channel synchronous rectifier (SR) controller for flyback, forward and half-bridge converter. With appropriate gate drive method and independent sampling input, the MK1170-Q1 can achieve maximum efficiency under different load conditions.

The extremely low turn−off propagation delay time and high sink current (~4A) capability of the driver reduce SR MOSFET VDS stress. With 4A source current capability, the IC can control one or more paralleled N-Channel MOSFETs to emulate the behavior of Schottky diode rectifiers. The unique VG clamping circuit prevents VG from turning on by fast rising at VD pin under low VCC condition, that avoids the shoot through between primary side and secondary side during system startup. The advanced control strategy of MK1170-Q1 allows for stable SR operation over entire load range. The SYNC pin can directly turn off MOSFETs through signals from the secondary or primary controller. By using the MODE pin, MK1170-Q1 can freely switch between SR mode and DRIVER mode, making system applications more flexible.

2. Applications

- Automotive DC-DC converters
- High power industrial SMPS
- High performance server power supply

3. Features

- Wide VCC Voltage Range from 12V-26V
- Ultra-Low Quiescent Current <70uA
- 22ns Fast Turn-off Propagation Delay Time
- VGA Clamping Circuit for Low Vth SR MOSFET
- Maximum Voltage at VD PIN 115V
- -3V Drain Voltage Spike Tolerance
- True Differential Inputs for VDS Sensing of SR MOSFET
- CCM Operation with SYNC Function
- Switch Freely Between DRIVER Mode and SR Mode
- 4A Source and Sink Output Peak Currents
- Enable Features and Cycle by Cycle MOT Check Circuit
- Available in ESOP-8 Package
- Qualified for Automotive Applications

4. Typical Application

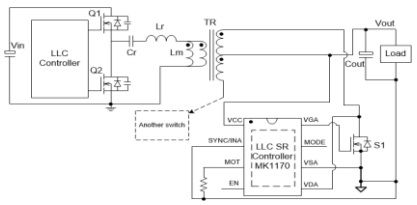


Figure 1. Typical Application Diagram

5. Order Information

Order Part Number	Descriptions
MK1170XAD-Q1	ESOP-8, tape, 4000 pcs/reel

6. Pin Configuration and Functions

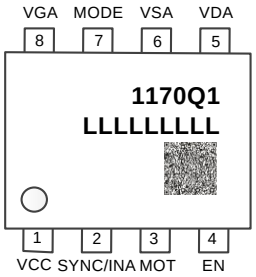


Figure 2. Pin Function (top view)

Table 1. Pin Functions

Pin		Descriptions
NO.	Name	
1	VCC	Supply voltage.
2	SYNC/INA	SYNC Input for direct turn off (SR mode); Input of driver (DRIVER mode).
3	MOT	Minimum on time (SR mode).
4	EN	Enable.
5	VDA	MOSFET drain sense input (SR mode).
6	VSA	Ground, also used as MOSFET source sense input.
7	MODE	Mode selection (SR or DRIVER).
8	VGA	MOSFET gate drive output.
	EspPad	at VSA potential, use only for thermal dissipation.

7. Specifications

7.1 Absolute Maximum Ratings (1)

Symbol	Parameter	MIN	MAX	Units
VCC	supply voltage VCC	-0.3	28	V
VGA (2)	voltage on pin VGA (DC)	-0.3	18	
	voltage on pin VGA (Pulse)	-2	18	
VDA	drain sense voltage VDA	-1	105	
VDA (3)	drain sense voltage VDA	-3	115	
SYNC/INA, EN, MODE	input voltage	-10	28	
T_J	operating junction temperature,	-40	150	°C
T_{stg}	storage temperature	-55	150	
T_{sld}	soldering temperature (10 second)		260	

Notes:

(1) Stresses beyond the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in "RECOMMENED OPERATING CONDITIONS". Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Output pin not to be voltage driven.

(3) Repetitive Pulse<200ns.

7.2 ESD Ratings

		Value	Units
Electrostatic discharge V_{ESD}	ESD Susceptibility all Pins (HBM) (1)	±2500	V
	ESD Susceptibility all Pins (CDM) (2)	±2000	V

Notes:

(1) ESD Susceptibility, Human Body Model "HBM", according to AEC-Q100-002.

(2) ESD Susceptibility, Charged Device Model "CDM", according to AEC-Q100-011.

7.3 Recommended Operating Conditions

		MIN	MAX	Units
Recommended Operation Conditions	VCC supply voltage	12	26	V
	drain sense voltage VDA and VDB	-0.7	100	V
	Input voltage, SYNC/INA, MODE, EN	-5	20	V
	MOT pin resistor value	5	75	kΩ
	operating junction temperature. (T_J)	-40	125	°C

7.4 Thermal Information

		Value	Units
Package Thermal Resistance (1)	θ_{JA} (Junction to ambient)	49	°C/W
	θ_{JC} (Junction to case)	15	

Note:

(1) Measured on JESD51-7, 4-layer PCB.

7.5 Electrical Characteristics

-40°C ≤ T_A = T_J ≤ 125°C. All Voltages are measured with respect to ground (pin 6). Currents are positive when flowing into the IC, unless otherwise specified.

Parameter		Test Conditions	MIN	TYP	MAX	Units
Supply Voltage Management						
V_{CC-ON}	VCC UVLO rising		10.0	10.5	11.0	V
V_{CC-OFF}	VCC UVLO falling		8.7	9.3	9.8	V
$V_{CC-HYST}$	VCC UVLO hysteresis			1.2		V
I_{CCQ}	VCC quiescent supply current	VCC = 9V, EN = 9V, SYNC/INA = 9V, VDA = 10V, R_{MOT} = 75kΩ		49	95	µA
		VCC = 12V, EN = 0V, SYNC/INA = 0V, VDA = 10V		175	280	µA
I_{CC}	Operating supply current	VCC = 12V, EN = 12V, R_{MODE} = 75kΩ, VDA = 10V, SYNC/INA = 12V		0.33	0.52	mA
		VCC = 12V, EN=12V, C_{LOAD} = 2.2nF, MODE = 0V, VDA = 10V, R_{MODE} = 75kΩ, F_{SW}=100kHz		3.5	5.4	mA
Synchronous Rectification Sense Input						
V_{DS-reg}	V_{DA} – V_{SA} Adjusting voltage	VCC = 12V		-10		mV
V_{ON-th}	V_{DA} – V_{SA} Turn-on threshold voltage	VCC = 12V	-350	-290	-250	mV
V_{OFF-th}	V_{DA} – V_{SA} Turn-off threshold voltage	VCC = 12V	10	48	86	mV
T_{D-on}	Turn-on propagation delay time	VCC = 12V, C_{LOAD} = 0nF, VDA step down from 5V to -0.8V, measure VGA rising to 1.5V		167	220	ns
T_{D-off}	Turn-off propagation delay time	VCC = 12V, C_{LOAD} = 0nF, VDA step up from -0.8V to 5V, measure VGA falling to 10.5		22	30	ns
Turn-on Blanking Time and Turn-off Blanking Time						
T_{B-on}	Turn-on blanking time (1)	R_{MOT} = 30kΩ		1.3		µs
T_{B-on}	Turn-on blanking time	R_{MOT} = 75kΩ	2.4	3.0	3.6	µs

T_{B-off}	Turn-off blanking time (1)	R_{MOT} = 30kΩ		1.65		µs
T_{B-off}	Turn-off blanking time	R_{MOT} = 75kΩ	3.2	3.75	4.8	µs
V_{B-off}	V_{DA} – V_{SA} Turn-off threshold during turn-on blanking time (1)			1.0		V
SYNC and INA Section						
V_{SIHI}	SYNC/INA Voltage High		1.8	2.1	2.3	V
V_{SILO}	SYNC/INA Voltage Low		0.9	1.1	1.3	V
V_{SIHYS}	SYNC/INA hysteresis			1		V
T_{SYON}	SYNC Turn-on Prop. Delay	SYNC = high to low C_{LOAD} = 2.2nF		87	105	ns
T_{SYOFF}	SYNC Turn-off Prop. Delay	SYNC = low to high C_{LOAD} = 2.2nF		83	100	ns
T_{INON}	INA Turn-on Prop. Delay	INA = high to low C_{LOAD} = 2.2nF	5	22	40	ns
T_{INOFF}	INA Turn-off Prop. Delay	INA = low to high C_{LOAD} = 2.2nF	5	27	45	ns
T_{SYPWf}	Minimum SYNC Pulse Width	VCC = 16V, EN = 16V		70		ns
T_{INPWf}	Minimum INA Pulse Width	VCC = 16V, EN = 16V, SYNC = 0V		25		ns
Enable and Mode Section						
V_{ENHI}	Enable Voltage High		1.8	2.1	2.3	V
V_{ENLO}	Enable Voltage Low		0.9	1.1	1.3	V
V_{ENHYS}	Enable hysteresis			1		V
T_{ENON}	Enable Turn-on Prop. Delay			21		µs
T_{ENOFF}	Enable Turn-off Prop. Delay			390		ns
V_{MOHI_SR}	MODE Voltage High (SR mode)		1.8	2.1	2.3	V
V_{MOLO_DR}	MODE Voltage		0.9	1.1	1.3	V

	Low (DRIVER mode)					
V_{MOHYS}	MODE hysteresis			1		V
T_{MOSR}	SR Mode Prop. Delay		7	11	15	µs
T_{MODR}	DRIVER Mode Prop. Delay		8	12	17	µs
Gate Driver						
V_{G-H}(high)	Gate High Voltage	VCC = 16V, C_{LOAD} = 10nF, R_{LOAD} = 10kΩ	11	12	13	V
V_{G-L}(low)	Gate Low Voltage	I_{GATE} = 100mA, VCC = 12V		0.06	0.1	V
I_{VG-H}	Maximum source current (1)			4		A
I_{VG-L}	Maximum sink current (1)			4		A
R_{sink}	Pull-down impedance	I_{GATE} = 100mA		0.6		Ω

Note:

(1) Values are verified by characterization on bench, not tested in production.

7.6 Typical Characteristics

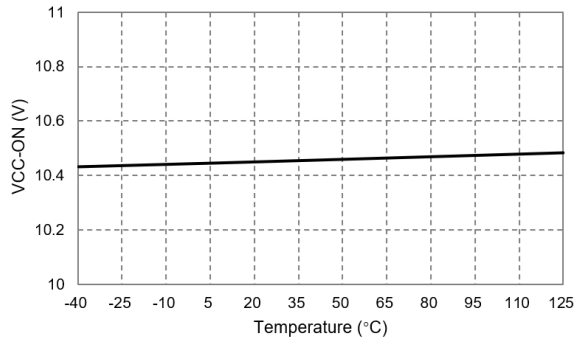


Figure 3. VCC UVLO Rising vs Temperature

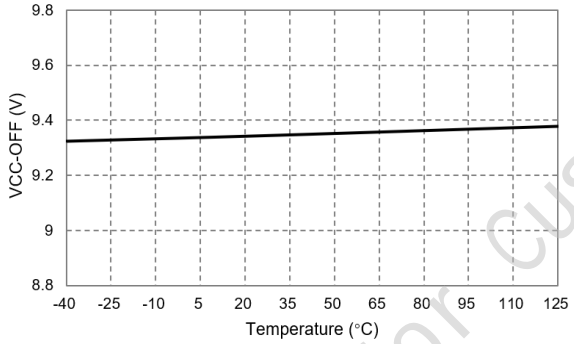


Figure 4. VCC UVLO Falling vs Temperature

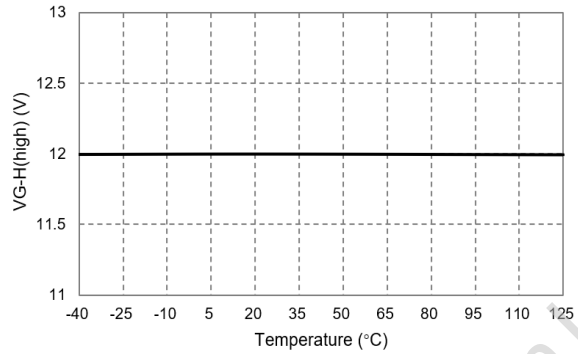


Figure 5. Gate High Voltage vs Temperature

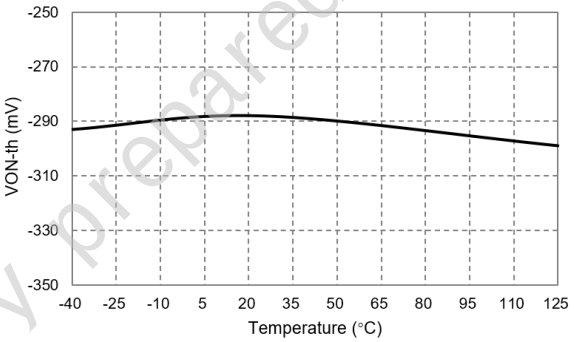


Figure 6. V_{DA} – V_{SA} Turn-on Threshold Voltage vs Temperature

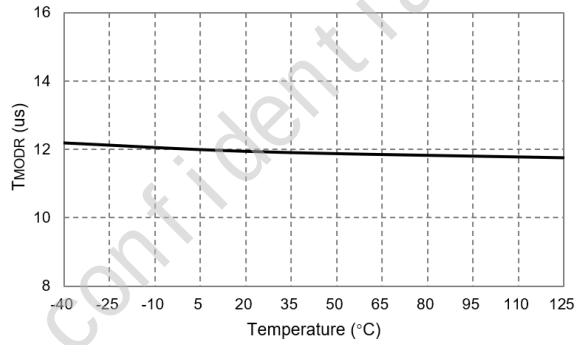


Figure 7. DRIVER Mode Propagation Delay Time vs Temperature

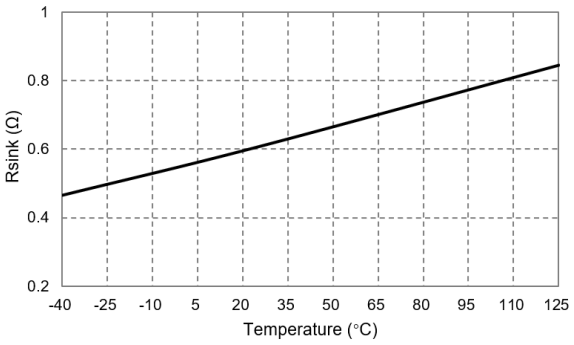


Figure 8. Pull-down Impedance vs Temperature

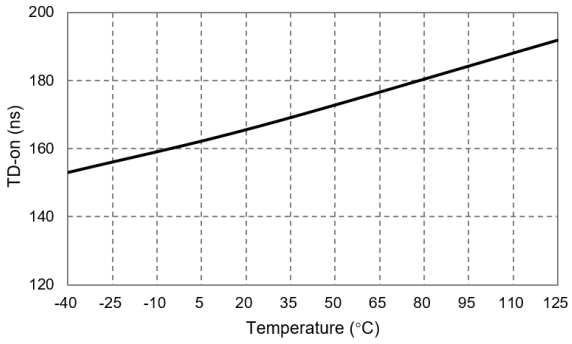


Figure 9. Turn-on Propagation Delay Time vs Temperature

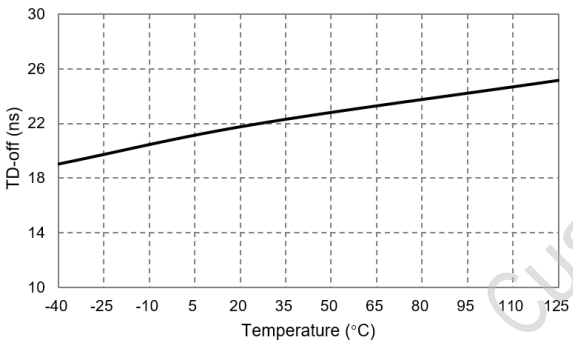


Figure 10. Turn-off Propagation Delay Time vs Temperature

Vout=14V, Iout=30A

Figure 11. Operation in 2kW LLC Converter

Vout=14V, Iout=50A

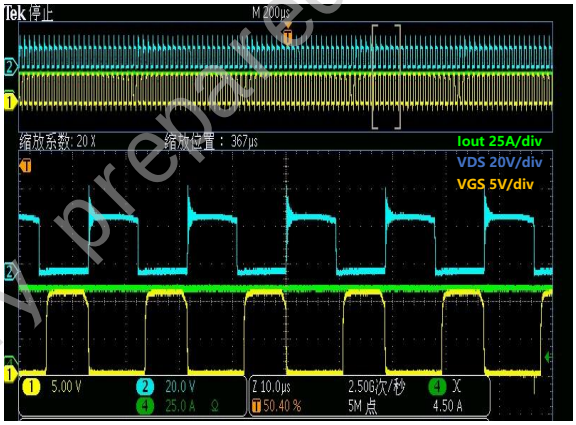


Figure 12. Operation in 2kW LLC Converter

Vout=14V, Iout=70A

Figure 13. Operation in 2kW LLC Converter

Vout=14V, Iout=140A

Figure 14. Operation in 2kW LLC Converter

8. Detailed Description

8.1 Overview

The MK1170-Q1 is a single-channel synchronous rectifier controller capable of driving N-Channel power MOSFETs in isolated resonant, flyback and forward converters. This controller has a differential sampling input to detect the voltage difference between the drain and source of SR MOSFET.

The gate voltage is adjusted consistently with the VDS voltage, which makes the chip easy to use. The unique VG clamping circuit works well to prevent VG from turning on by quickly rising at the VD pin with no VCC voltage. Extremely low turn−off propagation delay time and high sink current (~4A) capability of the driver reduce SR MOSFET VDS stress.

The advanced control scheme of MK1170-Q1 allows for stable SR operation over entire load range. The SYNC pin can directly turn off MOSFETs through signals from the secondary or primary controller. By using the MODE pin, MK1170-Q1 can freely switch between SR mode and DRIVER mode, making system applications more flexible.

8.2 Functional Block Diagram

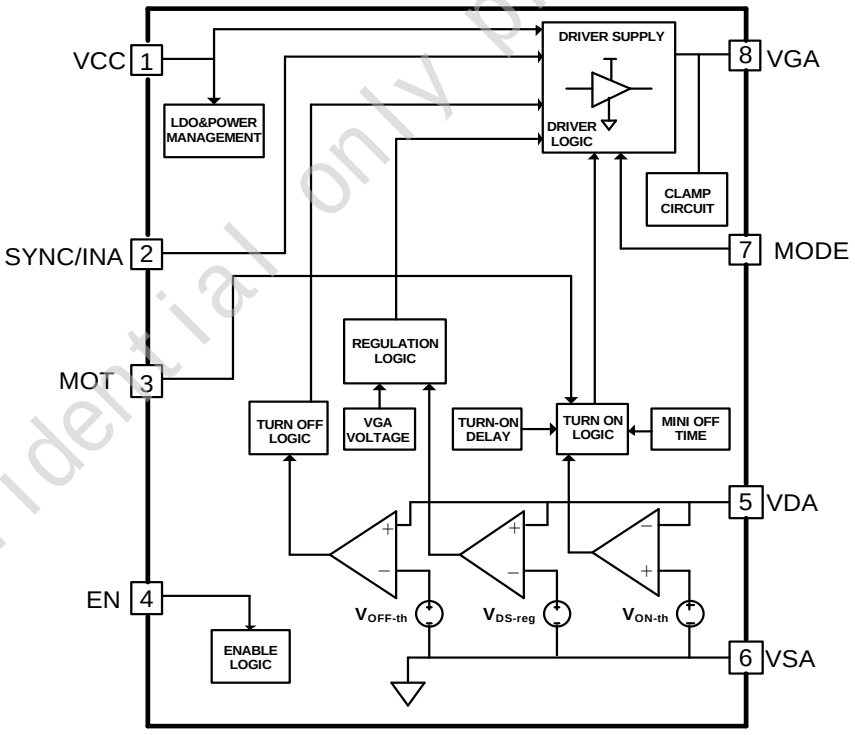


Figure 15. Block Diagram

8.3 Feature Description

8.3.1 VCC Power Supply and Undervoltage Lockout

The MK1170-Q1 operates from a supply voltage of 12V to 26V. This feature makes MK1170-Q1 suitable for a variety of application scenarios. For the best performance, use a typical 0.1uF decoupling capacitor as close as possible between the VCC and VSA pins of MK1170-Q1. A VCC bypass capacitor (1uF to 10uF) in parallel to the decoupling capacitor is also recommended to reduce noise ripple during switching.

MK1170-Q1 has an internal undervoltage lockout (UVLO) protection feature in the VCC supply circuit blocks. When the voltage on the VCC pin exceeds $V_{CC\text{-}ON}$, the controller leaves the UVLO state. When VCC voltage drops to below $V_{CC\text{-}OFF}$, the controller re-enters the UVLO state.

8.3.2 Enable Function

The EN pin is used to disable the IC by pulling the voltage level below V_{ENLO} and after a T_{ENOFF} delay. When the IC is disabled, all switching functions will be disabled and the gate will be inactive. When the voltage of EN pin is higher than V_{ENHI}, and after a T_{ENON} delay, the IC is enabled. The timing diagram is shown on Figure16.

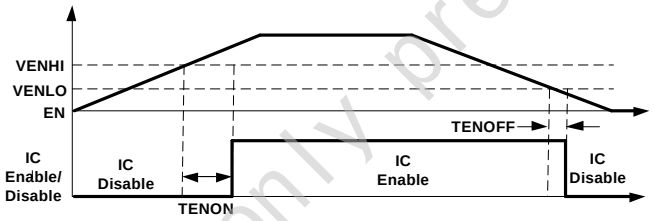


Figure 16. Enable Function Timing Diagram

8.3.3 Mode Function

Using the MODE pin, MK1170-Q1 can freely switch between SR mode and DRIVER mode. When the MODE pin floating or MODE pin voltage is higher than V_{MOHI_SR} and after a T_{MOSR} delay, MK1170-Q1 operates in SR mode. In SR mode, SYNC, MOT and VDA functions are effective. The gate voltage is adjusted consistently with the MOSFET VDS voltage.

The DRIVER mode is enabled by pulling the MODE pin voltage level below V_{MOLO_DR} and after a T_{MODR} delay. In DRIVER mode, INA function is effective, in which the gate output VGA follows the INA signal that is the non-inverting input of the MK1170-Q1 device. The timing diagram is shown on Figure17.

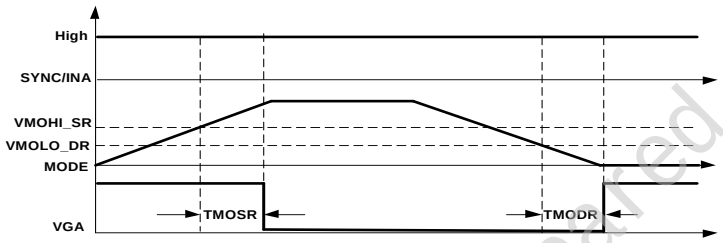


Figure 17. Mode Function Timing Diagram

8.3.4 MOT Function

In SR mode, the MOT programming pin controls the amount of turn-on blanking time and turn-off blanking time. After SR MOSFET turns on, a turn-on blanking time $T_{B\text{-}on}$ is required to prevent the IC from falsely turning off SR MOSFET by parasitic ringing. During the turn-on blanking time, the turn-off threshold increases to $V_{B\text{-}off}$.

After SR MOSFET turns off, a minimum turn-off blanking time $T_{B\text{-}off}$ is required, which helps to reduce the chances of false triggering in DCM. The turn-on blanking time is programmed between 200ns and 3us (typical) by using a resistor referenced to VSA according to the following formula:

$$R_{MOT} \approx 2.5 * 10\text{^}10 * T_{B-on}$$

$$T_{B-off} \approx 1.3 * T_{B-on}$$

8.3.5 SYNC/INA Function

SYNC/INA is a multi-function pin. In SR mode, SYNC function is effective, which can directly turn-off the SR MOSFET by an external signal. The gate output VGA is low when SYNC voltage is higher than V_{SIHI} threshold. The propagation delay from SYNC goes high to gate turns off is 100ns maximum. The gate turns off by SYNC signal is a dominant control, which overrides the turn-on blanking time and turn-off blanking time control.

In DRIVER mode, the gate output VGA is controlled by INA signal directly, which is typically an external PWM control signal. The logic level thresholds are TTL compatible, which is conveniently driven by PWM control signal derived from 3.3V and 5V digital power controller devices. The INA and EN function timing diagram is shown on Figure18.

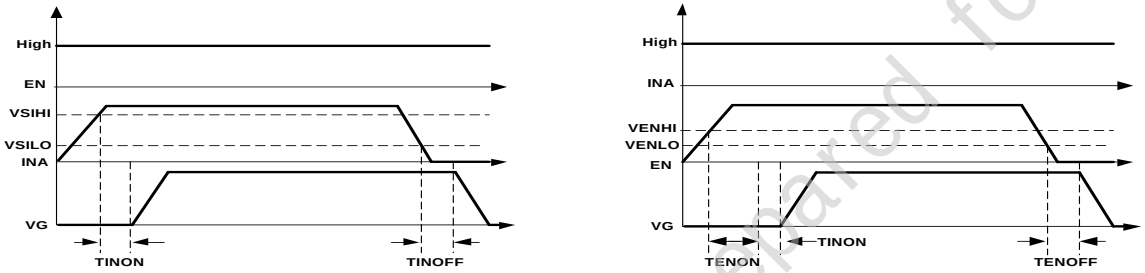


Figure 18. INA and EN Function Timing Diagram

8.3.6 SR Conduction Phase

When the IC is enabled and in SR mode, SYNC function is effective. The gate driver output of MK1170-Q1 is turned on when the SYNC voltage is below V_{SILO} and lasts a T_{MODR} delay, and the absolute voltage difference of SR MOSFET VDS (VDA-VSA) is greater than V_{ON-th} with VDS being negative.

After this, the MK1170-Q1 goes into regulation mode, and adjusts the VDS of SR MOSFET to be around V_{DS-reg} until the current through SR MOSFET drops to zero. The SR mode control timing diagram is shown on Figure19.

8.3.7 SR Turn-Off Phase

After the turn-on blanking time $T_{B\text{-}on}$, the turn-off threshold of VDS is set to around $V_{OFF\text{-}th}$. With a suitable VDS regulation and turn-off scheme, the MK1170-Q1 keeps SR MOSFET as much as possible to prevent it from turning off prematurely and conducting current through body diode for too long of time.

With an extremely fast turn-off propagation delay and ~4A pull-down (sink) current, the MK1170-Q1 is rapidly turned off when the current through the external SR MOSFET reaches zero.

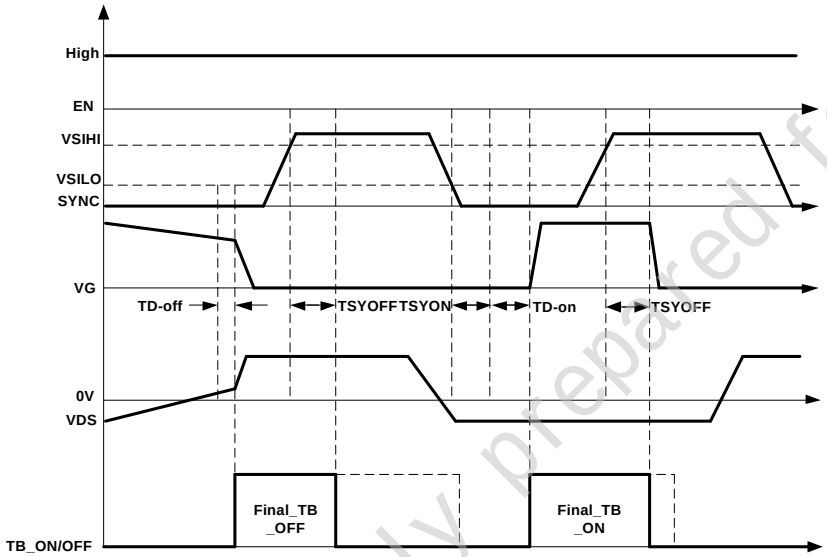


Figure 19. SR Mode Control Timing Diagram

9. Application and Implementation

9.1 Typical Applications

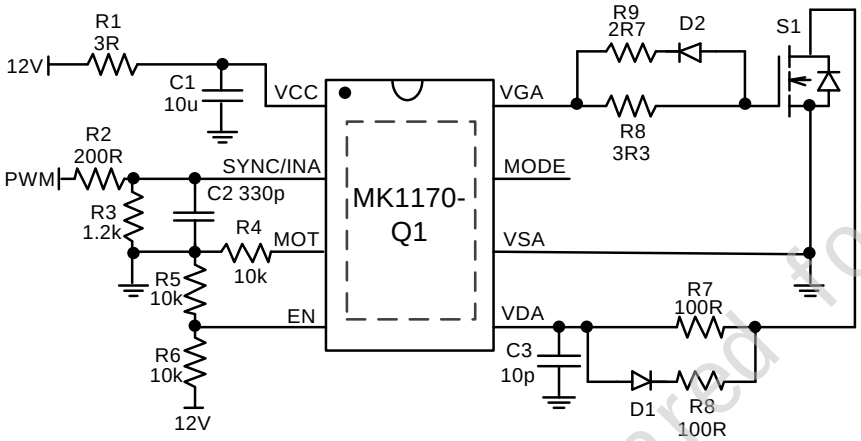


Figure 20. MK1170-Q1 Reference Design Circuit

9.2 Design Procedure

9.2.1 Supply Voltage

The supply voltage applied to the controller VCC pin should never exceed the absolute maximum ratings. Higher supply voltages require consideration of chip power dissipation and junction temperature (See Section 9.2.4). In some scenarios where the output bus voltage is high (for example, applications with outputs greater than 36V), a high voltage LDO must be used so that the VCC pin does not exceed the absolute maximum ratings and reduces the power dissipation of the internal LDO.

MK1170-Q1 reference design circuit is shown in Figure 20, connecting a low-ESR ceramic decoupling capacitor (C1) between 1μF and 10μF from VCC to VSA for stability. The choice of decoupling capacitor voltage rating should also depend on the VCC voltage. Place the capacitor (C1) as close as possible to the MK1170-Q1 VCC and VSA pins.

9.2.2 Peak Source and Sink Current

To reduce the switching losses and stress of the SR MOSFET, the switching speed of the MOSFET during turn-on and turn-off should be considered. The chip should be able to provide the required peak current for achieving the targeted switching speeds with the targeted power MOSFET. The maximum source and sink currents of the MK1170-Q1 have been provided.

For system applications, adding resistor R8 (such as 1Ω or 4.7Ω) between the gate of MOSFET and the VGA controls the switching speed of the MOSFET. Add diodes D2 as well as resistors R9. Keep the value of the resistor at 0Ω to achieve the fastest turn-off time.

9.2.3 Design of VDA Filtering Circuit

There are different circuit designs in different application systems. In SR mode, V_{ON-th} and V_{OFF-th} are important parameters, which determines the output of the gate driver. When VDS falls below V_{ON-th}, the gate driver output turns on the SR MOSFET. During regulation mode, MK1170-Q1 adjusts the VDS of SR MOSFET to be around V_{DS-reg} until the current through the SR MOSFET drops to zero. The driver will immediately shut down, when the VDS voltage exceeds V_{OFF-th}.
If really needed, the detection value of VDS may be slightly fine-tuned by adding the filtering circuit (C3, R7, R8 and D1) between the drain of the MOSFET and VDA. Among them, C3 and R7 increase the turn-off delay of SR MOSFET, and the C3, R8 and D1 add SR MOSFET turn-on delay.

9.2.4 Power Dissipation

The chip power consumption and junction temperature must be considered. The chip will be damaged, if these two parameters are too large. The total power consumption (P_{DIS}) is estimated by the following formula:

$$P_{DIS} = P_{DRV} + P_P$$

The gate power (P_{DRV}) needs to be calculated first. It is calculated based on the formula:

$$P_{DRV} = (Q_g - Q_{gd}) \times f_{smax} \times V_{CC}$$

Where (Q_g-Q_{gd}) is the total gate charge for SR MOSFET, f_{smax} is the maximum switching frequency, and V_{CC} is the supply voltage. The power consumption P_p (without gate charge) must also be included, as shown below:

$$P_P = I_{CC} \times V_{CC}$$

I_{CC} is the normal operating supply current without gate charging. The operating junction temperature (T_{JOP}) at a given ambient temperature (T_A) can be estimated according to the formula:

$$T_{JOP} = \theta_{JA} \times P_{DIS} + T_A$$

θ_{JA} is the junction-to-ambient thermal resistance.

9.2.5 MOSFET Selection

The voltage stress of SR MOSFET on LLC topology, without considering the ringing voltages, must be twice of the output voltage. However, due to the switching noises when MOSFET is turned off, there is always extra voltage stress. To ensure enough design margin, the selection of VDS voltage rating for MOSFEET is important. It is recommended to ensure a margin of at least 3 times the output voltage.
Due to the adjusting voltage threshold and driver ability of the synchronous rectifier controller, the selection of the power MOSFETs is a trade-off between RDS(ON) and Qg. Choosing the appropriate Qg value is also very important. A larger Qg will reduce the on/off speed and result in greater switching loss. Therefore, it is necessary to consider the on/off speed and switching loss. MOSFETs with smaller RDS (ON) will touch the adjusting voltage threshold at higher current, so that the power MOSFET cannot be fully turned on due to lower gate voltage. Therefore, the

conduction loss reduction barely observed, and the benefit of the lower RDS (ON) MOSFET is not obvious. It is recommended to calculate the appropriate Rdson using the following formula:

$$Rdson = \frac{Vdsreg * \Pi}{2\sqrt{2} * Ioutmax}$$

For example, the typical value Vdsreg of MK1170-Q1 is -10mV. In applications where the maximum output current Ioutmax is 20A, Rdson can be calculated:

$$Rdson = \frac{10mV * \Pi}{2\sqrt{2} * 20A} \approx 0.56m\Omega$$

the RDS(ON) of the MOSFET is recommended to be no lower than 0.56mΩ.

9.2.6 SYNC Signal Participates in SR Control

The working waveform with SYNC signal is shown in Figure 21, where the purple line represents the SYNC signal, the green line represents the MOSFET VDS signal, the yellow line represents the gate output signal. The gate output must be low when SYNC voltage is higher than V_{SIHI} threshold. Only when the SYNC voltage is below the V_{SILO} threshold, MK1170-Q1 begins to detect and determine whether the VDS voltage is below the turn-on threshold, if so, the gate output is high. When the VDS voltage is detected to be above the turn-off threshold, even if the SYNC signal is still low, the MOSFET will immediately turn off.

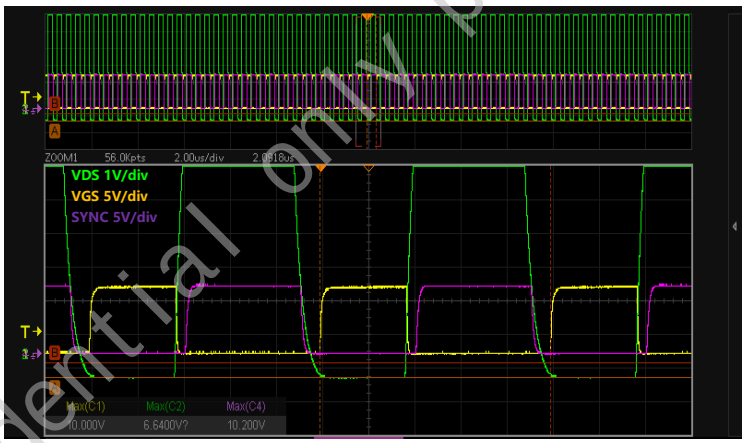


Figure 21. MK1170-Q1 Reference Working Waveform

10. Power Supply Recommendations

11. Layout

11.1 Layout Guidelines

To achieve high performance of the MK1170-Q1, the following layout tips must be followed.

1. Use separate clean traces for VCC and VSA pins.
2. At least one low-ESR ceramic bypass capacitor(100nF) must be used. Place the capacitor as close as possible to the VCC and VSA pins.
3. The VSA pin on the ground plane needs to route with a short and wide trace.
4. Use separate traces for source sense pin (VSA).
5. Keep the differential sampling inputs (VDA/VSA) to MOSFET drain/source pins as short as possible.
6. Keep the loop area of the differential sampling inputs (VDA/VSA) to MOSFET drain/source pins as small as possible.
7. Avoid placing the VDA, VSA and SYNC traces close to any other high dV/dT traces that would induce significant noise into the high impedance leads.
8. The trace from the VGA pin to the gate of the SR MOSFET needs to be as short as possible.

11.1 Layout Example

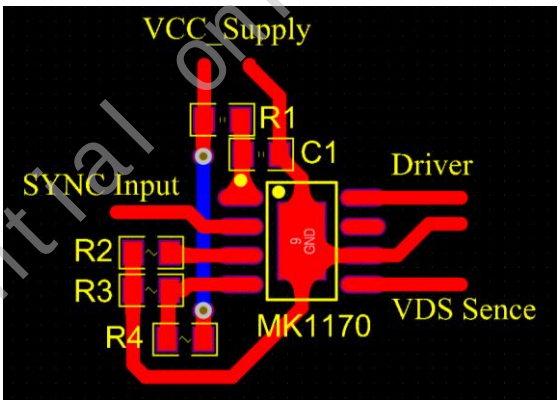


Figure 22. MK1170-Q1 Layout Example

12. Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13. Mechanical, Packaging

13.1 ESOP-8 Package Size

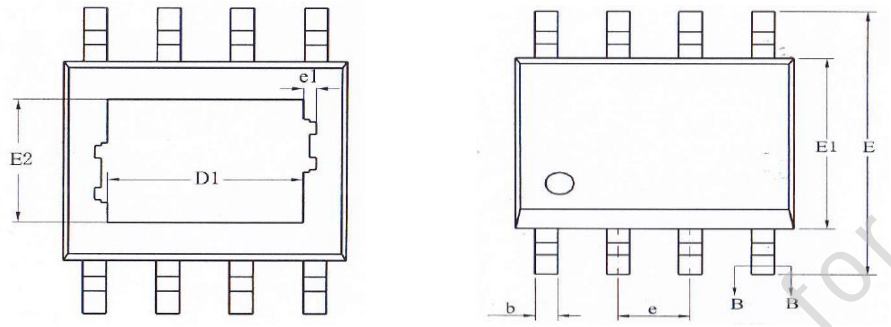


Figure 23. ESOP-8 Top View

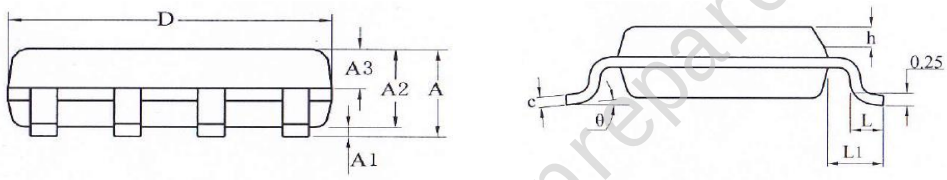


Figure 24. ESOP-8 Side View

SYMBOL	Dimensions In Millimeters	
	MIN	MAX
A	-	1.65
A1	0.05	0.15
A2	1.30	1.50
b	0.39	0.47
c	0.20	0.24
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
D1	3.1REF	
E2	2.21REF	
e	1.270(BSC)	
L	0.5	0.8
θ	0°	8°

Note:

（1）This drawing is subject to change without notice

13.2 ESOP-8 Recommended Land Pattern

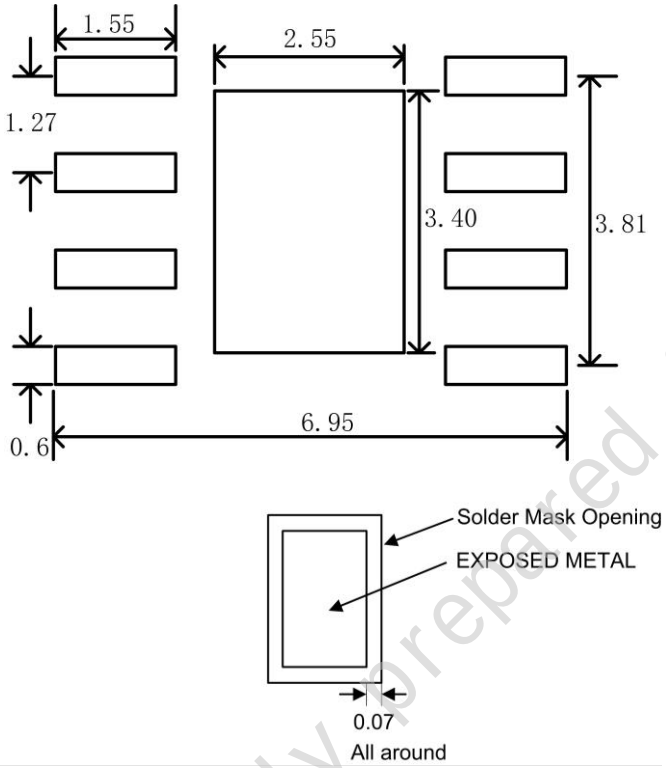


Figure 25. ESOP-8 Recommended Land Pattern

Notes: (continued)

（1） All linear dimensions are in millimeters.

（2） It is recommended that vias under paste be filled, plugged or tented.

14. Reel and Tape Information

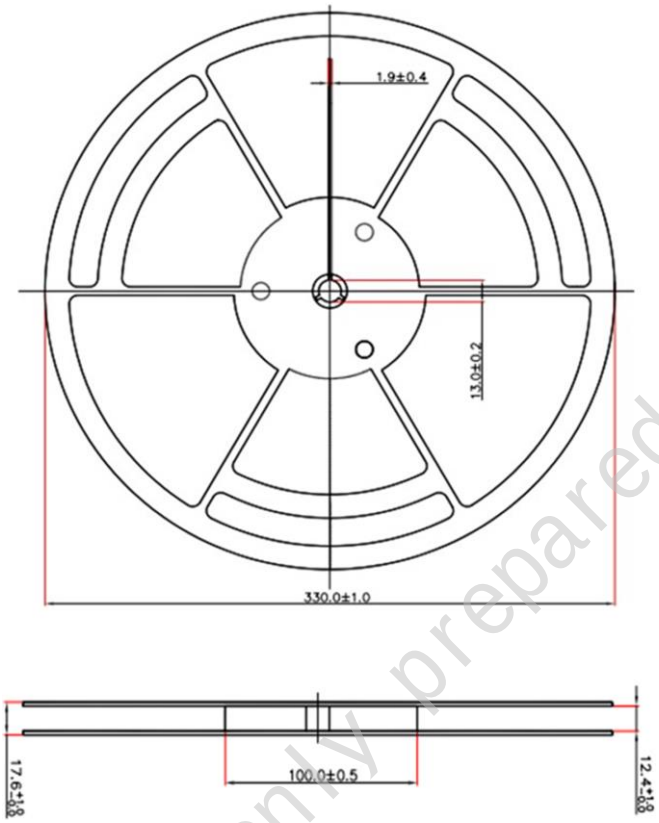
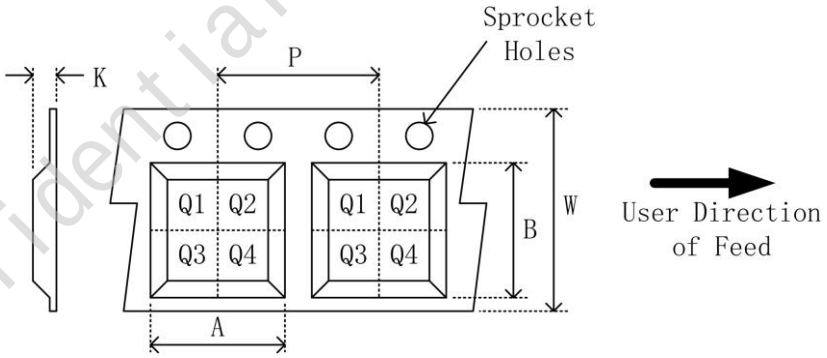


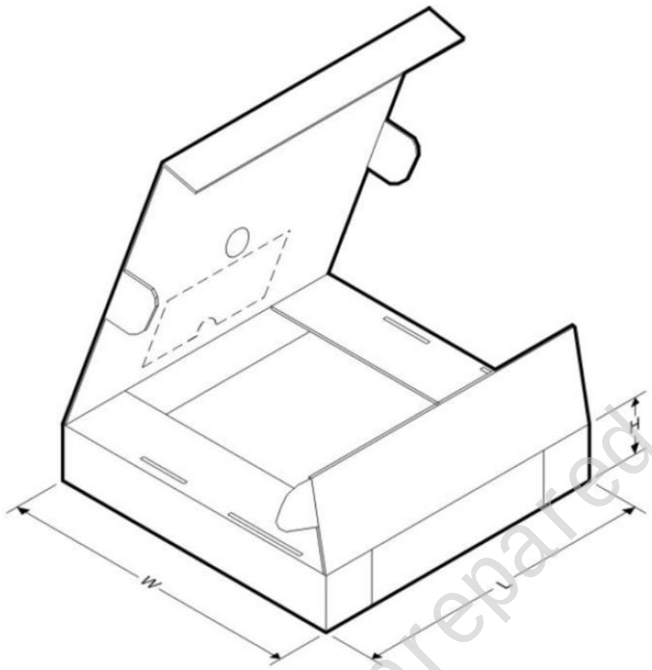
Figure 26. Reel Dimensions



Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	W (mm)	Pin1 Quadrant
MK1170XAD-Q1	ESOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8±0.1	12±0.1	Q1

Figure 27. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

15. Tape and Reel Box Dimensions



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MK1170XAD-Q1	ESOP-8	8	8000	360	360	65

Figure 28. Box Dimensions