MK2553 Critical Conduction Mode PFC GaN Controller

1. Description

The MK2553 families are critical conduction mode (CrM) power factor correction (PFC) controllers for high performance AC/DC power systems. With the highly linear multiplier and THD optimizer, the MK2553 can achieve ultra-low THD and near unity power factor under different operation conditions. The MK2553 operates over a wide supply voltage range from 11V to 30V, which is suitable for a variety of application scenarios. Ultra-low startup current and optimized VCC undervoltage protection makes startup easier for self-powered systems. In application scenarios that focus on light-load efficiency, MK2553 can choose to enter the discontinuous conduction mode (DCM). In this mode, when the switching frequency exceeds the frequency clamping threshold, the circuit operates in DCM with valley turn-on. The Intelligent protection functions and strategies of MK2553 can effectively reduce GaN electrical stress and greatly improve system reliability, such as soft-start and soft-stop protection, brown-in and brown-out protection, smart high/low line overcurrent protection, etc.

2. Applications

- AC/DC Adapters/Charger
- Industrial Power Supplies
- TV, Desktop PC, Monitor
- Lighting Application

3. Features

- Operates in a Wide VCC Voltage Range from 11V-30V
- Ultra-Low Quiescent Current: <160uA
- Ultra-Low Startup Current: <20uA
- Total Harmonic Compensator for AC Zero-Crossing
- Ultra-low THD & Unity Power Factor
- Smart High/Low Line Overcurrent Protection and Soft Start Function
- Maximum Operating Frequency Limit and Valley Switching
- Integrated E-GaN Driver
- On-Chip Current Sense Filter
- Brown-In and Brown-Out Protection (MK2553QG)
- Noise Immunity Enhancement
- Feedback Open Loop Protection
- Package: SOP-8

4. Typical Application

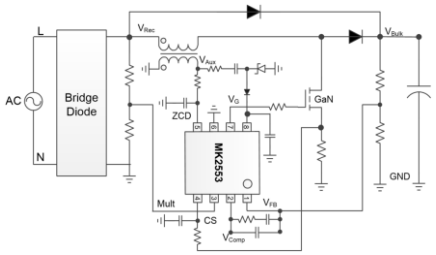


Figure 1. Typical Application Diagram

5. Order Information

Order Part Number	Descriptions
MK2553GXAB	SOP-8, tape, 4000 pcs/reel
MK2553QGXAB	SOP-8, tape, 4000 pcs/reel

6. Pin Configuration and Functions

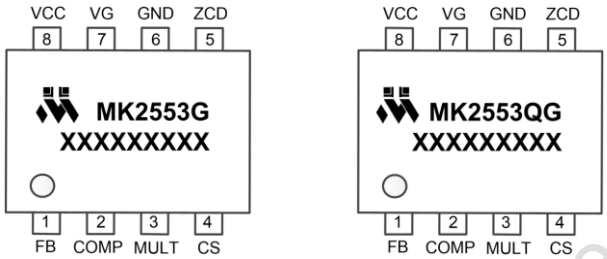


Figure 2. Pin Function (top view)

Table 1. Pin Functions

Pin		Descriptions
NO.	Name	
1	FB	Negative input of the error amplifier (E/A). The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and FB (pin#1) to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the GaN is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine GaN's turn-off.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers GaN's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	VG	Gate driver output.
8	VCC	Supply Voltage of both the signal part of the IC and the gate driver.

7. Specifications

7.1 Absolute Maximum Ratings (1)

Symbol	Parameter	MIN	MAX	Units
VCC	supply voltage VCC	-0.3	32	V
FB, COMP, MULT, CS (2)	voltage on pin FB, COMP, MULT, CS	-0.3	8	
VG (2)	voltage on pin VG	-0.3	8	
T_J	operating junction temperature,	-40	150	°C
T_{stg}	storage temperature	-55	150	
T_{sld}	soldering temperature (10 second)		260	

Notes:

(1) Stresses beyond the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in "RECOMMENED OPERATING CONDITIONS". Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Output pin not to be voltage driven.

7.2 ESD Ratings

		Value	Unit
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±2000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	Units
Recommended Operation Conditions	VCC supply voltage	12	28	V
	ZCD max current	-0.8	0.8	mA
	operating junction temperature. (T_J)	-40	125	°C

7.4 Thermal Information

		Value	Units
Package Thermal Resistance (1)	θ_{JA} (Junction to ambient)	128	°C/W
	θ_{JC} (Junction to case)	75	

Note:

(1) Measured on JESD51-7, 4-layer PCB.

7.5 Electrical Characteristics

-40°C ≤ T_A = T_J ≤ 125°C. V_{CC} = 13V_{DC}, 1μF from VCC to GND. All voltages are measured with respect to ground (pin 6). Currents are positive when flowing into the IC, unless otherwise specified.

Parameter		Test Conditions	Min	Typ	Max	Unit
Supply Current						
I_{st}	Start-up current	Before turn-on, V_{CC}=11V		20	35	μA
I_q	Quiescent current	V_{CC}=13V, V_{FB}=3V		160	230	μA
I_{op}	Operating supply current	T_J=+25°C; F_{sw}=70kHz, C_{load}=1nF at VG		1.3	1.8	mA
		F_{sw}=70kHz, C_{load}=1nF at VG		2.0	3.6	
Supply Voltage						
V_{CC}	Operating range	After turn-on	11		30	V
V_{CC_ON}	Turn-on threshold		11	12	13	V
V_{CC_OFF}	Turn-off threshold		8.7	9.5	10.5	V
V_{CC_Hys}	Threshold hysteresis	T_J=+25°C	2.1		2.6	V
		T_J=-40~+125°C	1.7		3.2	
V_Z	VCC holding threshold	I_{CC}=20mA	30	32	35	V
Multiplier Input						
I_{mult}	Input bias current (1)	V_{mult}=2V			1	μA
V_{mult}	Linear operating range (1)		0 to 3			V
ΔV_{CS} /ΔV_{mult}	Output max slope (1)	V_{COMP}=upper clamp, V_{mult}=0V to 0.9V		1.3		V/V
K	Multiplier output gain	V_{mult}=1V, V_{COMP}=4V; T_J=+25°C	0.50	0.60	0.77	1/V
		V_{mult}=2.2V, V_{COMP}=3V; T_J=+25°C	0.13	0.23	0.33	1/V
Error Amplifier						
V_{FB}	Feedback voltage threshold	T_J=+25°C	2.455	2.510	2.575	V
		T_J=-40~+125°C	2.42	2.51	2.59	
I_{FB}	Input bias current (1)	V_{FB}=2.5V			1	μA
I_{COMP}	Source current (1)	V_{COMP}=4V, V_{FB} =2.4V		3.6		mA
	Sink current (1)	V_{COMP}=4V, V_{FB} =2.6V		5.7		mA

V_{COMP}	Upper clamp voltage	I_{source}=0.5mA, V_{CC}=13V, T_J=+25°C	5.4	5.9	6.5	V
	Lower clamp voltage	I_{sink}=0.1mA, V_{CC}=13V, T_J=+25°C	2.00	2.15	2.30	V
V_{FB_dis}	FB Disable threshold		260	300	340	mV
V_{FB_en}	FB Enable threshold		360	400	440	mV
Brown-In Brown-Out Protection and Line Feed Forward (MK2553QG)						
V_{BI}	Brown-in Threshold		0.8	0.9	1.0	V
V_{BO}	Brown-out Threshold		0.7	0.8	0.9	V
V_{HL}	Comparator threshold for high line detection		1.9	2.0	2.1	V
V_{LL}	Comparator threshold for low line detection		1.6	1.7	1.8	V
Output Overvoltage						
I_{OVP}	Dynamic OVP triggering current	T_J=+25°C	23.5	27.0	30.5	µA
I_{OVP_Hys}	Dynamic OVP current hysteresis (1)			10		µA
V_{OVP}	Static OVP threshold		2.00	2.15	2.30	V
Current Sense Comparator						
I_{CS}	Input bias current (1)	V_{CS}=1V			1	µA
T_{dly}	Delay to output (1)			100		ns
V_{CS_offset}	Current sense offset (1)	V_{mult}=0V		30		mV
		V_{mult}=3V		0		
V_{CS_OC}	OC threshold	V_{COMP}=upper clamp	1.0	1.1	1.2	V
$V_{CS\_OC\_LL}$	OC threshold when low line is detected	V_{COMP}=upper clamp	1.0	1.1	1.2	V
$V_{CS\_OC\_HL}$	OC threshold when low line is detected	V_{COMP}=upper clamp	0.6	0.7	0.8	V
Zero Current Detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD}=0.5mA, T_J=+25°C	5.5	5.7	6.6	V

V_{ZCDL}	Lower clamp voltage	I_{ZCD}=-0.5mA, T_J=+25°C	0.50	0.65	0.80	V
V_{ZCDA}	Arming voltage		1.3	1.4	1.5	V
V_{ZCDT}	Triggering voltage		0.6	0.7	0.8	V
I_{ZCD}	Input bias current (1)	V_{ZCD}=3V			1	μA
I_{ZCD_src}	Source current (1)	V_{CC}=13V, V_{ZCD}=0.3V		4.5		mA
I_{ZCD_snk}	Sink current (1)	V_{CC}=13V, V_{ZCD}=6.3V		1		mA
V_{ZCD_dis}	ZCD Disable threshold		260	300	340	mV
V_{ZCD_en}	ZCD Enable threshold		360	400	440	mV
Gate Driver						
V_L	Gate low level (1)	I_{gate}=200mA		0.1	0.5	V
V_H	Gate high level	I_{gate}=200mA	5	5.4	6	V
V_{clamp}	Gate clamp voltage	V_{CC}=28V	5	5.5	6	V
T_r	Gate rising time (1) (20%~80%)	C_{load}=1nF,		40		ns
T_f	Gate falling time (1) (80%~20%)	C_{load}=1nF		30		ns
Starter						
T_{start}	Start timer period		100	190	230	μs
T_{ss}	Soft start time		5	10	15	ms
Maximum Operating Frequency Limit						
F_{sw_max}	Maximum switching frequency (1)			135		kHz

Note:

(1) Values are guaranteed by design and verified by characterization on bench, not tested in production.

7.6 Typical Characteristics

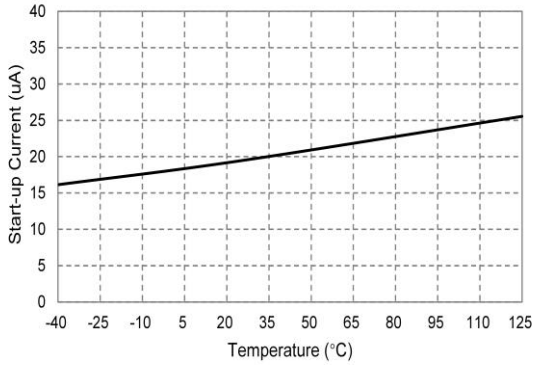


Figure 3 Start-up Current vs Temperature

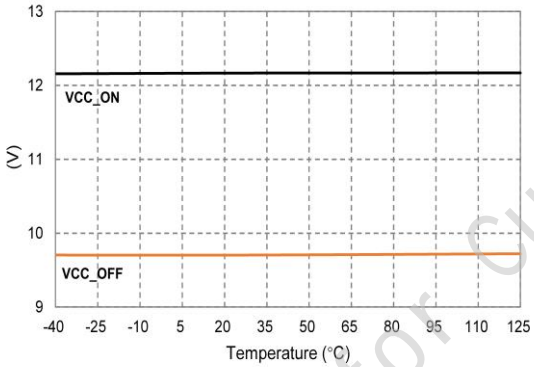


Figure 4 Start-up & UVLO vs Temperature

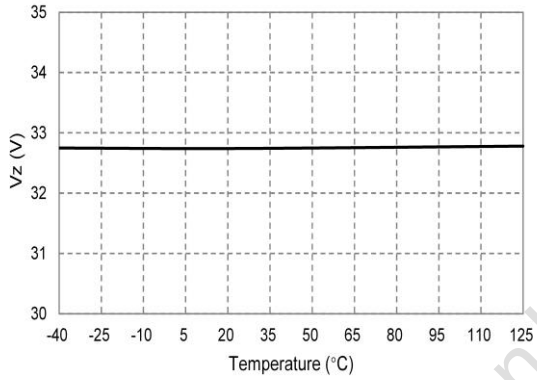


Figure 5 VCC Zener Voltage vs Temperature

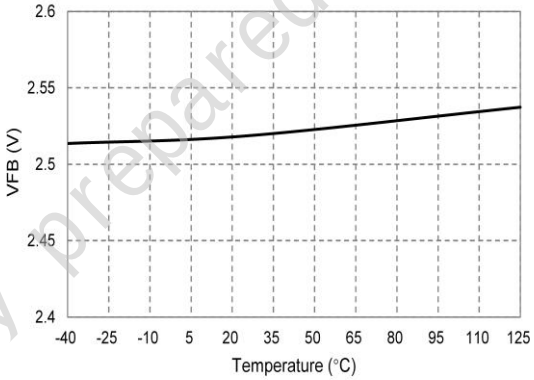


Figure 6 Feedback Reference vs Temperature

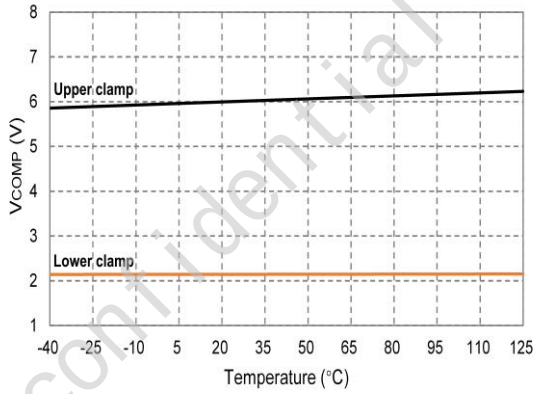


Figure 7 E/A Output Clamp Levels vsTemperature

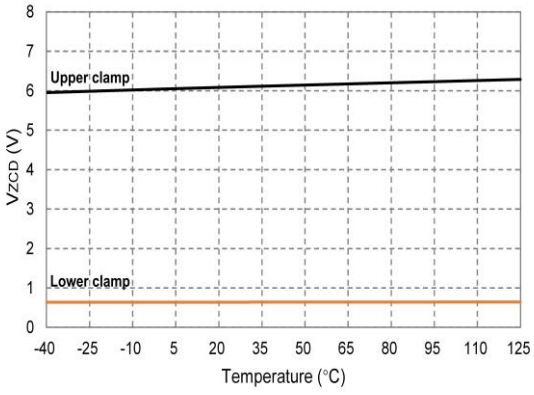


Figure 8 ZCD Clamp Levels vs Temperature

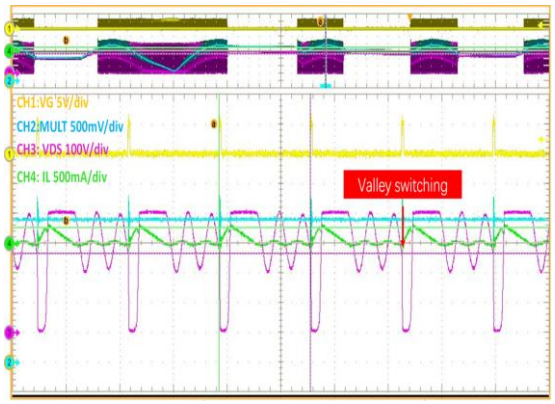


Figure 9 Frequency Limit and Valley Switching Test

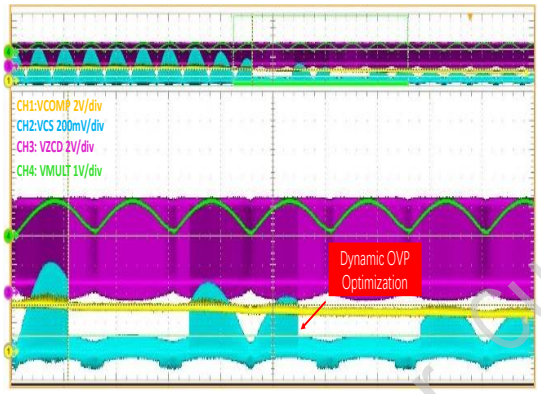


Figure 10 Dynamic OVP Test

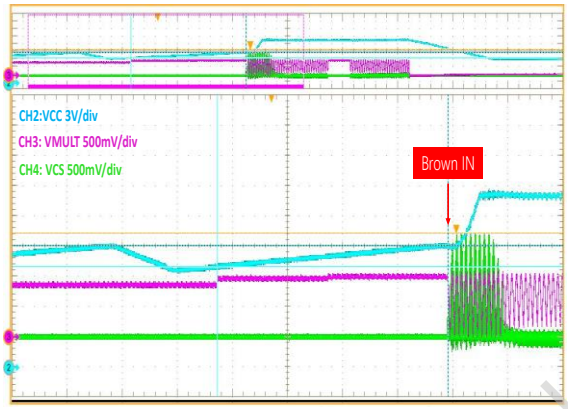


Figure 11 Brown-In and Brown-Out Test

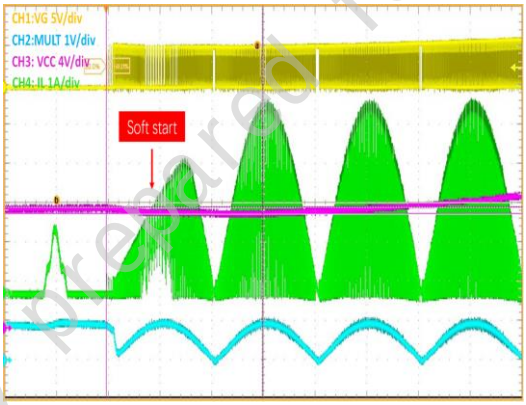


Figure 12 System Soft Startup Test

8. Detailed Description

8.1 Overview

The MK2553 families are critical conduction mode (CrM) power factor correction (PFC) controllers for high performance AC/DC power systems，which achieve ultra-low THD and near unity power factor under different operation conditions. It features an operational amplifier for feedback error processing, a highly linear multiplier for low THD, a current-sense comparator, a current zero-crossing detector, PWM logic, and a driver for external GaN FET, etc.

The system performance is enhanced by increasing the operating voltage range and optimizing the startup strategy, which makes the controller easier to start in the self-powered system. The device also features an innovative dynamic overvoltage protection enhancement circuit, which improves the performance of the system under dynamic load. The soft start function and optimized operating currents of the device result in low current stress and low power consumption. The Intelligent protection functions and strategies of MK2553 can greatly improve system reliability, such as feedback open loop protection, soft stop protection, brown in/brown out protection, and smart high/low line overcurrent protection.

MK2553 includes a range of features designed to make the PFC converter operation well controlled and protected. It can be flexibly configured according to requirements. MK2553 includes frequency limit and valley switching functions. In application scenarios that focus on light-load efficiency, MK2553 enters the discontinuous conduction mode (DCM). In this mode, when the switching frequency exceeds the frequency clamping threshold, the circuit operates in DCM with valley turn-on. MK2553QG, and MK2553G can be selected according to usage requirements. Table 2 compares the two devices, those parameters that may result in different values of the external components.

Table 2 MK2553QG and MK2553G

Parameter	MK2553QG	MK2553G
H/L line overcurrent protection	Yes	Yes
FB disable function	Yes	Yes
Soft start function	Yes	Yes
Brownout protection and soft stop function	Yes	No
Frequency limit and valley switching	Yes	Yes
Integrated E-GaN Driver	Yes	Yes
Multiplier gain (typ.)	0.42	
Current sense reference clamp (typ.)	1.1 V	
Dynamic OVP triggering current (typ.)	27 uA	
ZCD arm/trigger thresholds (typ.)	1.4/0.7 V	

8.2 Functional Block Diagram

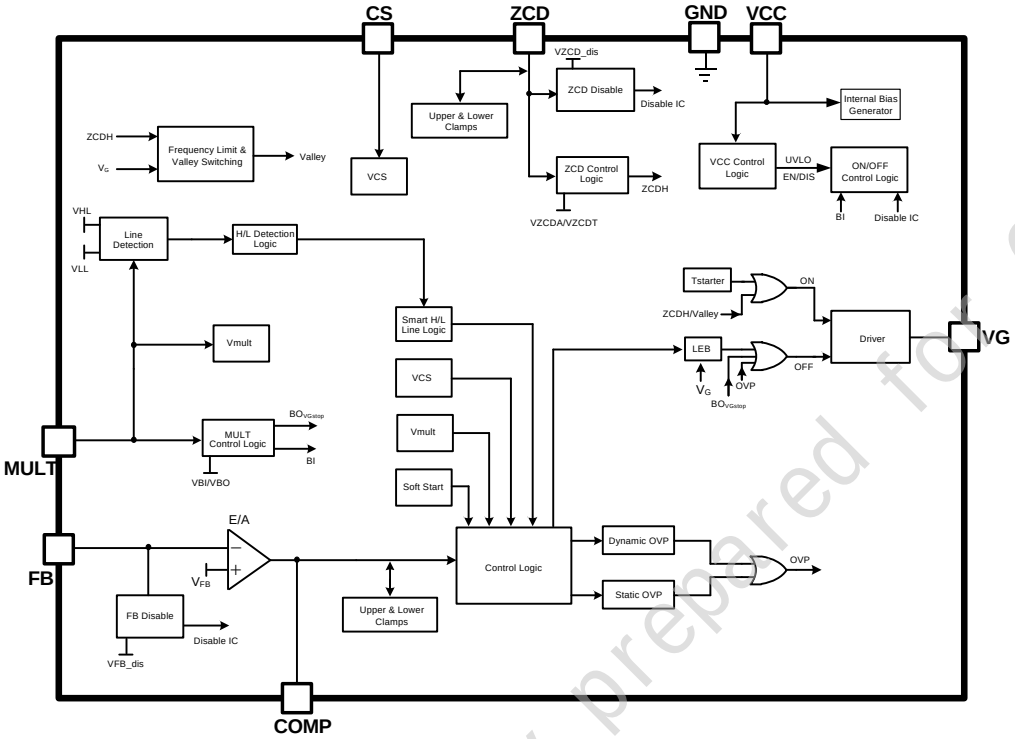


Figure 13 Block Diagram

8.3 Feature Description

8.3.1 VCC Power Supply and Undervoltage Lockout

The MK2553 operates from a supply voltage of 11V to 30V. This feature makes MK2553 suitable for a variety of application scenarios. For the best performance, use a typical 0.1uF decoupling capacitor as close as possible between the VCC and GND pins of MK2553. A VCC bypass capacitor (1uF to 10uF) in parallel to the decoupling capacitor is also recommended to reduce noise ripple during switching.

MK2553 has an internal undervoltage lockout (UVLO) protection feature in the VCC supply circuit blocks. When the voltage on the VCC pin exceeds $V_{CC\text{-}ON}$, the controller leaves the UVLO state and activates the circuitry. When VCC voltage drops to below $V_{CC\text{-}OFF}$, the controller re-enters the UVLO state.

8.3.2 Disable Function

When FB pin voltage is below V_{FB_dis}, the MK2553 is shut down and reduces its power consumption to a lower value. To restart the IC, the FB pin voltage must exceed V_{FB_en}. Using this function, the user can flexibly control the operating state of the MK2553.

Moreover, the FB pin also provides a certain degree of additional security. When the lower resistor of the output voltage divider is shorted to ground or the upper resistor is missing, the MK2553 will be in the off-protection state. The MK2553 ZCD pin also has similar functions.

8.3.3 Soft Start Function

During startup, when the output capacitor voltage has not yet been established, and the converter is started with or without load, it will bring greater current stress to the GaN, reducing the reliability of the system. The MK2553 adds a soft start feature to prevent this. In the start-up stage (T_{SS}), the soft start function is achieved by linearly raising the overcurrent protection threshold, so that the conduction current on the GaN rises steadily.

8.3.4 Overvoltage Function

When the output voltage is higher than the set overvoltage protection point， the difference current will flow through the compensation network and enter the error amplifier output (pin COMP). This current is monitored inside the device. As the current exceeds I_{OVP}, the OVP is triggered (Dynamic OVP).

when the load of a PFC converter is very low, the output voltage tends to stay steadily above the nominal value, which cannot be handled by the Dynamic OVP. If this occurs, the error amplifier output will saturate low. When this is detected, the external power transistor is switched off and the MK2553 put in an idle state (Static OVP).

When the system performs a load jump, the MK2553 also adds dynamic overvoltage protection enhancement optimization, which can make the drive waveform as continuous as possible. This improves system noise and ripple. The control diagram is shown on Figure14.

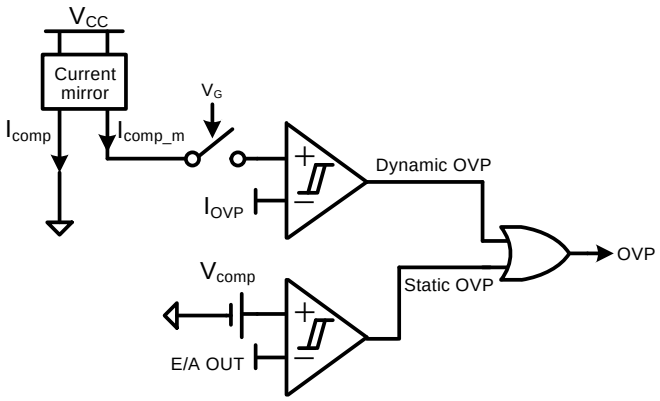


Figure 14 Overvoltage Function Logic Control Diagram

8.3.5 Overcurrent Protection

Under certain conditions (such as inrush, brownout-recovery, and output over-load) the PFC power stage sees large currents. It is critical that the power devices be protected from switching during these conditions.

A shunt resistor in series with GaN source leg is used to sense the peak currents. When the GaN is turned on, the conduction current flows through the detection resistor. If the voltage at the resistor is higher than V_{CS_OC}, the GaN is turned off, and the MK2553 enters overcurrent protection. The reference voltage for overcurrent detection in traditional controllers is always a fixed value. However, when the system input voltage changes and the detection resistance is fixed, this can lead to changes in the actual overcurrent protection value. Consequently, under high input voltage, GaN may be damaged due to overcurrent before the overcurrent protection point is even touched. MK2553 has improved the above issues by designing a two-level overcurrent protection threshold based on the input voltage. When the voltage of the MULT pin is lower than V_{LL}, MK2553 determines that it is low line, and the overcurrent protection threshold is $V_{CS\_OC\_LL}$. When the voltage of the MULT pin is higher than V_{HL}, it is judged as high line and the overcurrent protection threshold is reduced to $V_{CS\_OC\_HL}$. In this way, the MK2553 can effectively solve the differences of high low line overcurrent values under wide input voltage conditions. The control diagram is shown on Figure15.

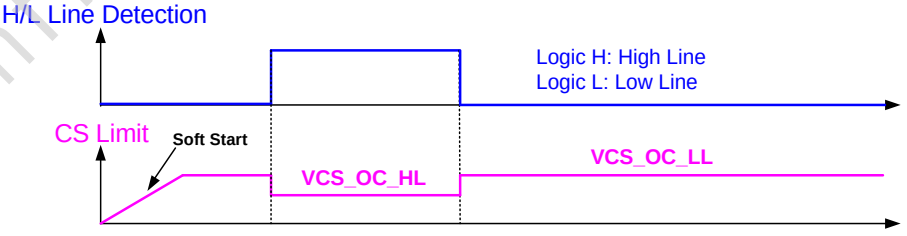


Figure 15 High/Low Line Overcurrent Protection Control Diagram

8.3.6 Brownout Protection and Soft Stop Function

As the power line voltage decreases, input current must increase to maintain a constant output voltage for a specific load. Brownout protection helps prevent excess system thermal stress (due to the higher RMS input current) from exceeding a safe operating level.

Power-line voltage is sensed at MULT pin. When the MULT pin voltage fails to exceed the brownout threshold (V_{BO}), a brownout condition is detected, and gate drive output does not immediately turn off until the input voltage approaches the valley. The addition of the soft stop function ensures a smooth shutdown and does not lead to incorrect startup due to oscillations.

During brownout, COMP is actively pulled low, soft-start condition is initiated, and the VCC pin continues to sink about 1mA of current until the VCC voltage drops to UVLO. When the MULT pin voltage rises above the brown-in threshold (V_{BI}) and VCC pin exceeds V_{CC-ON}, the power stage soft starts as COMP rises with controlled voltage. The control diagram is shown on Figure16.

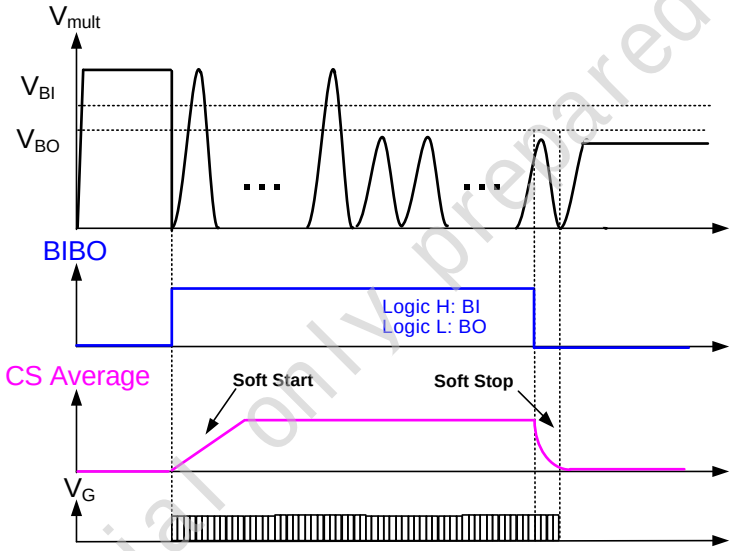


Figure 16 Brownout Protection and Soft Stop Function Control Diagram

8.3.7 Maximum Operating Frequency Limit and Valley Switching

In application scenarios focusing on light-load efficiency, the high switching frequency of CrM increases system switching losses. This loss is difficult to ignore because the system itself is at an extremely light load stage. Normally controllers only have a frequency limiting function to reduce switching loss. Although the switching frequency is reduced, the VDS voltage remains high at the moment of the GaN turned on, which increases switching loss and reduces system efficiency. The MK2553 can optionally add frequency limiting and valley switching functions to reduce switching loss at light load.

Due to the addition of the frequency limiting function, the converter will enter the discontinuous conduction mode (DCM). In this mode, when the switching frequency exceeds the frequency clamping threshold, the circuit operates in DCM with valley turn-on. The control diagram is shown on Figure17. As shown in the figure, the system has entered DCM due to a minimum cycle time ($1/F_{sw\_max}$). The driver will turn on the GaN, if the minimum cycle time is exceeded and the VDS is detected to be in a valley.

The addition of this function can significantly improve the efficiency of the system under high voltage and light load, but on the contrary, PF and THD will be affected to a certain extent.

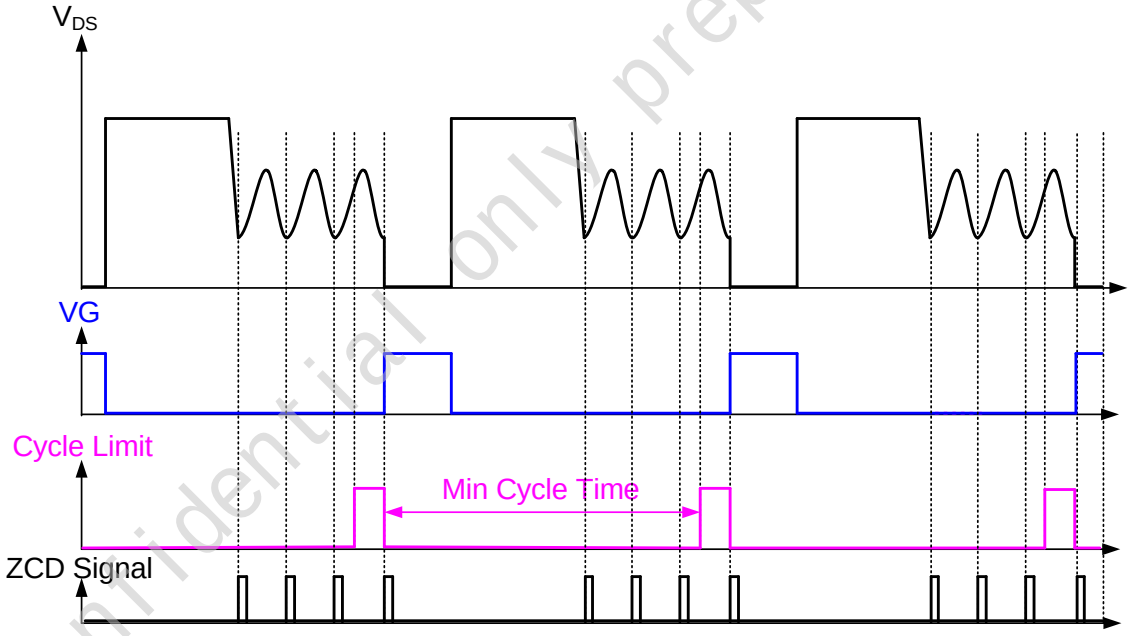


Figure 17 Frequency Limit and Valley Switching Logic Control Diagram

9. Application and Implementation

9.1 Typical Applications

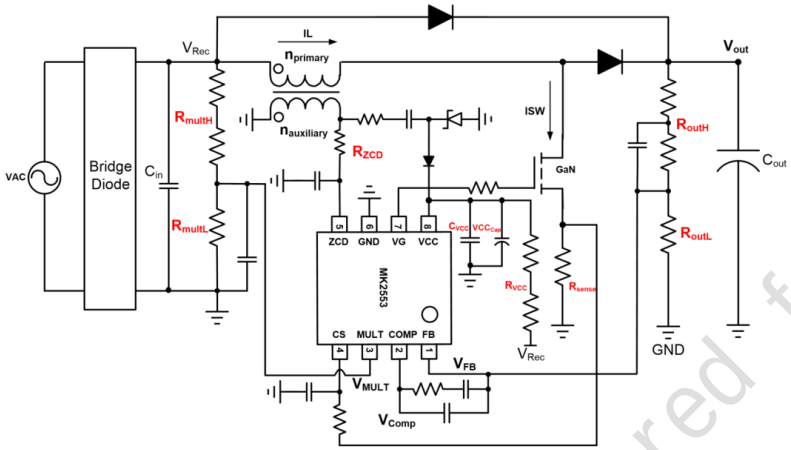


Figure 18 MK2553 Reference Design Circuit

9.2 Design Procedure

9.2.1 Supply Voltage

The supply voltage applied to the controller VCC pin should never exceed the absolute maximum ratings. Higher supply voltages require the consideration of chip power dissipation and junction temperature. In some scenarios where the supply voltage is high (for example, supply voltage greater than 30V), a high voltage LDO must be used so that the VCC pin does not exceed the absolute maximum ratings and reduce the power dissipation of the internal LDO.

MK2553 reference design circuit is shown in Figure 18. At startup, the MK2553 is powered by the VCC capacitor (VCC_{cap}) that is charged via the resistors R_{VCC}. Connect a low-ESR ceramic decoupling capacitor (C_{VCC}) in a range of 100 nF to 1 μF between VCC and GND for stability. The choice of capacitor voltage rating should also depend on the VCC voltage. Place the decoupling capacitor (C_{VCC}) as close as possible to the MK2553 VCC and GND pins.

9.2.2 Zero Current Detector

The ZCD pin is the input for demagnetization of the boost inductor. In transition mode PFC, the ZCD pin is connected to the auxiliary winding of the boost inductor through a limiting resistor. Before triggering the ZCD circuit, the voltage on the ZCD pin must experience a rising edge exceeding V_{ZCDA} (due to the GaN's turn-off). When the voltage on the pin falls below V_{ZCDT}, it sets the PWM latch and the GaN is turned on. Therefore, the maximum main-to-auxiliary winding turn ratio, n_{max}, has to ensure that the voltage delivered to the pin during the GaN's OFF-time is sufficient enough to arm the ZCD circuit. A safe margin of 15% is added.

$$n_{max} = \frac{n_{primary}}{n_{auxiliary}} = \frac{V_{out} - \sqrt{2} * VAC_{max}}{1.15 * V_{ZCDA}}$$

The minimum value of the limiting resistor can be found considering the maximum voltage across the auxiliary winding and assumes a 0.8 mA current through the pin. During the GaN ON and OFF stages, two resistance values can be calculated.

$$R_1 = \frac{\frac{V_{out}}{n_{aux}} - V_{ZCDH}}{0.8mA}$$

$$R_2 = \frac{\frac{\sqrt{2} * VAC_{max}}{n_{aux}} - V_{ZCDL}}{0.8mA}$$

Out of the two values, the higher value between the two is limiting resistor.

$$R_{ZCD} = \mathrm{Max}(R_1, R_2)$$

9.2.3 Overcurrent Protection

The CS pin is the inverting input of the current sense comparator. Through this pin, the MK2553 senses the instantaneous inductor current, which is converted to a proportional voltage by an external sense resistor (R_{sense}). As this signal crosses the overcurrent threshold, the PWM latch is reset and the power GaN is turned off. The GaN stays in OFF-state until the PWM latch is reset by the ZCD signal.

The sense resistor value (R_{sense}) can be calculated as follows.

$$R_{sense} < \frac{V_{CS\_OC\_min}}{IL_{pk}}$$

where, IL_{pk} is the maximum peak current in the inductor. $V_{CS\_OC\_min}$ is the minimum voltage allowed on the MK2553 current sense. Based on the RMS switch current ISW_{rms}, the power dissipated in R_{sense} is then given by:

$$P_{sense} = {ISW_{rms}}^2 * R_{Sense}$$

9.2.4 Multiplier and Brownout Protection (MK2553G no use)

The internal multiplier has two inputs, one from the instantaneous line voltage after rectification (MULT pin) and the other from the output of the error amplifier (COMP pin). The multiplier output is then fed into the PWM comparator and compared with the current sensing voltage VCS, to turn off the power GaN. The MK2553, by using a multiplier, can directly follow the input current with the input voltage to achieve good power factor. The multiplier output can be described by the relationship:

$$V_{mult\_out} = K * (V_{COMP} - 2.5V) * V_{MULT}$$

where, the K is the multiplier gain, V_{COMP} is the voltage on COMP pin, and V_{MULT} is the voltage on MULT pin.

The linear operation of the multiplier is guaranteed within the range 0V to 3 V of V_{MULT}, and according to 8.3.6, the functional characteristics of brownout protection is described. If using the MK2553QG with brownout protection, the V_{MULT} voltage at startup needs to be calculated first.

$$\frac{R_{multL} * \sqrt{2} * VAC_{min}}{R_{multL}+R_{multH}} > V_{BI}$$

A 200 μA current is assumed to flow into the multiplier divider, a resistor R_{multH} or series of resistors with suitable voltage rating is needed, as shown below.

$$R_{multH} = \frac{\sqrt{2} * VAC_{max}}{200\ \mu A}$$

9.2.5 Output Overvoltage Protection

According to 8.3.4, the functional characteristics of output overvoltage protection is described. The voltage at FB pin is kept at V_{FB} by the local feedback of the error amplifier. The network connected between FB and COMP introduces a time constant to achieve high PF. If there is any abrupt change of output voltage, the MK2553 monitors the current flowing into the error amplifier output pin. When the detected current is higher than I_{OVP}, the dynamic OVP is triggered, the MK2553 will be disabled, and the driver signal will be stopped. Therefore, the R_{outH} and R_{outL} are then selected as follows:

$$R_{outH} = \frac{\Delta V_{OVP}}{I_{OVP}}$$

where, the ΔV_{OVP} is the difference between the maximum allowable overvoltage and the output voltage.

$$R_{outL} = \frac{V_{FB} * R_{outH}}{V_{out} - V_{FB}}$$

Please note that a resistor R_{outH} with a suitable voltage rating is needed, or more resistors in series must be used.

10. Layout

10.1 Layout Guidelines

To achieve high performance of the MK2553, the following layout tips must be followed.

1. Use separate clean traces for VCC and GND pins.
2. At least one low-ESR ceramic bypass capacitor(100nF) must be used. Place the capacitor as close as possible to the MK2553 VCC and GND pins.
3. The GND pin on the ground plane needs to route with a short and wide trace. It is necessary to note that the power GND and signal GND should be routed separately, and a single point of ground should be maintained.
4. In order to minimize interference caused by capacitive coupling of the boost inductor, the device should maintain a distance from the boost inductor. It is also recommended that the device not be placed underneath magnetic elements.
5. Because of the precise zero current detection requirement, the ZCD resistor should be placed as close as possible to the ZCD pin.
6. Keep the loop area between the CS sampling resistor and the CS pin as small as possible.
7. Avoid placing the FB, COMP and MULT traces close to any other high dV/dT traces that would induce significant noise into the high impedance leads.
8. The trace from the VGA pin to the gate of the GaN needs to be as short as possible.

10.2 Layout Example

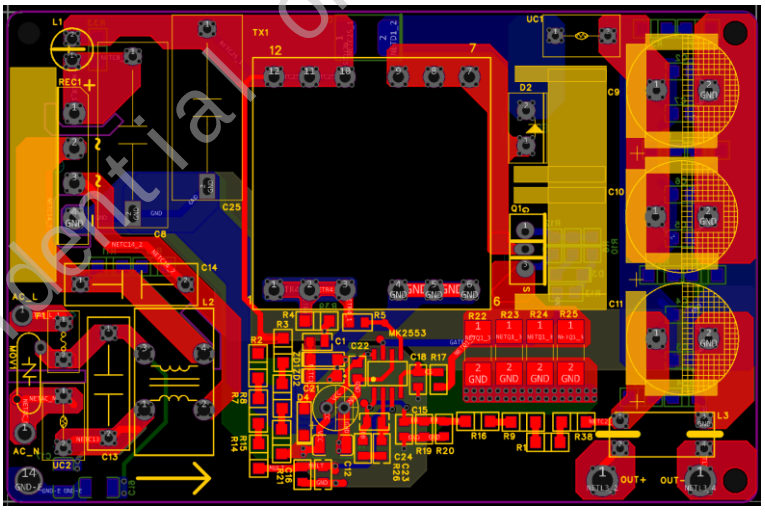


Figure 19 MK2553 Layout Example (Top Layer)

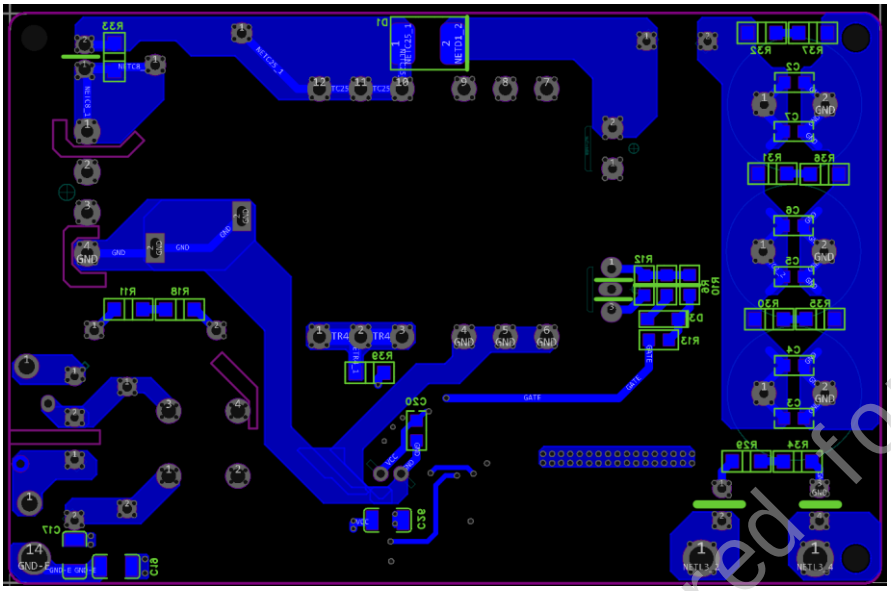


Figure 20 MK2553 Layout Example (Bottom Layer)

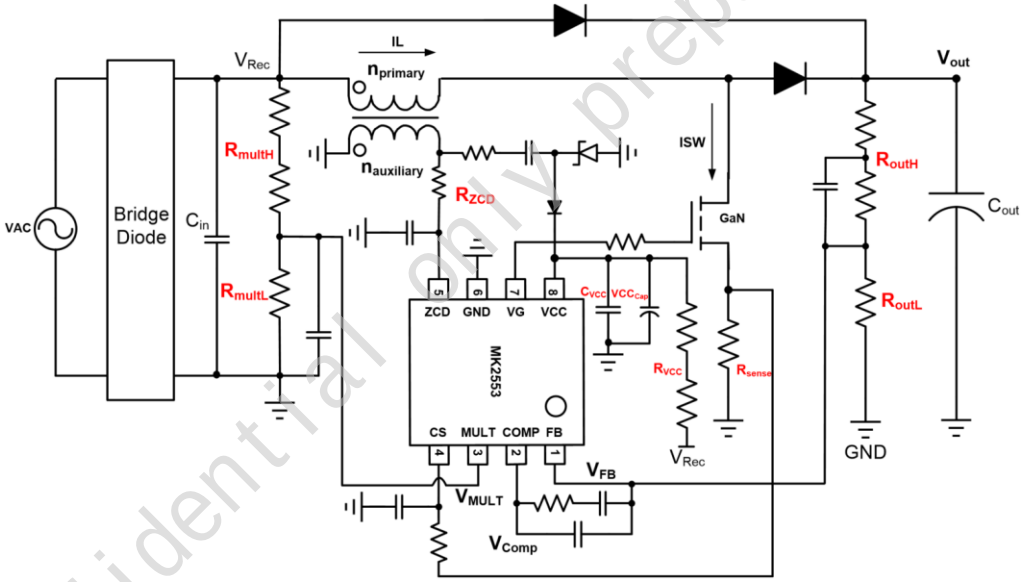


Figure 21 MK2553 Typical Schematic

11. Device and Documentation Support

11.1 Device Support

11.2 Documentation Support

11.3 Receiving Notification of Documentation Updates

11.4 Support Resources

11.5 Trademarks

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12. Mechanical, Packaging

12.1 Package Size

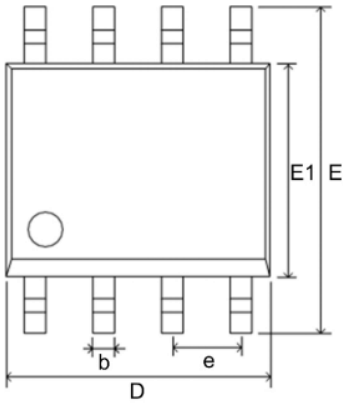


Figure 22 SOP-8 Top View

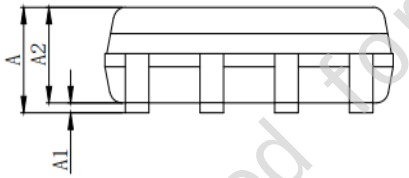


Figure 23 SOP-8 Side View

Figure 24 SOP-8 Side View

SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.30	1.55	1.75
A1	0.05	-	0.25
A2	1.25	1.40	1.65
b	0.33	-	0.51
c	0.20	-	0.25
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27(BSC)		
L	0.40	-	1.27
θ	0°	-	8°

Note:

This drawing is subject to change without notice

12.2 Recommended Land Pattern

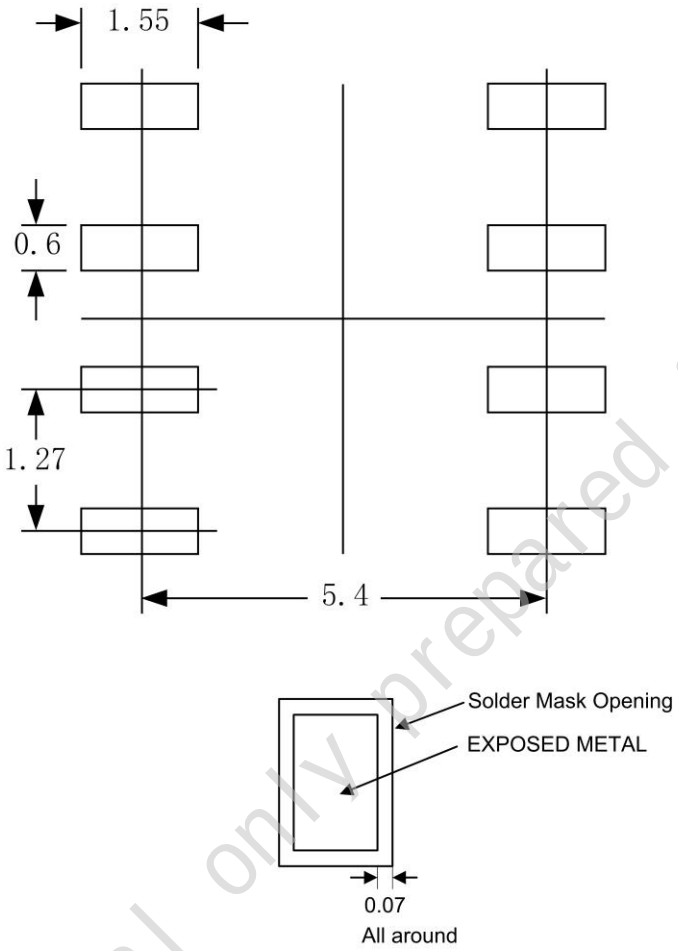


Figure 25 Recommended Land Pattern

Notes: (continued)

1. **All linear dimensions are in millimeters.**
2. **It is recommended that vias under paste be filled, plugged or tented.**

13. Reel and Tape Information

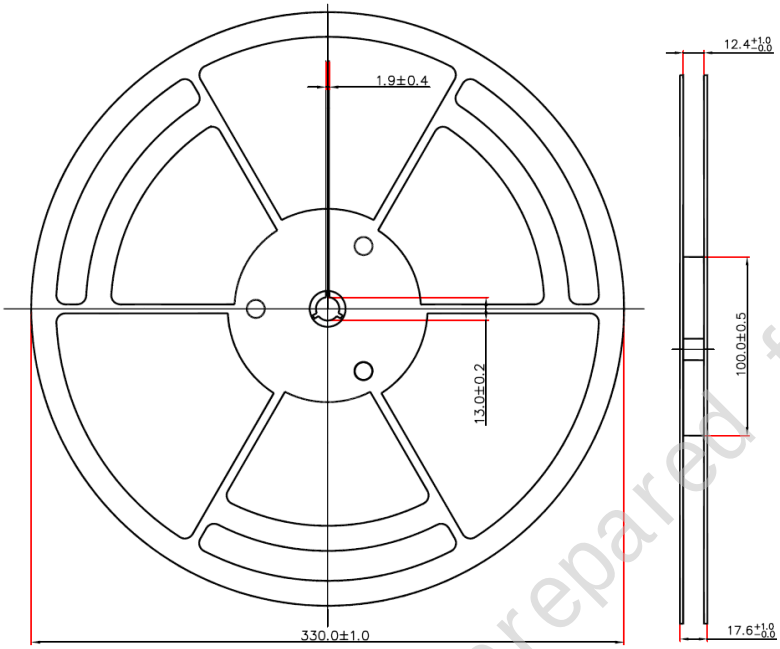
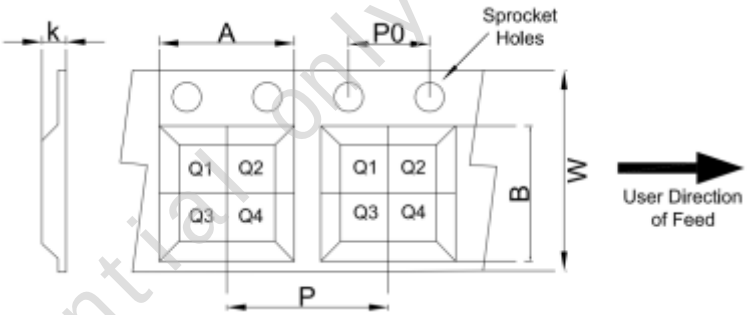


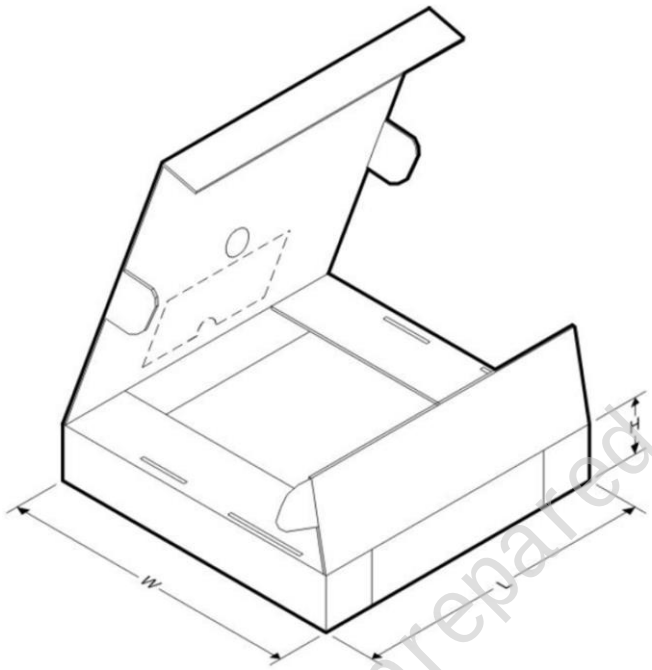
Figure 26 Reel Dimensions



Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	k (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
MK2553GXAB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	12±0.1	Q1
MK2553QGXAB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	12±0.1	Q1

Figure 27 Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

14. Tape and Reel Box Dimensions



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MK2553GXAB	SOP-8	8	8000	360	360	65
MK2553QGXAB	SOP-8	8	8000	360	360	65

Figure 28 Box Dimensions