110V, 600mA, Synchronous Buck / Iso-Buck Converter

1 Descriptions

The MK9816 is a synchronous stepdown (Buck) converter operating over a wide input voltage range from 7V to 100V. With the main MOSFET and synchronous MOSFET integrated, the MK9816 delivers up to 600mA output current.

The MK9816 adopts a constant on-time (COT) control architecture to achieve excellent transient response and to enable very high step-down ratios without external loop compensation components.

With an adaptive COT architecture, the on-time varies inversely proportional to the input voltage and proportional to the output voltage resulting in nearly constant frequency over the input and output voltage range.

The MK9816 supports Forced Continuous Conduction Mode (FCCM) and intelligent Pulse Frequency Modulation Mode (PFM) modulation techniques. FCCM operation eliminates switching frequency variation to minimize EMI and achieve optimum load transient response performance across the whole operating load range. PFM operation lowers current consumption at light-load conditions.

Peak and valley current limits protect against overload. MK9816 features input under voltage lockout (UVLO) and over-temperature protection.

2 Features

- Wide Input Voltage 7V-100V
- 0.6A Output Current Capability
- Integrated Always On 30mA LDO (VIN to V_{CC} pin)
- Programmable Zero Current Time (T_{ZC}) During PFM Mode
- Unique Enhanced On-time During PFM Mode
- Internal 3.5ms Soft-start
- Integrated 700mΩ High-side MOSFET
- Integrated 350mΩ Low-side MOSFET
- Smart Power Saving and Ultra-fast Transient Response
- Fixed Switching Frequency 300kHz
- No Loop Compensation Components
- VIN, SW, EN Absolute Max. Voltage 110V
- Input UVLO, Output Over-voltage and Under-voltage Protection
- Over-current, Over-temperature Protection
- ESOP8 Package with Thermal PAD

3 Applications

- Low-power Isolated DC/DC
- Industry Power Systems
- Motor Drives, Telecom
- BMS (E-Bike, Electric Tools)

4 Typical Application

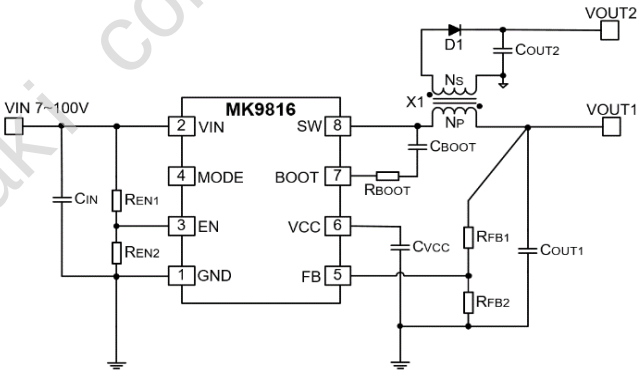

Figure 1. Typical Application Diagram

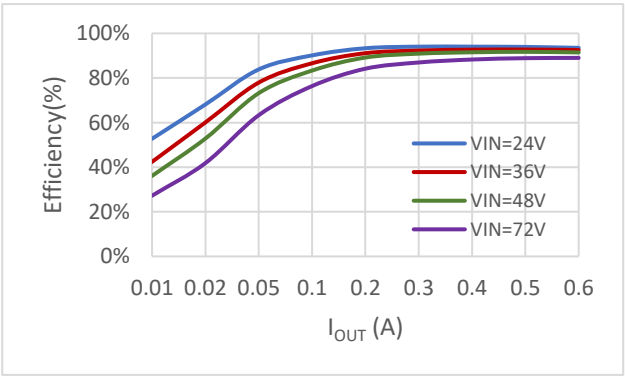

Figure 2. Efficiency, F_{SW}=300kHz, V_{OUT}=10V

5 Order Information

Part Number	Package Type	Package Qty	Eco Plan	MSL	Description
MK9816XAD	ESOP-8	4k/reel	RoHS & Green	MSL3	FSW=300kHz

6 Pin Configuration and Marking Information

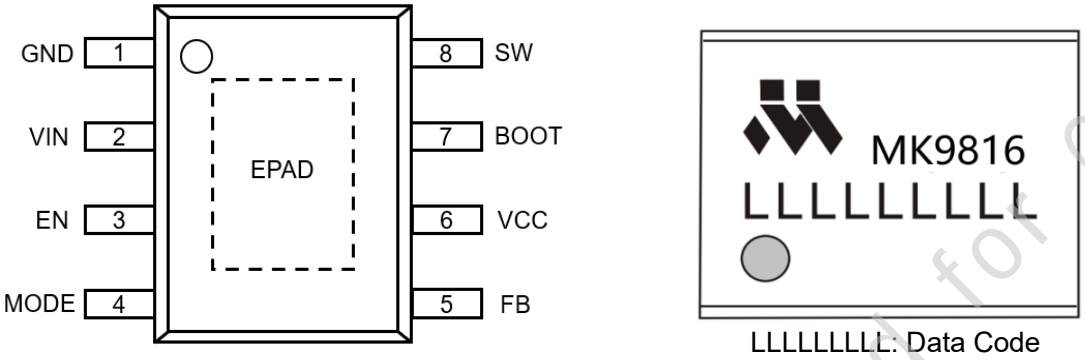

Figure 3. Pin Function (top view)

Table 1. Pin Functions

Pin		I/O (1)	Description
Number	Name		
1	GND	G	Ground
2	VIN	P/I	Input voltage pin. Decouple this pin to GND with low ESR capacitor. Connect to a VIN power plane to improve thermal performance.
3	EN	I	Enable control pin. (1) Resistor divider from VIN to EN to GND programs the undervoltage detection threshold. (2) Keep floating or pull up above 1.218V to enable the converter. When EN pin is pulled below 0.62V, the converter is in shutdown mode.
4	MODE	I	Operation mode selection pin. (1) Leave floating or a pull-down resistor ≥2MΩ for FCCM. (2) A 15kΩ~400kΩ resistor between MODE and GND to set zero current time duration in PFM mode.
5	FB	I	Feedback input, connect to output through the resistor divider.
6	VCC	I/O	LDO output and internal Bias generation input. A 1.0μF X7R decoupling capacitor is recommended.
7	BOOT	P/I	Boot-strap pin. Decouple this pin to SW pin with a 0.1uF X7R ceramic capacitor.
8	SW	P	Power switching node. Connect to the output inductor and bootstrap capacitor.
-	EPAD	-	Exposed pad of the package. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal.

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings (1)

		MIN	MAX	UNIT
Input Voltages (1)	VIN, EN, SW to GND	-0.3	110	V
	SW to GND (20ns pulse)	-3		
	BOOT to GND	-0.3	SW+6.6	
	FB, MODE to GND	-0.3	6.6	
	VCC to GND	-0.3	30	
Operating Junction Temperature (2)		-40	150	°C
Storage Temperature		-65	150	
Soldering Temperature (10 second)			260	

(1) Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in "Recommended Operating Conditions". Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

		Value	UNIT
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Recommended Operation Conditions	VIN Voltage	7	100	V
	EN Voltage	-0.3	100	
	SW Voltage	-0.3	100	
	Junction Temperature	-40	125	°C

7.4 Thermal Information

		Value	UNIT
Package Thermal Resistance	θ_{JA} (Junction to ambient)	30	°C/W
	θ_{JC} (Junction to case)	10	°C/W

7.5 Electrical Characteristics

F_{SW}=300kHz, V_{IN}=48V, V_{OUT}=10V, C_{OUT}=20uF. Typical values correspond to T_J=25°C, Minimum and Maximum limits apply over -40°C to 125°C junction temperature range unless otherwise indicated.

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Input Voltage						
V_{IN}	Input Voltage		7		100	V
V_{IN_UVLO}	Input Voltage UVLO	V_{IN} rising		5.7	6.5	V
Supply Current						
I_{Q1}	Quiescent current, Buck off, LDO on	V_{EN}=0V, VIN=48V		6.8	10	μA
I_{Q2}	Quiescent current, Buck on (none switching), LDO on	EN=5V, FB=1.5V		650	1200	μA
Feedback						
V_{REF}	Feedback reference voltage		1.198	1.218	1.238	V
EN						
V_{EN_H}	EN rising, enable switching	EN rising		1.22	1.27	V
V_{EN_L}	EN falling, disable switching	EN falling	1.12	1.17		V
$I_{EN\ Hysteresis}$	Hysteresis Input Current			-2		μA
V_{EN_SD}	Remote shutdown threshold	EN falling	0.42	0.62		V
Frequency						
F_{SW}	Switching frequency	MODE pin floating, No load		300		kHz
LDO (1)						
V_{LDO}	LDO output voltage	V_{EN}=0V, No load	7.5	8.5	9.5	V
		V_{EN}=0V, I_{LOAD} =30mA	5.3	6	7	V
I_{LDO}	LDO output current capability	VLDO=6V		30		mA
I_{LDOOC}	LDO foldback current limit	V_{EN}=0V, VLDO=0V		18		mA
Timing						
T_{ON_MIN}	Minimum on-time			155		ns
T_{OFF_MIN}	Minimum off-time			210		ns
T_{ZC}	Zero current time during PFM mode	MODE pull down resistor 50kΩ		9		us
Power Switches						
R_{DSON_HS}	High-side MOSFET RDSON			700		mΩ
R_{DSON_LS}	Low-side MOSFET RDSON			350		mΩ
High-side Current Limit						
I_{HSOC}	High-side current limit		1.2	1.4	1.6	A
Low-side Current Limit						
I_{LSOC}	Low-side source current limit		0.55	0.65	0.8	A

Soft Start						
T_{SS}	Soft-start time	V_{FB} from 0V to V_{REF}		3.5		ms
Thermal Shutdown (2)						
T_{SD}	Thermal Shutdown Threshold	T_J rising		165		°C
T_{HYS}	Thermal Shutdown Hysteresis			20		°C
V_{REF_OVP}	Feedback reference voltage to trigger OVP			107		%
V_{REF_UVP}	Feedback reference voltage to trigger UVP			35		%
T_{HICCUP}	Hiccup time during UVP protection			80		ms
$T_{SD(LDO)}$	Thermal Shutdown Threshold	VEN=0V		165		°C
$T_{HYS(LDO)}$	Thermal Shutdown Hysteresis	VEN=0V		20		°C

(1) At 25°C, LDO cannot maintain normal output if the time at 3W thermal loss exceeds 500ms, when EN is pulled down. If EN is pulled up, the LDO is not recommended for powering the system, avoid trigger LDO over temperature protection.

(2) Values are verified by characterization on bench, not tested in production.

7.6 Typical Characteristics

F_{SW}=300kHz, V_{IN}=48V, V_{OUT}=10V, C_{OUT}=20μF, T_A=25°C, unless otherwise specified.

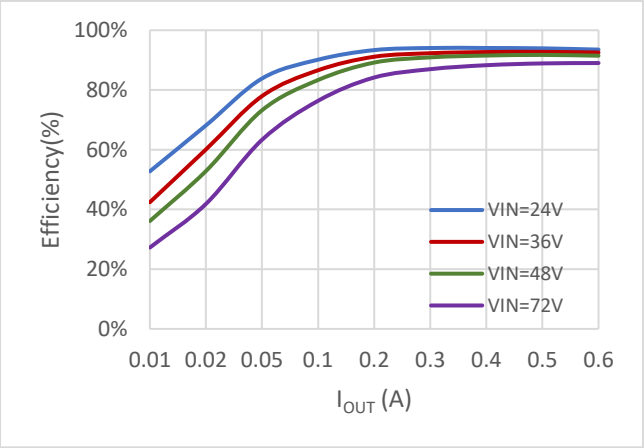

Figure 4. Buck Efficiency with V_{CC} diode, V_{OUT}=10V

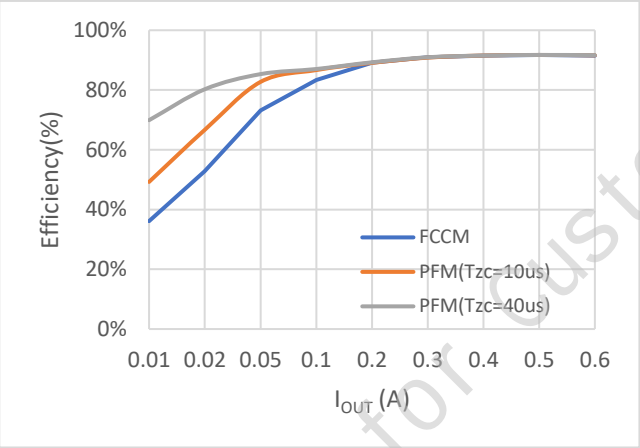

Figure 5. Buck Efficiency, V_{IN}=48V, V_{OUT}=10V

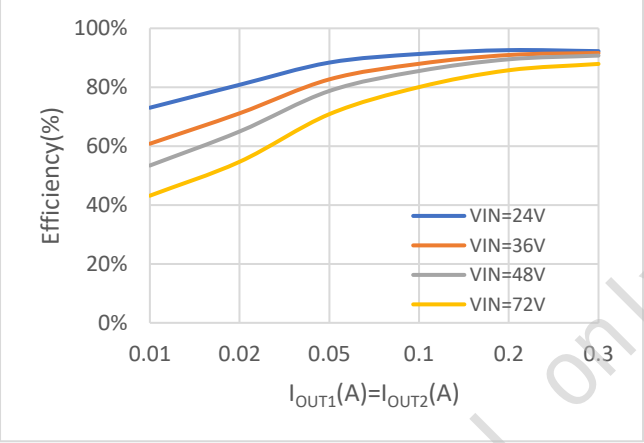

Figure 6. Efficiency with VCC diode, V_{OUT1}=V_{OUT2}=10V

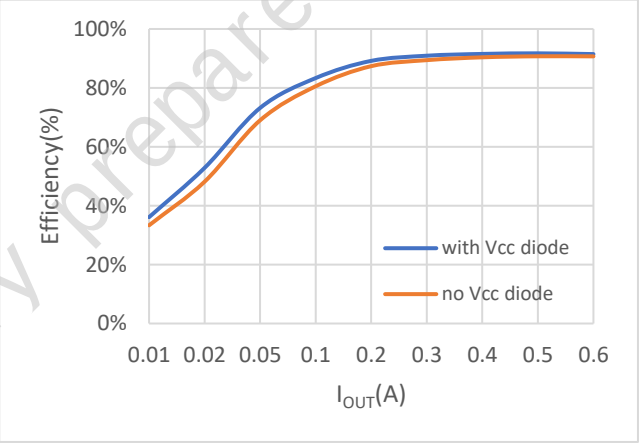

Figure 7. Buck Efficiency, V_{IN}=48V, V_{OUT}=10V

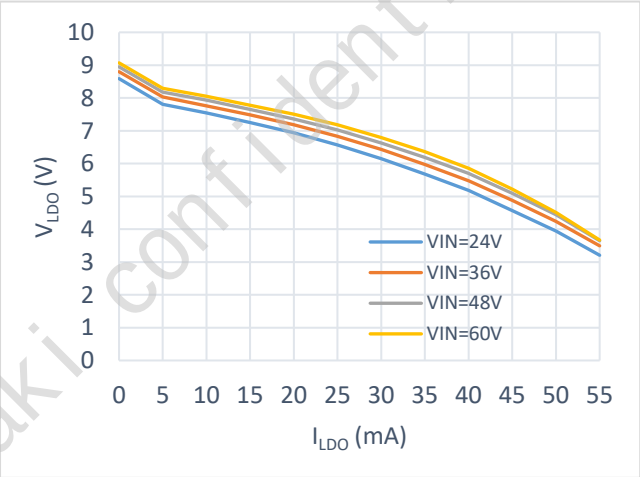

Figure 8. LDO load regulation, V_{LDO} VS I_{LDO}

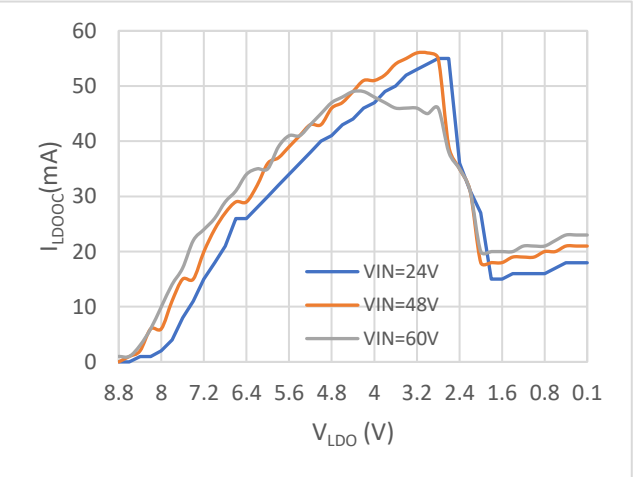

Figure 9. LDO current foldback character, I_{LDOOC} VS V_{LDO}

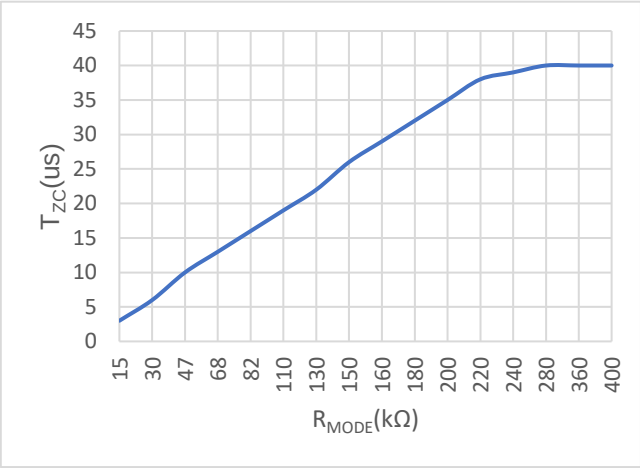

Figure 10. Adjustable T_{ZC}, T_{ZC} VS R_{MODE}

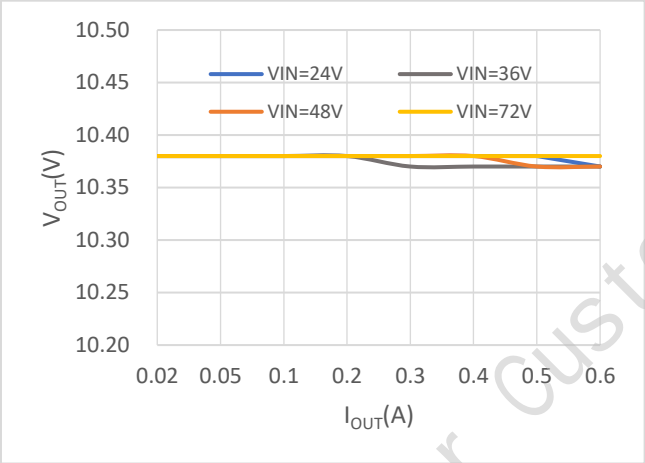

Figure 11. Load and line regulation

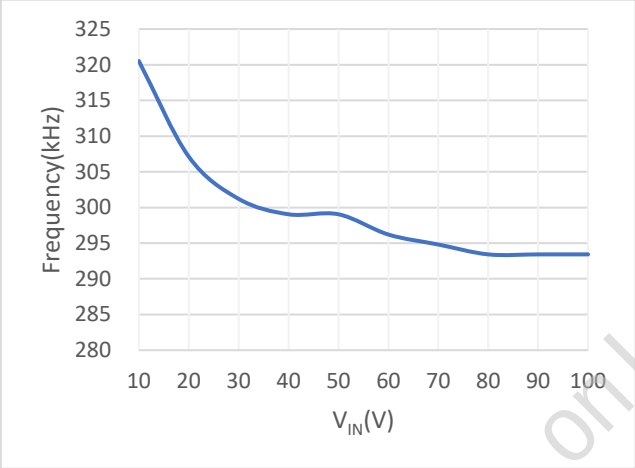

Figure 12. Frequency VS V_{IN}

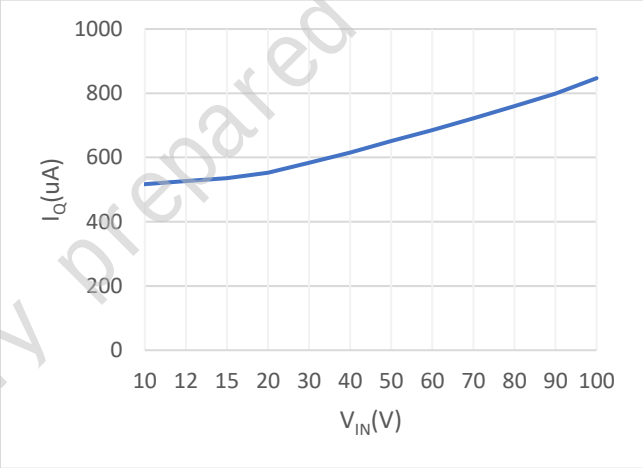

Figure 13. I_Q VS V_{IN}

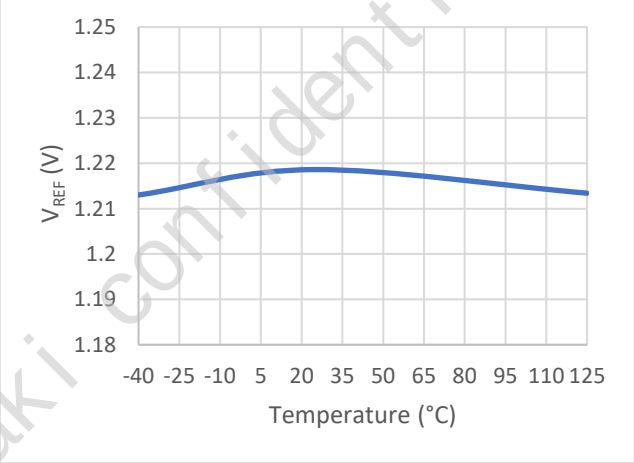

Figure 14. V_{REF} VS Temperature

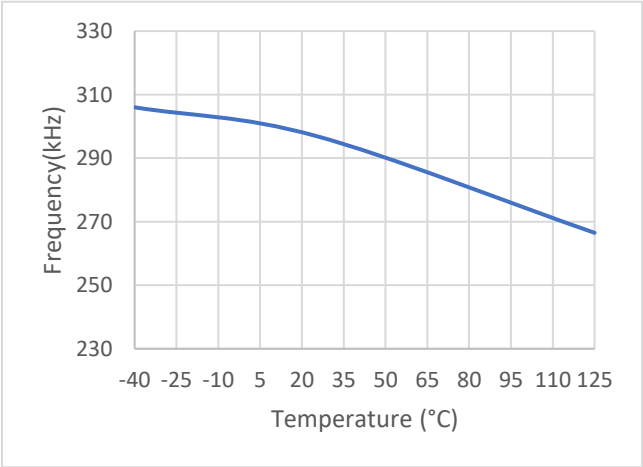

Figure 15. Frequency VS Temperature

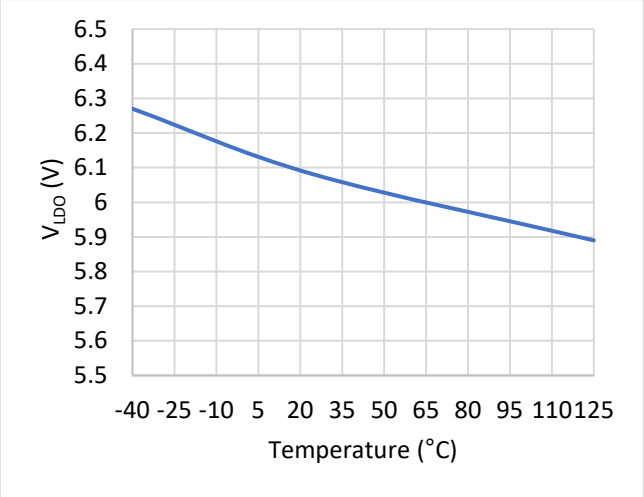

Figure 16. V_{LDO} VS Temperature, I_{LDO}=30mA

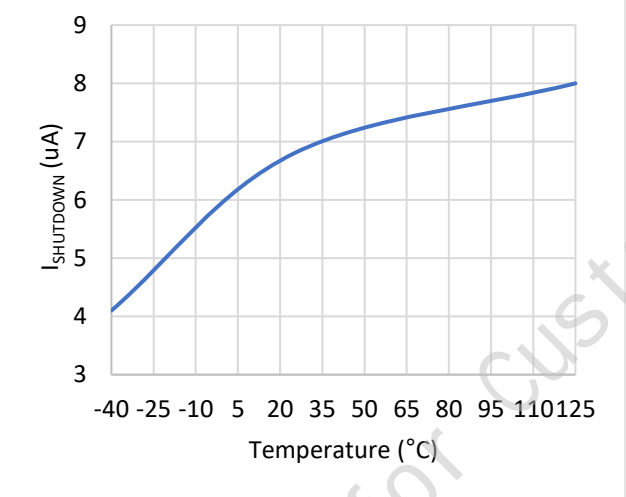

Figure 17. $I_{SHUTDOWN}$ VS Temperature

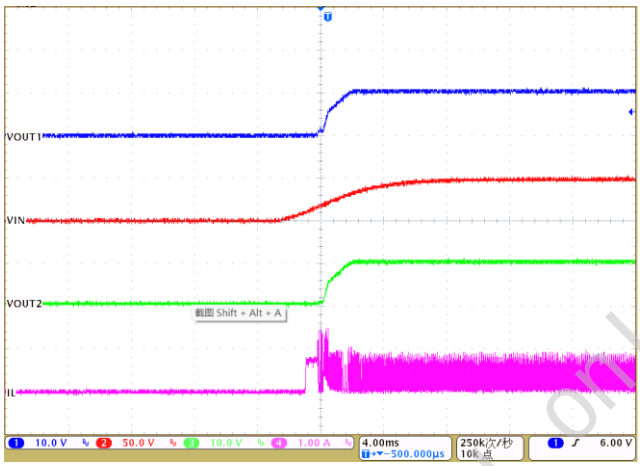

Figure 18. Power on from V_{IN}, I_{OUT1}=0.4A, I_{OUT2}=0.2A

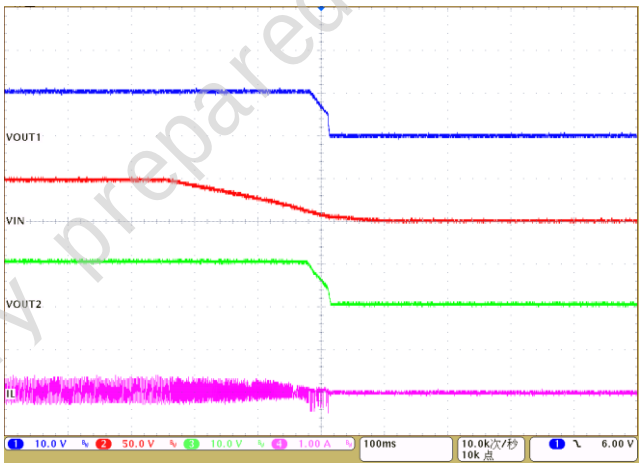

Figure 19. Power off from V_{IN}, I_{OUT1}=0.4A, I_{OUT2}=0.2A

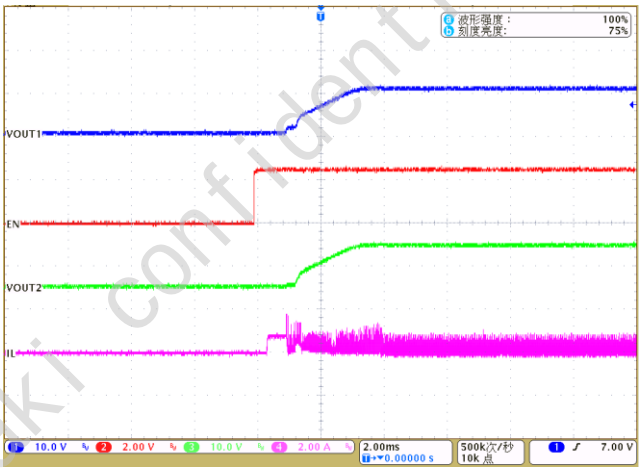

Figure 20. Power on from EN, I_{OUT1}=0.4A, I_{OUT2}=0.2A

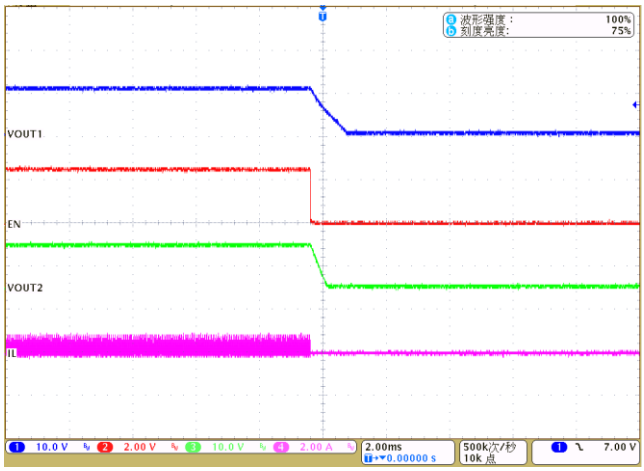

Figure 21. Power off from EN, I_{OUT1}=0.4A, I_{OUT2}=0.2A

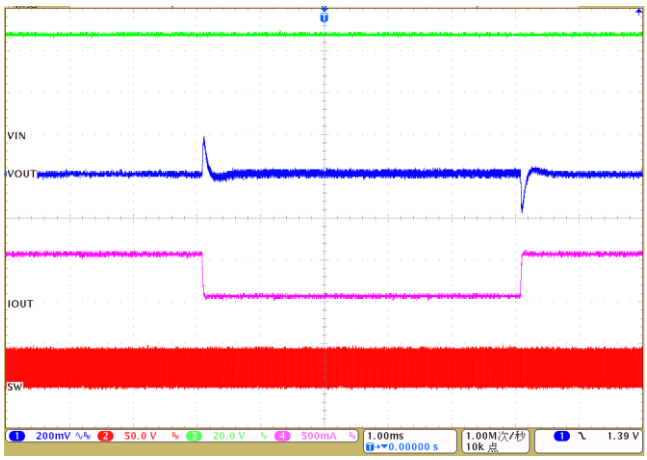

Figure 22. Load Transient, I_{OUT1}=0.1~0.6A

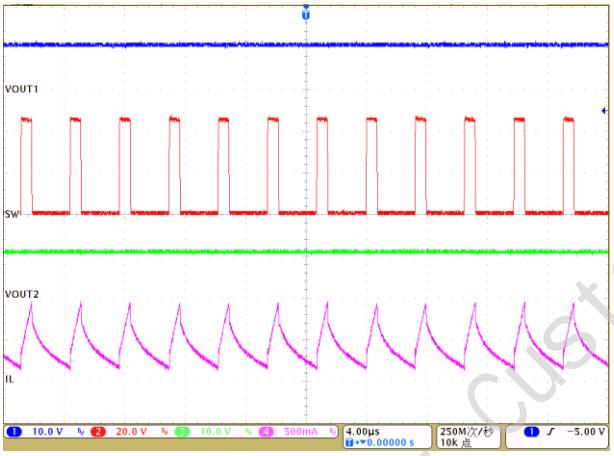

Figure 23. Steady state, I_{OUT1}=I_{OUT2}=0.3A

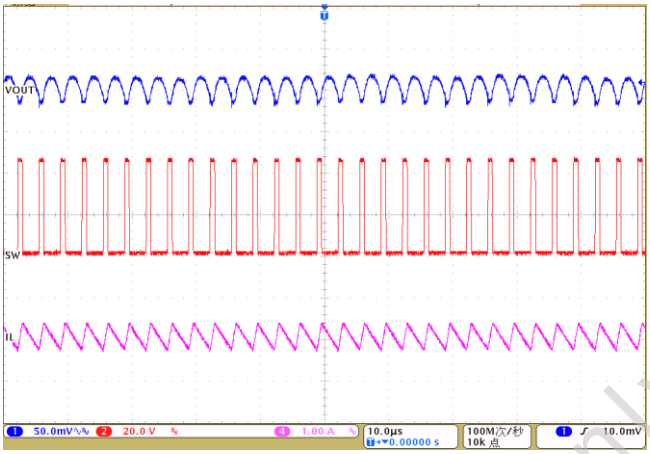

Figure 24. Output ripple, I_{LOAD}=0A, FCCM

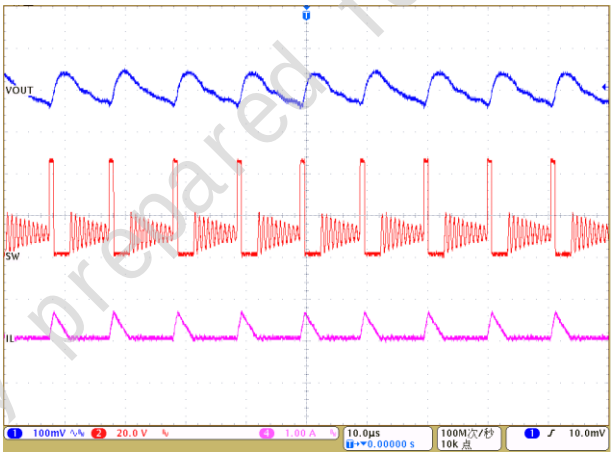

Figure 25. Output ripple, I_{LOAD}=0.1A, PFM, R_{MODE}=47k

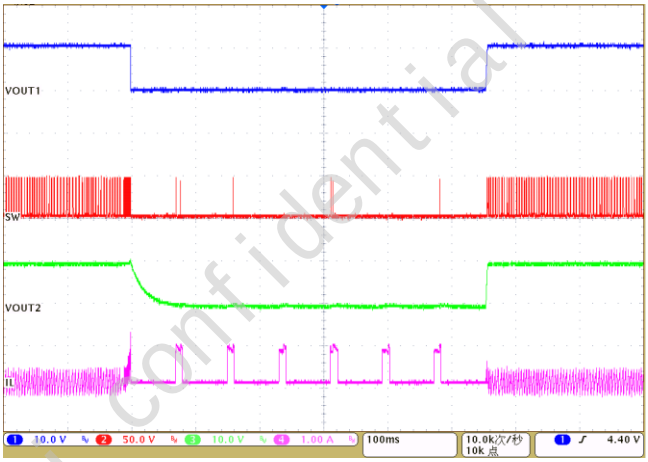

Figure 26. Primary side short protection and recovery

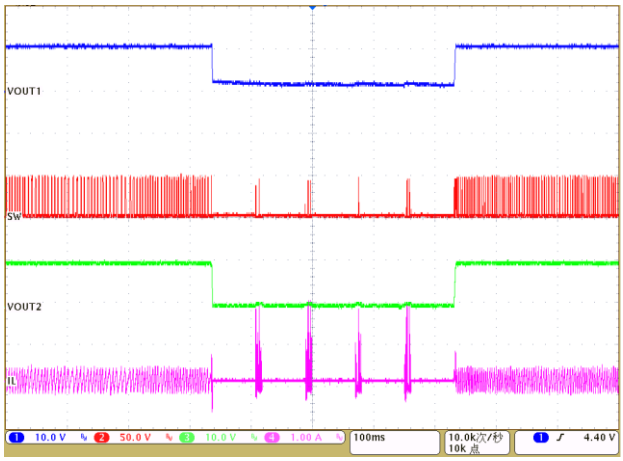

Figure 27. Secondary side short protection and recovery

8 Detailed Description

8.1 Overview

The MK9816 is a synchronous stepdown (Buck) converter operating over a wide input voltage range from 7V to 100V. With the main MOSFET and synchronous MOSFET integrated, the MK9816 delivers up to 600mA output current.

The MK9816 supports Forced Continuous Conduction Mode (FCCM) and intelligent Pulse Frequency Modulation Mode (PFM) techniques. In CCM mode, the switching frequency is fixed at 300kHz.The PFM frequency is programmable, by adjusting the zero current time (T_{ZC}) to achieve light load high efficiency and keep frequency above audible frequency areas to avoid audible noise.

The MK9816 integrates an internal high voltage LDO, which could deliver up to 30mA output current. The variation of LDO output voltage is shown in *Figure 8*. LDO always is enabled, whether EN is high or low.

The MK9816 protection features input under voltage lockout (UVLO), the output over-voltage and under-voltage protection, over current protection, output hard short protection, and thermal shutdown protection.

8.2 Functional Block Diagram

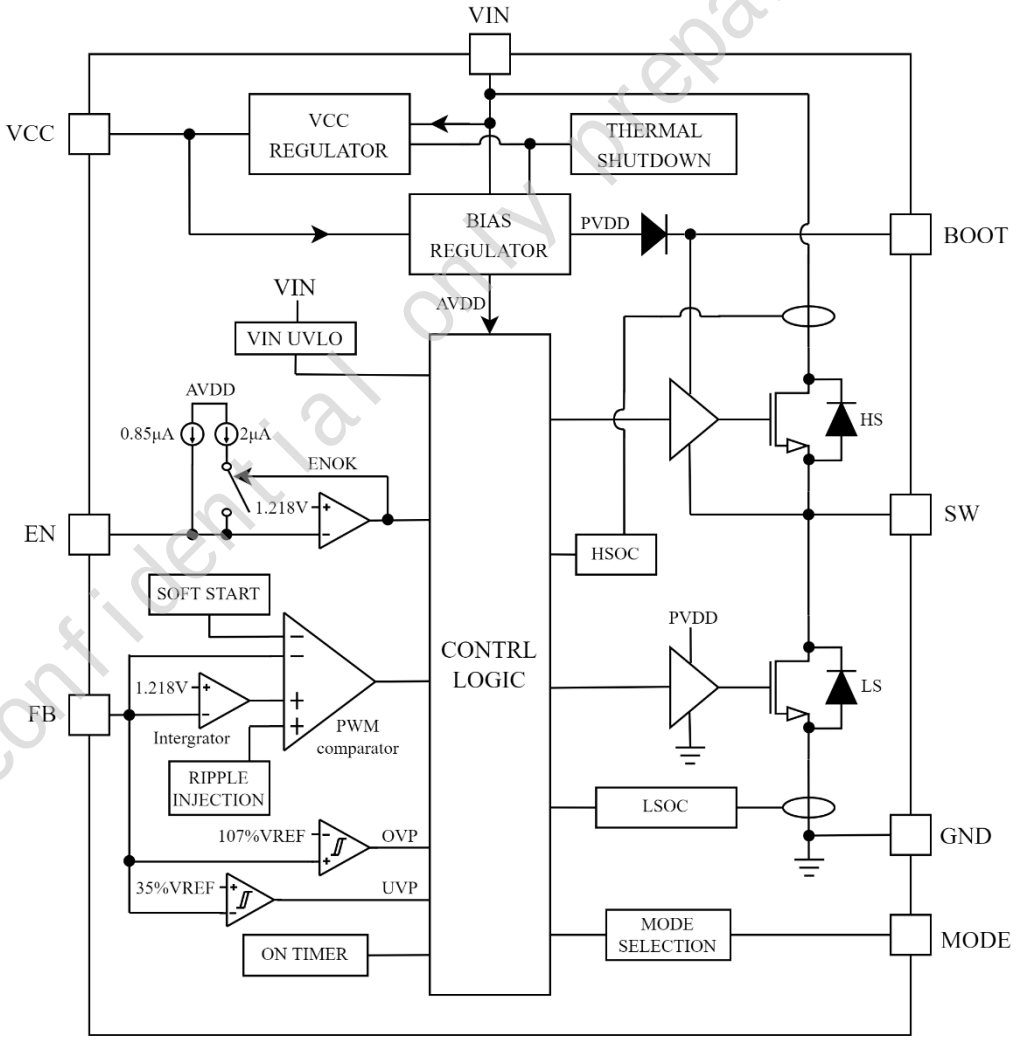

Figure 28. Block Diagram

8.3 Feature Description

8.3.1 Constant On-Time Control

The MK9816 adopts a constant on-time (COT) control architecture to achieve excellent transient response and enable very high step-down ratio. COT control scheme, in which the on-time is terminated by an on-timer, and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time.

The MK9816 does not need external loop compensation components to achieve simple design. However, the R_{BOOT} resistance needs to be connected to provide flexibility for optimizing the loop stability.

8.3.2 Output Voltage

Choose R_{FB1} and R_{FB2} to program the output voltage. For target V_{OUT} setpoint, calculate R_{FB1} and R_{FB2} using below equation:

$$V_{OUT} = 1.218\text{V} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

R_{FB1} and R_{FB2} is not recommended for use with MΩ resistors for most applications. Larger feedback resistors consume less DC current, which is important if light-load efficiency is critical. But too large of resistors are not recommended as the feedback path would become more susceptible.

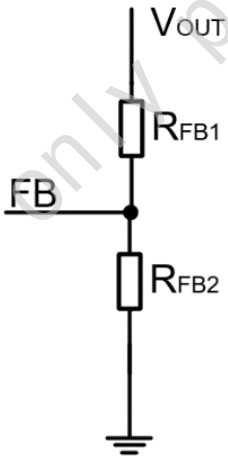

Figure 29. Feedback Resistor Divider

8.3.3 VCC Regulator

The LDO supports output current foldback function. When the LDO voltage is very low, the output current of the LDO will be limited. The limited current value is shown in *Figure 8*.This scheme protects the LDO start up with high current, when LDO output is anomaly.

Also, the internal VCC regulator as input to bias generation, it provides bias supply for the gate drivers and other internal circuitry. If the VCC voltage is powered by output voltage source, this will reduce the power dissipation in the IC and improve the efficiency.

8.3.4 Mode Selection

The MK9816 features different operation modes by programming the MODE pin. The programming information is listed in following table.

Table 2. MODE Pin config for different operation mode

MODE pin config	Operation Mode	T_{ZC} (us)	Frequency(kHz)
Connect to GND by a 15kΩ~400kΩ resister	PFM	3~40	22~143
Floating/Connect to GND by a ≥2MΩ resister	FCCM		

8.3.5 Soft-Start

The MK9816 integrates an internal soft-start circuit that avoids V_{OUT} spikes during startup, with the nominal internal soft-start time of 3.5ms. If the EN pin is pulled below 1.218V, the internal soft-start resets.
The soft-start also resets during shutdown due to thermal shutdown.

8.3.6 Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver of high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

8.3.7 Undervoltage Detector

Input UVLO can be programmed by EN rising threshold. The UVLO turn-on voltage can be calculated as:

$$V_{UVLO} = (1 + \frac{R_{EN1}}{R_{EN2}}) \times V_{EN\_H}$$

V_{EN_H} is EN rising threshold voltage, typical is 1.218V.
The UVLO hysteresis is accomplished with an internal 2μA current source that is switched on or off into the impedance of the set-point divider. When the voltage at the EN pin exceeds the rising threshold, the current source is activated to quickly raise the voltage at the EN pin. The hysteresis can be calculated as:

$$V_{hys}(\mathrm{V}) = R_{EN1} \times 2\mu\mathrm{A}$$

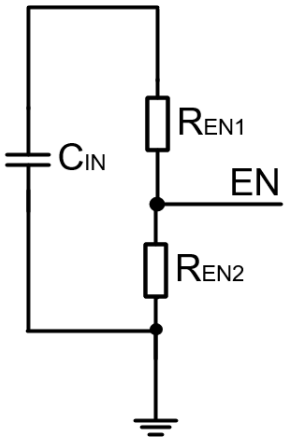

Figure 30. EN Resistor Divider

8.3.8 Current Limit

The current passing through the low-side MOSFET is constantly monitored for output overload. If the current exceeds Low-side current limit (LSOC), the signal that turns on High-side MOSFET is shielded, and the Low-side MOSFET remains on, until the current below the LSOC and the High-side MOSFET is turned on. After the LSOC, if the output load continues to increase and the output voltage falls below the UVP threshold, the output under-voltage protection is triggered with hiccup mode. The hiccup mode is described in section 8.3.10

Also，MK9816 contains high-side MOSFET current limit. The High-side MOSFET is turned off，if the current exceeds High-side current limit, to prevent output overload.

8.3.9 Over Voltage Protection

The MK9816 implements the output Over-voltage Protection circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The over voltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 107% of internal reference V_{REF}, the high-side MOSFET turns off to avoid output voltage from continuing to increase, and the low-side MOSFET will turn on to discharge the output voltage.

8.3.10 Under Voltage Protection

The MK9816 implements the output Under-voltage Protection with hiccup mode. When FB voltage falls below 35% of internal reference V_{REF}, the MK9816 enters hiccup mode. Hiccup mode starts after a 150us delay. The hiccup mode interval time is 80ms.

8.3.11 Unique enhanced on-time during PFM mode

During PFM mode, the regulation of secondary side (V_{OUT2}) becomes very bad. The MK9816 will generate a larger on-time with a larger load of V_{OUT2} so that larger current can be delivered to V_{OUT2} during PFM mode. The load regulation of V_{OUT2} is much better than traditional constant on-time PFM mode.

8.3.12 Thermal Shutdown

The junction temperature once exceeds 165°C, the power MOSFETs stop switching. When the junction temperature falls below 145°C, the device restarts.

9 Application and Implementation

9.1 Typical Applications

9.1.1 Typical application 1

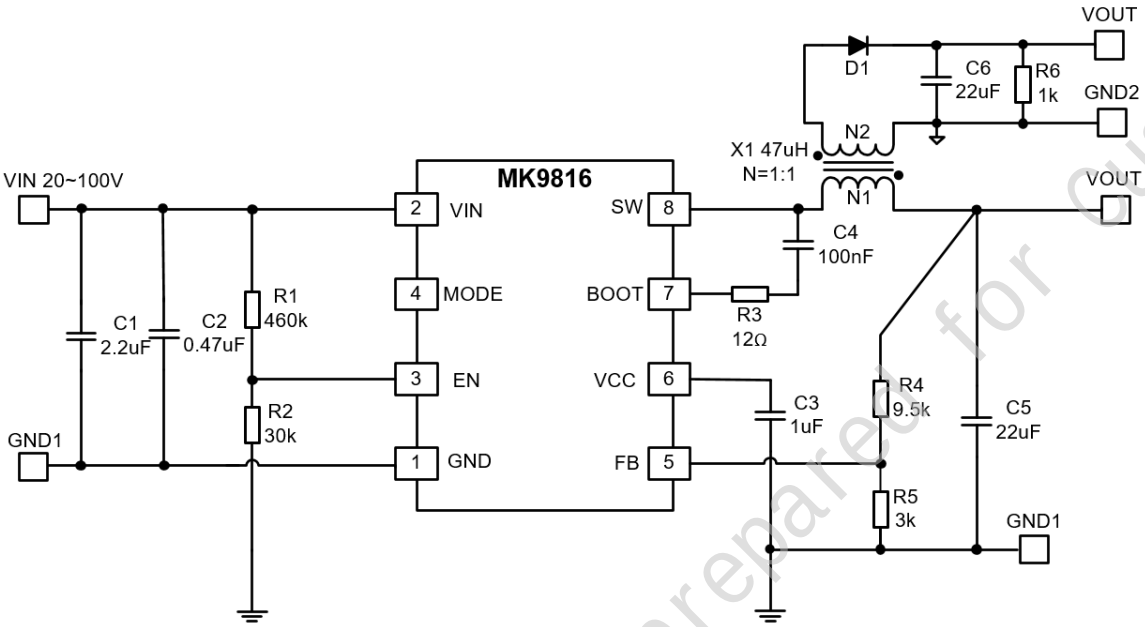

Figure 31. ISO-Buck, FCCM mode, without V_{CC} Diode

Design Parameters

Parameter	Example Value
Input Voltage, V_{IN}	48V Type，20V ~ 100V
Output Voltage, V_{OUT1}/V_{OUT2}	5V
Transformer, X1	47uH, N2:N1=1:1
Maximum Output Current, I_{OUT1}+I_{OUT2}	0.6A
Switching Frequency	300kHz Type

9.1.2 Typical application 2

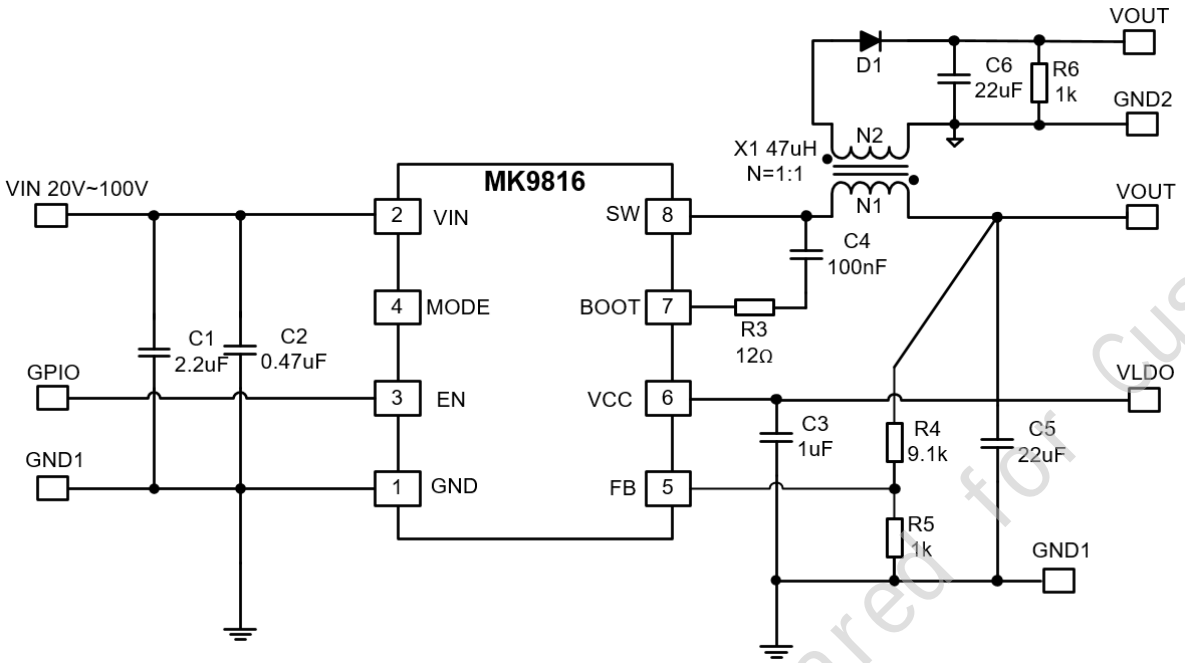

Figure 32. ISO-Buck, FCCM mode, LDO output supply for MCU standby

Design Parameters

Parameter	Example Value
Input Voltage, V_{IN}	48V Type，20V ~ 100V
Output Voltage, V_{OUT1}/V_{OUT2}	10V
Transformer, X1	47uH, N2:N1=1:1
Maximum Output Current,	0.6A
Switching Frequency	300kHz Type
LDO	When EN is pulled down, LDO output supply for MCU standby. LDO operating time at 3W thermal loss not exceeds 500ms. For example, V_{IN}=100V, V_{LDO}=6V, I_{LDO}=32mA, LDO thermal loss is equal to (100V-6V) *0.032=3W.

9.1.3 Typical application 3

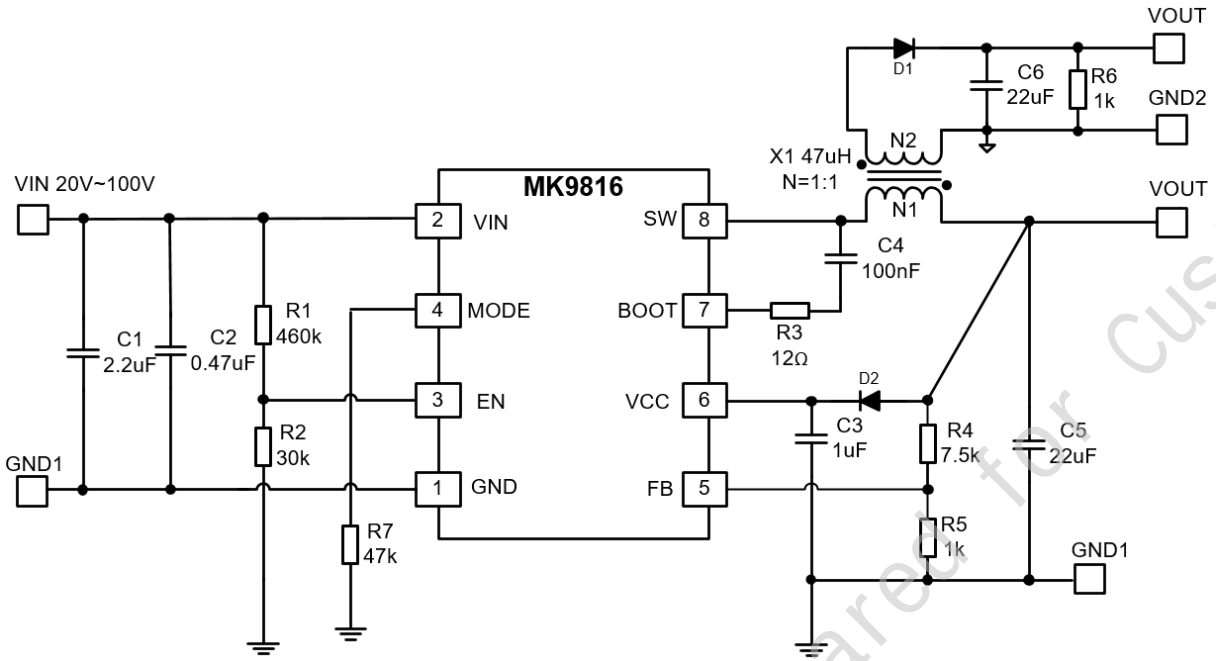

Figure 33. ISO-Buck, PFM mode, VCC with Diode

Design Parameters

Parameter	Example Value
Input Voltage, VIN	48V Type，20V ~ 100V
Output Voltage, VOUT1/VOUT2	10V
Transformer, X1	47uH, N2:N1=1:1
Maximum Output Current,	0.6A
Zero Current Time, T_{ZC}	10us
Voltage drops of D2, V_{D2}	0.7V
Switching Frequency	300kHz Type

9.1.4 Typical application 4

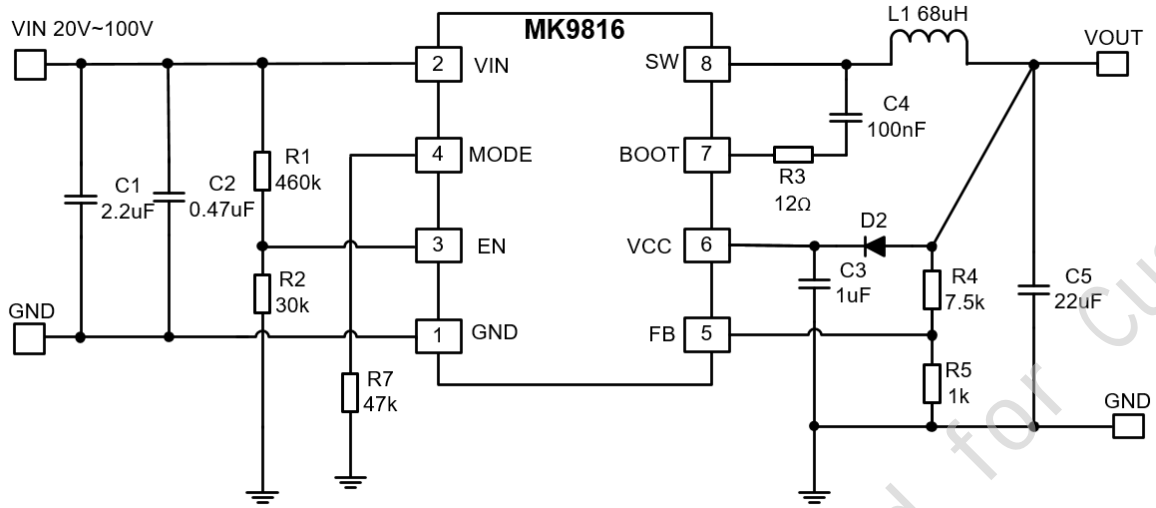

Figure 34. Buck, PFM mode, VCC with Diode

Design Parameters

Parameter	Example Value
Input Voltage, V_{IN}	48V Type，20V ~ 100V
Output Voltage, V_{OUT}	10V
Transformer, X1	47uH, N2:N1=1:1
Maximum Output Current, I_{OUT}	0.6A
Zero Current Time, T_{ZC}	10us
Voltage drops of D2, V_{D2}	0.7V
Switching Frequency	300kHz Type
Output Ripple	40mV, I_{LOAD}=0mA

9.2 Detailed design parameter

9.2.1 Selection of VOUT and Turns Ratio

The transformer turns ratio is selected based on the ratio of the primary output voltage to the secondary (isolated) output voltage. In this design example, the two outputs are nearly equal and a 1:1 turns ratio transformer is selected.

The primary output voltage should be no more than one half of the minimum input voltage. For example, at the minimum VIN of 36 V, the primary output voltage (VOUT1) should be no higher than 18V. Using this turns ratio, the required primary output voltage VOUT1 is calculated by the following equation:

$$V_{out1} = \frac{V_{out2} + V_{d1}}{N_2/N_1}$$

The Vd1 is forward voltage drop of the secondary rectifier diode. Setting the primary output voltage VOUT1 by selecting the feedback resistors, the secondary voltage is regulated at VOUT2 nominally. Adjustment of the primary side VOUT1 may be required to compensate for voltage errors due to the leakage inductance of the transformer, the resistance of the transformer windings, the diode drop in the power path on the secondary side.

9.2.2 RFB1, RFB2 Selection

The output voltage is set by an external resistor divider R4 and R5 in typical application schematic. The selected value for R5 is 1kΩ, R4 can be calculated using the following equations.

$$R_4 = 1.218\text{V} \times (\frac{V_{out}}{R_5} - 1)$$

9.2.3 EN Resistors

The UVLO threshold and hysteresis can be programmed by R_{EN1} and R_{EN2}. For a UVLO hysteresis of 0.92 V and UVLO rising threshold of 20V, require R1 of 460kΩ and R2 of 30kΩ and these values are selected for this design example.

$$V_{hys}(\text{V}) = R_1 \times 2\mu\text{A}$$

$$V_{UVLO} = (1 + \frac{R_1}{R_2}) \times V_{EN\_H}$$

9.2.4 Output Inductor

It is recommended to choose the ripple current of inductor between 30% to 50% of the rated load current I_{OUT} (max) for most applications. The inductance is calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

And the peak current of inductor is calculated as:

$$I_L(\text{peak}) = I_{OUT}(max) + \frac{\Delta I_L}{2}$$

The saturation current rating of the inductor must greater than the I_L (peak). An inductor whose saturation current is above the current limit setting of the MK9816 will be best choice. Note that inductor saturation current levels generally decrease as the inductor temperature increase.

9.2.5 Boot-strap Capacitor and Resistor

A 0.1μF X7R capacitor of 16 V or higher rating and a 12Ω resistor is recommended between BOOT pin and SW pin. The 12Ω resistor must be connected for optimizing the loop stability.

9.2.6 Input Capacitor

An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck converter at every switching cycle. The input ripple voltage ΔV_{IN} at input capacitor is calculated as:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1-D)}{F_{SW} \times (\Delta V_{IN} - I_{OUT} \times R_{ESR})}$$

To minimize the potential noise problem, a X7R or better grade capacitor with sufficient voltage rating is recommended. This capacitor should be close to the VIN and GND pins to minimize the loop area formed by C_{IN} and VIN/GND pins. In this application, a 2.2μF and 0.47uF X7R low ESR ceramic capacitor is recommended.

9.2.7 Output Capacitor

The output capacitor limits the capacitive voltage ripple at the converter output. This voltage ripple which is generated from the triangular inductor current ripple flowing into and out of the capacitor can be calculated as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times F_{SW} \times C_{OUT}}$$

Above equation only takes the steady state ripple into consideration. The transient requirements also must be taken into consideration when selecting the output capacitor. The X7R or better grade ceramic capacitor larger than 22μF is recommended.

9.2.8 VCC Capacitor Selection

A 1-μF capacitor of 16 V or higher rating is recommended for the VCC regulator bypass capacitor.

9.2.9 Secondary Diode

The reverse voltage across secondary-rectifier diode D1 can be calculated as:

$$V_{d1} > \frac{N_2}{N_1} * VIN_{(MAX)} + Vout2$$

For a V_{IN_MAX} of 100 V and the 1:1 turns ratio of this design, a 150-V Schottky is selected in this application.

9.2.10 VCC Diode

Diode D2 is an optional diode connected between V_{OUT1} and the V_{CC} regulator output pin. It is recommended with $V_{OUT1} > V_{D2}$+7.5V if D2 is used to supply bias current.

10 Power Supply Recommendations

MK9816 is a power-management device. The power supply for the device is any dc voltage source within the specified input range.

11 Layout

11.1 Layout Guidelines

To achieve high performance of the MK9816, the following layout tips must be followed.

1. C_{IN}: At least one low-ESR ceramic bypass capacitor C_{IN} must be used. Place the C_{IN} as close as possible to the MK9816 V_{IN} and GND pins, place decoupling caps as close as possible between V_{IN} and catch diode's GND. Minimize the loop area formed by C_{IN} connections to V_{IN} and GND pins.
2. C_{VCC}, C_{BOOT} and R_{BOOT}: This capacitor and resistor must be placed as close to the IC as possible, and the connecting trace lengths and loop area should be minimized
3. Inductor must be placed close to the SW pin. Minimize the area of SW trace to avoid the potential noise problem.
4. Maximize the PCB area connecting to the GND pin to thermal pad. If it is allowed, a ground plane can be used as noise shielding and heat dissipation path.
5. Place the feedback resistors, R_{FB1} and R_{FB2}, close to the FB pin. Route the feedback VOUT sense path away from noisy nodes such as the SW net.
6. The MODE pin is sensitive to noise. Avoid all possible coupling noise, and not close to magnetic components and switching trace.

11.2 Layout Example

The layout of the DEMO board contains circuits that V_{OUT2} connect to an LDO (U2)

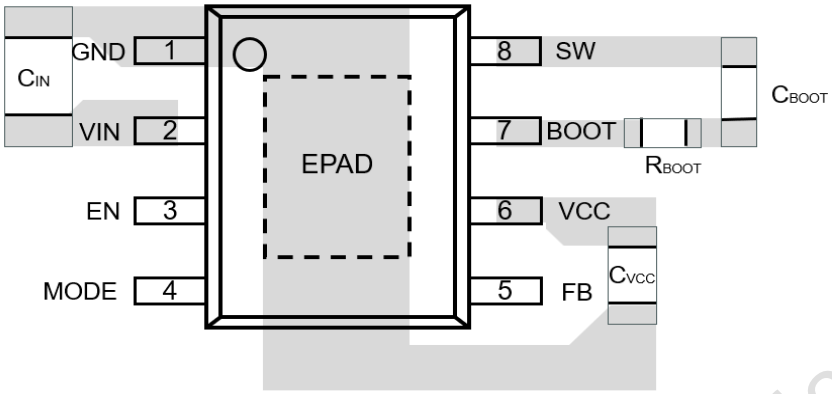

Figure 35. Layout example

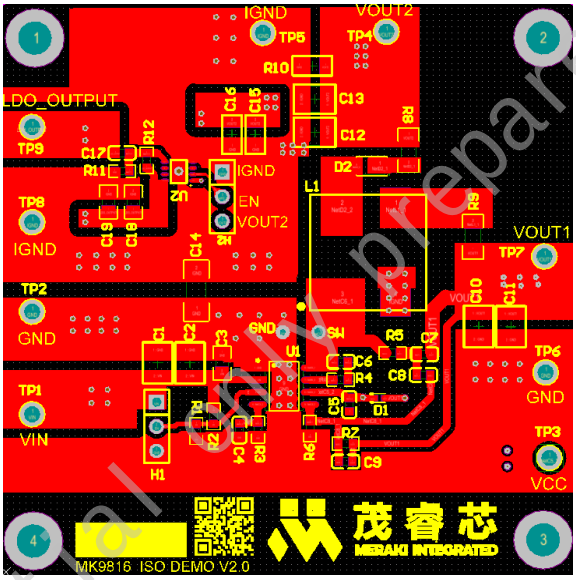

Figure 36. DEMO Layout (Tope Layer)

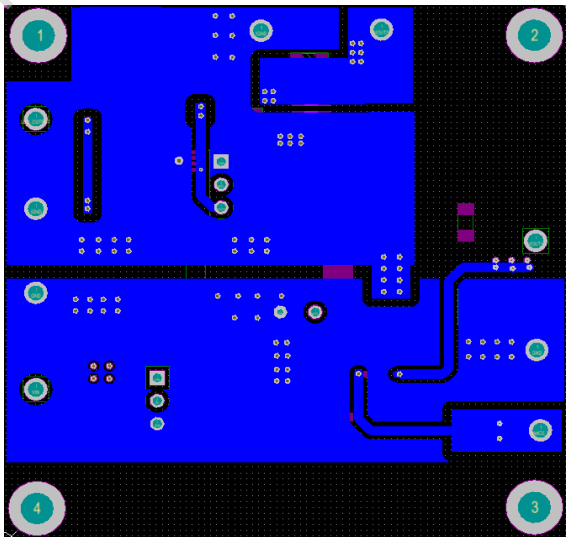

Figure 37. DEMO Layout (Bottom Layer)

12 Receiving Notification of Documentation Updates

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13 Mechanical, Packaging

13.1 Package Size

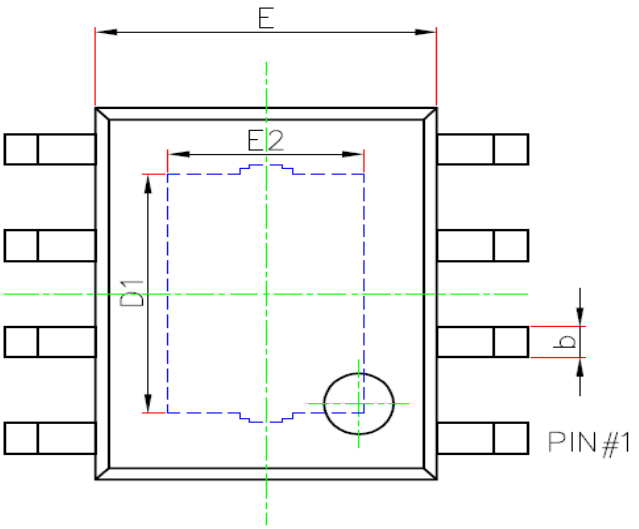

Figure 38. MK9816 Top View

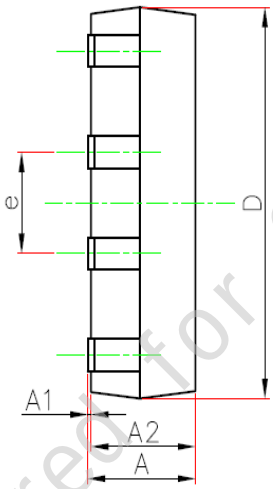

Figure 39. MK9816 Side View

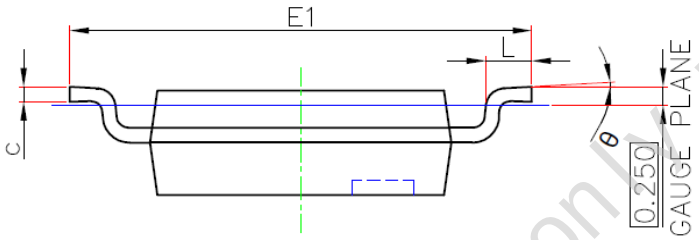

Figure 40. MK9816 Side View

Symbol	Dimensions In Millimeters	
	MIN	MAX
A	1.30	1.70
A1	0.00	0.10
A2	1.35	1.55
b	0.33	0.51
c	0.17	0.25
D	4.70	5.10
E	3.80	4.00
E1	5.80	6.20
D1	3.05	3.25
E2	2.16	2.36
e	1.270(BSC)	
L	0.4	1.27
θ	0°	8°

13.2 Recommended Land Pattern

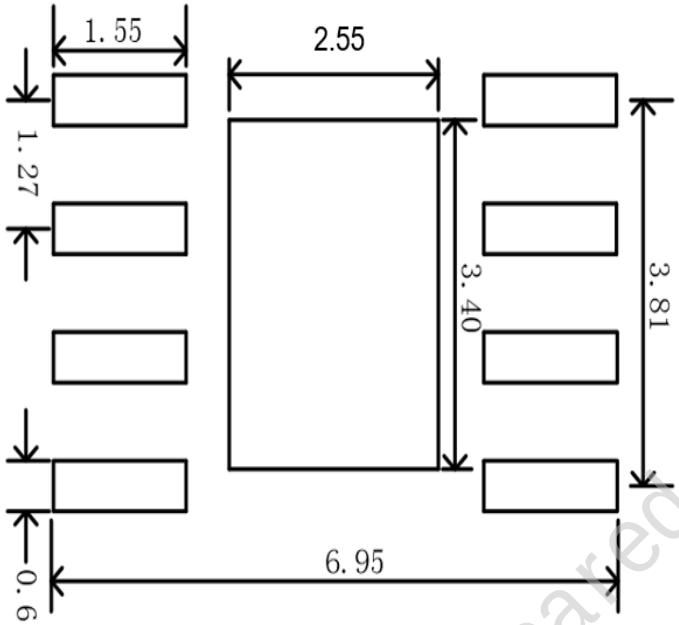

Figure 41. Recommend Land and Pattern

Note:

（1） All linear dimensions are in millimeters.

14 Reel and Tape Information

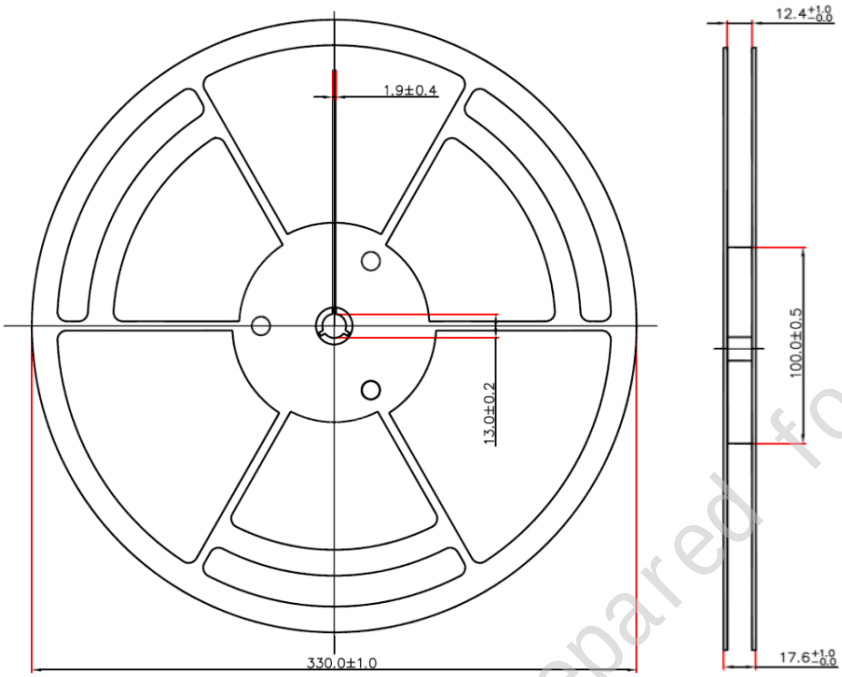

Figure 42. Reel Dimensions

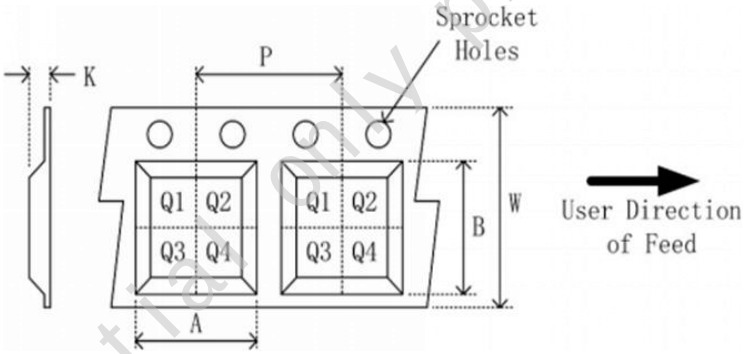

Figure 43. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

Device	Package Type	Pins	SPQ	A	B	K	P	W	Pin1
			(pcs)	(mm)	(mm)	(mm)	(mm)	(mm)	Quadrant
MK9816	ESOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8±0.1	12±0.1	Q1

15 Tape and Reel Box Dimensions

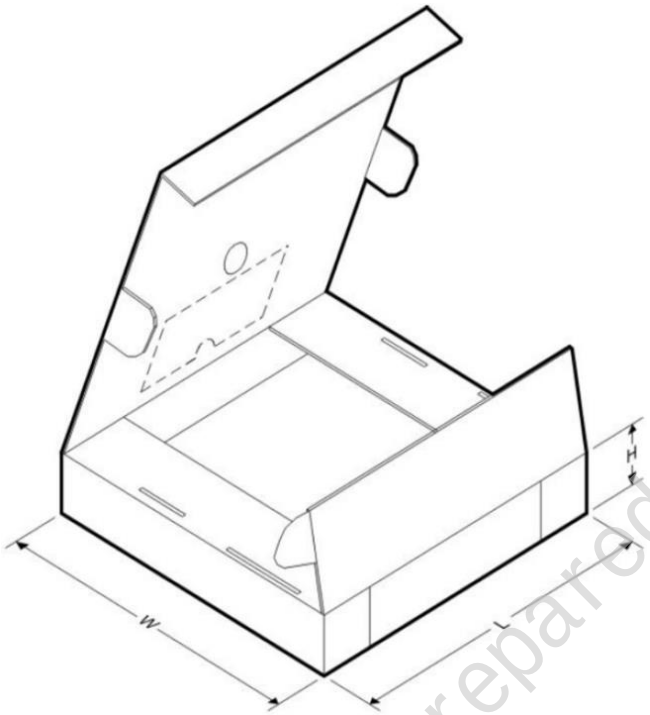

Figure 44. Box Dimensions

Device	Package Type	Pins	SPQ	Length	Width	Height
			(pcs)	(mm)	(mm)	(mm)
MK9816	ESOP-8	8	8000	360	360	65