85V Synchronous Buck DC/DC Controller

1. Descriptions

MK9286 supports wide input voltage ranges from 6V to 85V. With appropriate external high-side and low-side MOSFETs and inductor, MK9286 delivers up to 30A output current.

MK9286 adopts a voltage mode control scheme to achieve excellent accurate voltage output. The switching frequency is adjustable up to 1MHz, which also can be synchronized to an external clock to eliminate beat frequencies.

Both Forced-PWM (FPWM) and diode emulation mode is supported by MK9286. FPWM helps to minimize EMI by operating at constant frequency, while diode emulation mode lowers current consumption at light-load condition.

Wide duty cycle from 1% to 98% is offered by MK9286 under appropriate switching frequency, so input and output voltages can be chosen easily.

MK9286 also provides a power good (PG) flag pin to indicate output voltage, and an internal LDO output (VCC pin). For high efficiency applications, an external bias power supply is recommended to apply to VCC pin after start-up.

2. Features

- Wide input voltage range of 6V-85V
- Adjustable output voltage from 0.8V to 60V
- 45ns Ton(min) for low duty ratio
- 145ns Toff(min) for high duty ratio
- Precision ±1% feedback reference
- Adjustable F_{SW} from 100kHz to 1MHz
- Configurable diode emulation or FPWM
- 2.5A source and 3.5A sink driver capability
- Prebias start-up
- SYNCI and SYNCO capability
- Open-Drain power good indicator
- Adjustable output voltage soft start
- Input UVLO with hysteresis
- VCC UVLO protection
- OC, OT protection with hiccup mode
- 3.5x4.5 QFN-20 package with thermal PAD

3. Applications

- PoL modules
- High-Power density DC – DC
- Datacenter and telecom
- Non-isolated PoE and IP cameras

4. Typical Application

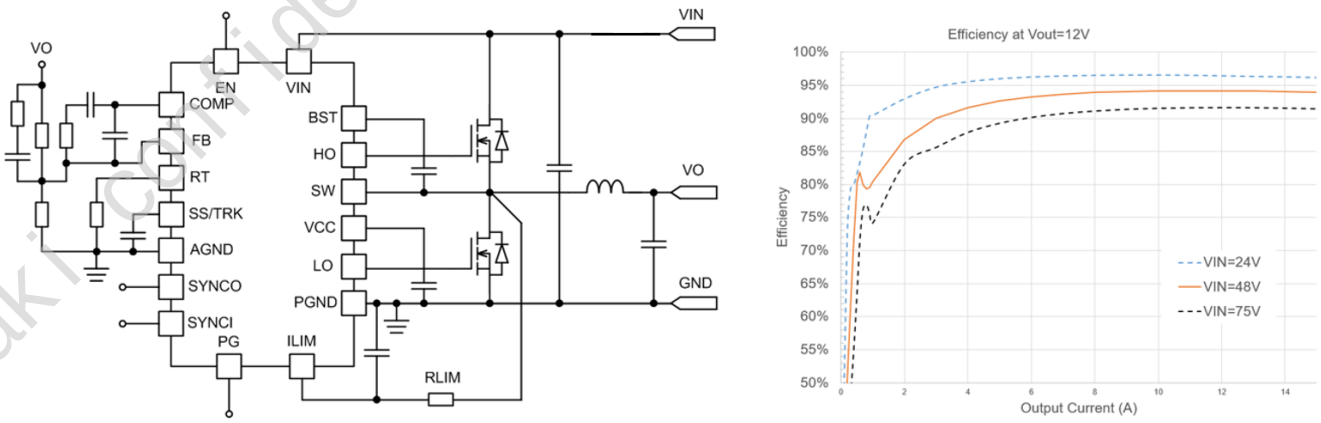


Figure 1. Typical Application Diagram and Efficiency

5. Order Information

Order No.	Description
MK9286DQB	MSL2,3.5x4.5 QFN-20, tape, 3000/reel

6. Pin Configuration and Functions

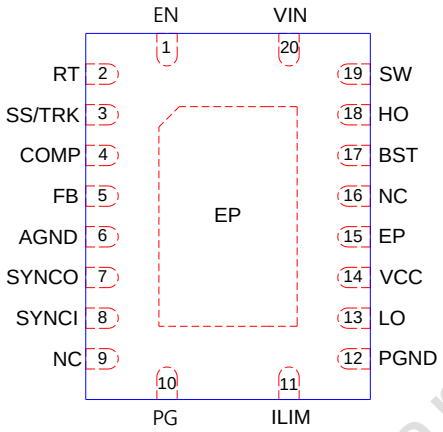


Figure 2. MK9286 Package (Top View)

Table 1. Pin Functions

Pin NO.	Name	I/O	Description
1	EN	I	Enable input and/or input undervoltage lockout programming pin. EN pin offers tri-state (shutdown、standby、operating) thresholds to reduce quiescent current consumptions. In operating state, an accurate 1.2V rising threshold, and an internal current source which is enabled once EN exceeds 1.2V to program falling threshold along with external resistors. Connecting with resistor divider from VIN, this pin sets input voltage UVLO threshold with programmable hysteresis, which is adjusted by varying the resistance of external resistor divider. V_{EN}＜0.75V,shutdown mode, VIN to VCC LDO shutdown；0.75V≤V_{EN}＜1.2V,standby mode, VIN to VCC LDO regulated to 7.5V；V_{EN}＞1.2V,operating mode, start to operating；
2	RT	O	Oscillator frequency set pin. The internal oscillator is programmed with a single resistor between RT and AGND.
3	SS/TRK	O	Soft-start and voltage-tracking pin. During start-up, output voltage tracks SS/TRK voltage; after start-up, output voltage tracks Ref.
4	COMP	O	Compensation pin. Low impedance output of the internal error amplifier. Connect the loop compensation network between the COMP pin and the FB pin.
5	FB	I	Feedback connection to the inverting input of the internal error amplifier. Connect this pin to the output resister divider to program the output regulation voltage: VOUT=0.8×(1+Rf1/Rf2)

6	AGND	P	Analog ground. Return for the internal 0.8V voltage reference and analog circuits.
7	SYNCO	O	Synchronization output. Logic level output that provides a clock signal that is 180° out-of-phase with the HS FET drive signal.
8	SYNCI	I	Synchronization input. Tri function: 1.optional external clock input 2.low-side MOSFET diode emulation mode 3.FPWM.
9	NC	-	No electrical connection.
10	PG	O	Power good indicator. This pin is an open-drain output pin. Connect to a source voltage through a pull-up resistor.
11	ILIM	I	Current limit set pin. Connect a resistor to SW to sense Rdson of low-side MOSFET or to sense resister which is connected between the source of low-side FET and PGND in order to adjust current limit.
12	PGND	P	Power ground.
13	LO	O	LS MOSFET gate driver output. Connect to the gate of the low-side MOSFET through a short, low inductance path.
14	VCC	I	VCC. Output of the 7.5V bias regulator. Locally decoupled to PGND using a low ESR/ESL capacitor located as close as possible to the controller.
15	EP	-	Connection to exposed pad
16	NC	-	No electrical connection.
17	BST	O	Boot-strap supply. Decouple this pin to SW pin with a 100nF ceramic capacitor located as close as possible to the controller.
18	HO	O	HS MOSFET gate driver output. Connect to the gate of the high-side MOSFET through a short, low inductance path.
19	SW	P	Switching node. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET using short, low inductance paths.
20	VIN	P	Supply input. Decouple this pin to PGND with low ESR ceramic capacitor.
-	EP	-	Exposed pad. Solder the EP to the PGND pin and connect to a large copper plane to reduce thermal resistance.

7. Specifications

7.1 Absolute Maximum Ratings

		Min	Max	Units
Input Voltages	VIN, EN, SW, ILIM to GND	-0.3	85	V
	SW to PGND (20ns pulse)	-5	85	
	VCC, SYNCI, SYNCO, PG to AGND	-0.3	14	
	FB, COMP, SS/TRK, RT to AGND	-0.3	6.6	
	BST to GND	-0.3	100	
	BST to VCC	0	95	
	BST, HO to SW	-0.3	14	
	VCC to BST (20ns pulse)	0	14	
	LO to GND (20ns pulse)	-5	14	
Operating Junction Temperature, TJ		-40	150	°C
Storage Temperature, Tstg		-55	150	
Soldering Temperature (10 second), Tsld			260	

Note:

(1) Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in “Recommended Operating Conditions”. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		Value	Units
Electrostatic Discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000(3)	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

(3) EN/ILIM Human body model (HBM) Passed ±1000V

7.3 Recommended Operating Conditions

		Min	Max	Units
Recommended Operation Conditions	VIN Voltage	7	80	V
	EN Voltage	-0.3	80	
	SW Voltage	-0.3	80	
	BST Voltage	-0.3	100	
	ILIM Voltage	-0.3	80	
	Operating Junction Temperature	-40	+125	°C

7.4 Thermal Information

		Value	Units
Package Thermal Resistance	θ_{JA} (Junction to ambient)	36.8	°C/W
	θ_{JC} (Junction to case)	28	°C/W

7.5 Electrical Characteristics

V_{IN}=48V, V_{OUT}=12V, I_{OUT}=5A, L=4.7uH, C_{OUT}=400uF, R_{RT}=25K,T_A=-40°C to 125°C, unless otherwise specified

Parameter		Test Conditions	Min	Typ	Max	Unit
Input Voltage						
V_{IN}	Input voltage		6		85	V
Supply Current						
V_{IN}	Operating voltage		6		85	V
I_{Q-SDN}	Shutdown current	V_{EN}=0V		8.5	15	uA
I_{Q-STBY}	Standby current	V_{EN}=1V		0.6	0.7	mA
I_{Q-RUN}	Operating current, no switching	V_{EN}=1.5V, $V_{SS/TRK}$=0V		1.7	2.2	mA
VCC Regulator						
V_{VCC}	VCC regulation voltage	$V_{SS/TRK}$=0V,9V≤V_{IN}≤85V,0mA≤I_{VCC}≤20 mA	7.1	7.5	8	V
I_{SC-LDO}	VCC max current	$V_{SS/TRK}$=0V,V_{CC}=0V	18	26	38	mA
$V_{VCC-FALLING}$	VCC undervoltage threshold	V_{CC} falling	4.45	4.7	4.95	V
$V_{VCC-RISING}$	VCC UVLO threshold	V_{CC} rising	4.7	5	5.3	V
$V_{VCC-UVH}$	VCC undervoltage hysteresis	Rising threshold-falling threshold		0.26		V
$V_{VCC-EXT}$	Minimum external bias supply voltage	＞V_{CC}	8.2			V
I_{VCC}	External VCC input	$V_{SS/TRK}$=0V,V_{CC}=13V		1.7	2.2	mA
EN						
$V_{EN-STBY}$	EN rising to standby threshold	Vcc rising	0.58	0.75	0.91	V

V_{EN-SD}	EN falling to shutdown threshold	Vcc falling	0.48	0.65	0.79	V
V_{EN}	EN rising to operating threshold		1.12	1.2	1.33	V
I_{EN-HYS}	Hysteresis input current	V_{EN}=1.5V	6	8	10	uA
Feedback Amplifier						
V_{REF}	Feedback reference voltage	$V_{FB}=V_{COMP}$	0.792	0.8	0.808	V
V_{COMP-H}	COMP output high voltage	V_{FB}=0V, COMP sourcing 1 mA		4		V
V_{COMP-L}	COMP output low voltage	COMP sinking 1 mA			0.3	V
I_{FB}	FB input bias current	V_{FB}=0.8V	-0.1		0.1	uA
SS/TRK						
I_{SS}	SS/TRK charging current	$V_{SS/TRK}$ = 0.1 V	5	8	11	uA
V_{SS-FB}	SS/TRK to FB offset		-15	0	13	mV
$V_{SS-CLAMP}$	SS/TRK to FB clamp voltage	$V_{SS/TRK}$-V_{FB} (0.8V)	200	300	400	mV
PG						
PG_{UTH}	FB upper threshold for PG high to low	% of V_{REF}, V_{FB} rising	105	108	111	%
PG_{LTH}	FB lower threshold for PG high to low	% of V_{REF}, V_{FB} falling	89	92	95	%
$T_{PG-RISE}$	PG rising filter	FB to PG rising edge	18	25	35	us
$T_{PG-FALL}$	PG falling filter	FB to PG falling edge	18	29	55	us
V_{PG-OL}	PG low state output	V_{FB}=0.9V, I_{PG}=2mA			150	mV

I_{PG-OH}	PG high state leakage current	V_{FB}=0.8V, V_{PG}=13V			200	nA
Frequency						
F_{SW}	Programmable switching frequency	$F_{SW}(kHz) = \frac{10^4}{R_T(K\Omega)}$	100		1000	kHz
SYNCI and SYNCO						
F_{SYNCI}	SYNCI external Fsw	% of F_{SW} set by R_{RT}	-20		50	%
R_{SYNCI}	SYNCI input resistance	V_{SYNCI}=3V	14	20	26	kΩ
$T_{SYNCI-DEL}$	Delay from SYCNI leading edge to HO rising	50% to 50%		250		ns
$T_{SYNCO-DEL}$	Delay from HO rising to SYNCO leading edge	V_{SYNCI}=0, T_S=1/F_{SW}, 50% to 50%		T_S/2-250		ns
PWM Control						
T_{ON-MIN}	Minimum on-time	HO rising to falling, VBST-VSW=7V	20	45	75	ns
$T_{OFF-MIN}$	Minimum off-time	HO falling to rising, VBST-VSW=7V	95	145	210	ns
D_{100K}	Maximum duty cycle	F_{SW}=100kHz,6V≤V_{IN}≤60V	95	98		%
D_{400K}	Maximum duty cycle	F_{SW}=400kHz,6V≤V_{IN}≤60V	85	90		%
V_{RAMP}	Minimum ramp valley	COMP at 0% duty cycle	190	240	350	mV
k_{FF}	Feedforward gain	V_{IN}/V_{RAMP}, 6V≤V_{IN}≤60V		18		V/V
BST						
V_{BST_FWD}	Diode forward voltage, VCC to BST	VCC to BST, BST pin sourcing 20 mA		0.85	1	V
I_{Q-BST}	BST to SW quiescent current, not switching	$V_{SS/TRK}$ = 0 V, V_{SW} = 48 V, V_{BST} = 54 V			10	uA

ILIM-OCP						
I_{RS}	ILIM source current, R_{SENSE} mode	Low voltage detected at ILIM	90	100	110	uA
I_{RDSON}	ILIM source current, $R_{DS(ON)}$ mode	SW voltage detected at ILIM TJ=25°C	180	200	220	uA
$V_{ILIM-TH}$	ILIM comparator threshold at ILIM		-13	0	13	mV
Hiccup(1)						
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycle with current limiting before hiccup off-time activated		512		cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycle with no switching followed by SS/TRK release		8192		cycles
Diode Emulation Mode						
V_{ZCD-SS}	ZCD soft-start ramp			0		mV
$V_{ZCD-DIS}$	ZCD disable threshold (CCM)		130	190	240	mV
V_{DEM-TH}	Diode emulation ZC threshold	Measured at SW with V_{SW} rising		0		mV
Drivers						
R_{HO-UP}	HO high-state resistance HO to BST	V_{BST}-V_{SW}=7V, I_{HO}=-100mA		1.5		Ω
$R_{HO-DOWN}$	HO low-state resistance HO to SW	V_{BST}-V_{SW}=7V, I_{HO}=100mA		0.9		Ω
R_{LO-UP}	LO high-state resistance LO to VCC	V_{BST}-V_{SW}=7V, I_{LO}=-100mA		1.5		Ω
$R_{LO-DOWN}$	LO low-state resistance LO to PGND	V_{BST}-V_{SW}=7V, I_{HO}=100mA		0.9		Ω

I_{HOH},H_{LOH}	HO,LO source current	V_{BST}-V_{SW}=7V, HO=SW LO=AGND		2.5		A
I_{HOL},H_{LOL}	HO,LO sink current	V_{BST}-V_{SW}=7V, HO=BST LO=VCC		3.5		A
T_{HO-TR} T_{LO-TR}	HO, LO rise times	VBST – VSW = 7 V, CLOAD = 1 nF, 20% to 80%		7		ns
T_{HO-TF} T_{LO-TF}	HO, LO fall times	VBST – VSW = 7 V, CLOAD = 1 nF, 80% to 20%		4		ns
T_{HO-DT}	HO turn-on dead time	VBST – VSW = 7 V, LO off to HO on, 50% to 50%	25	35	60	ns
T_{LO-DT}	LO turn-on dead time	VBST – VSW = 7 V, HO off to LO on, 50% to 50%	10	25	40	ns
Thermal Shutdown(2)						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD-HYS}	Thermal shutdown hysteresis			20		°C

Notes:

(1) Design guarantee

(2) Characterized at bench evaluations, not tested in mass production test.

7.6 Typical Characteristics

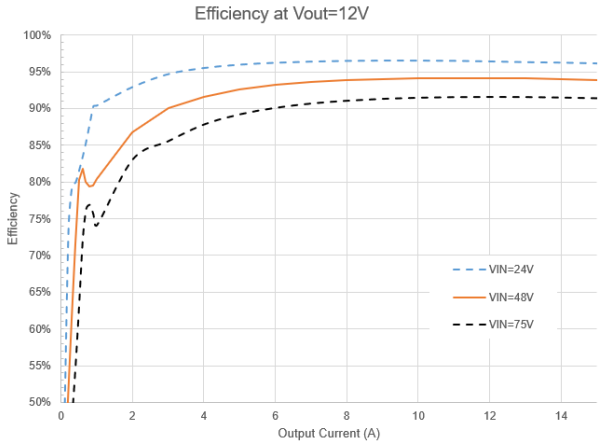


Figure 3. Efficiency at 12V-Vout(400kHz)

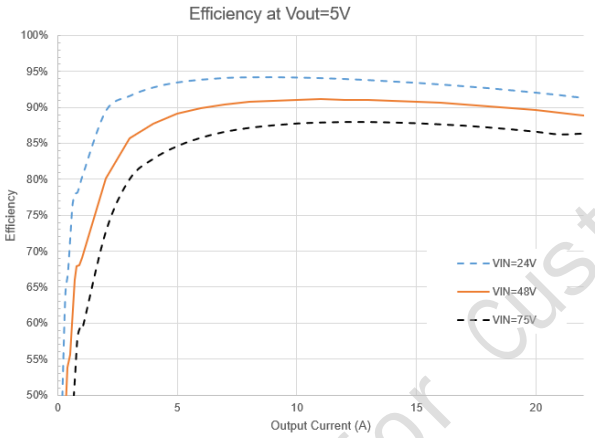
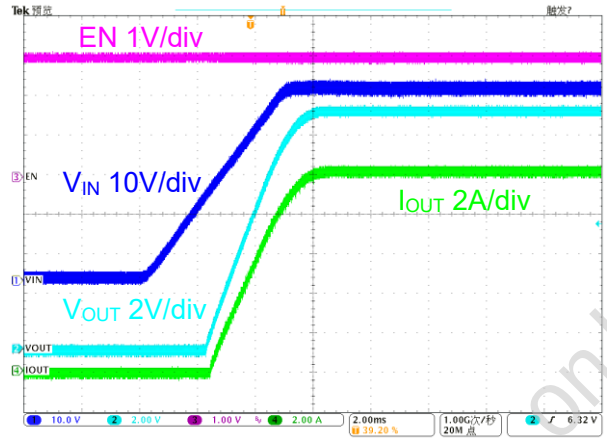
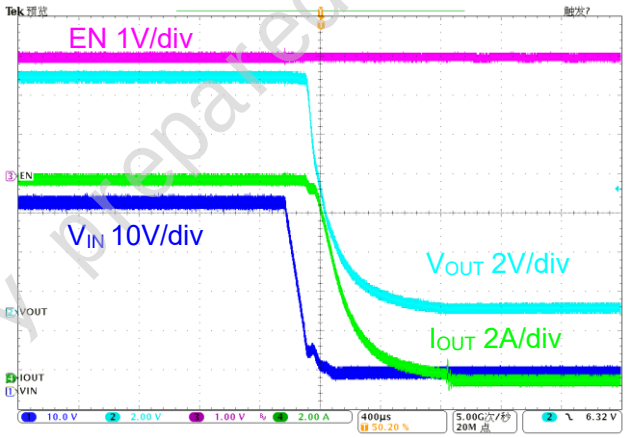


Figure 4. Efficiency at 5V-Vout(230kHz)



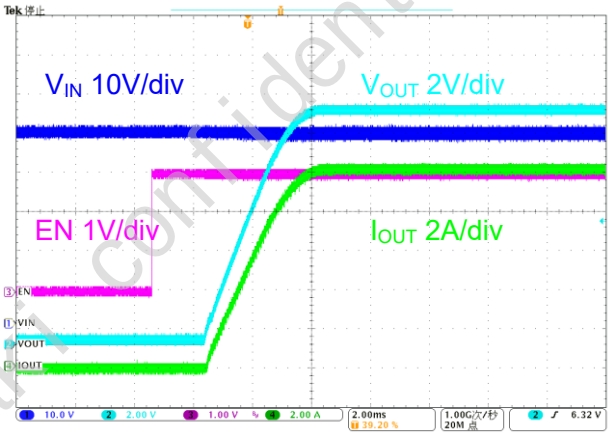
V_{IN}=48V Time(2ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 5. Startup by V_{IN}



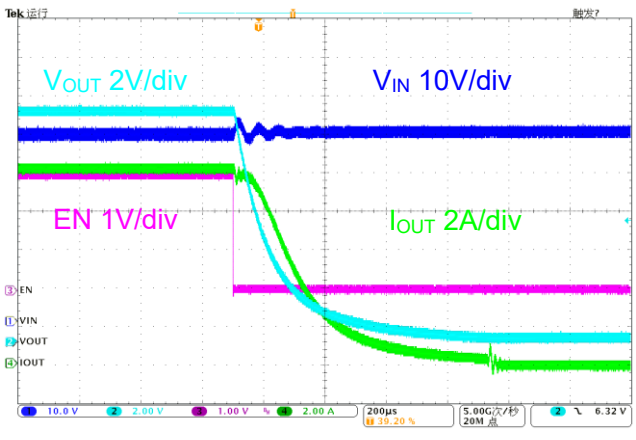
V_{IN}=48V Time(0.4ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 6. Shutdown by V_{IN}



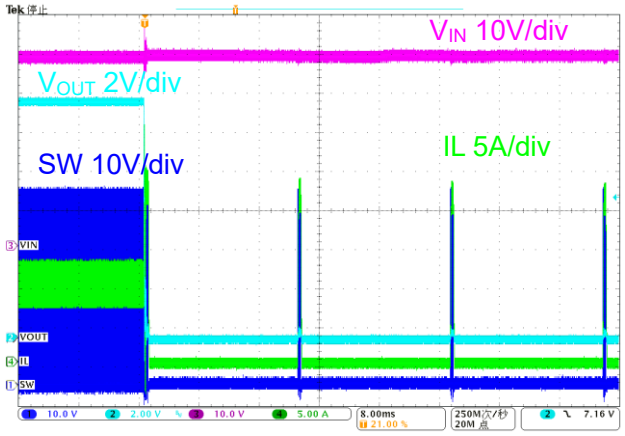
V_{IN}=48V Time(2ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 7. Startup by EN



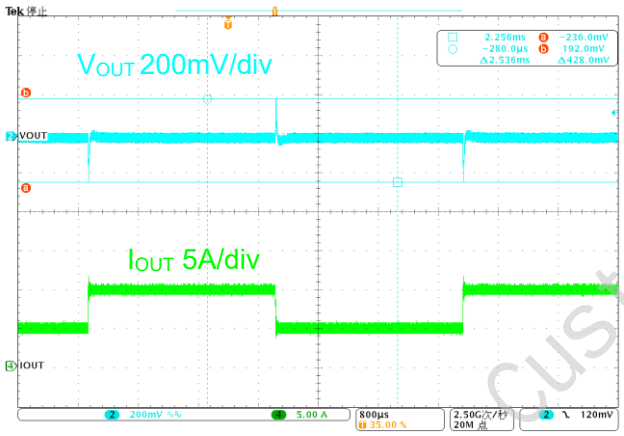
V_{IN}=48V Time(0.2ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 8. Shutdown by EN



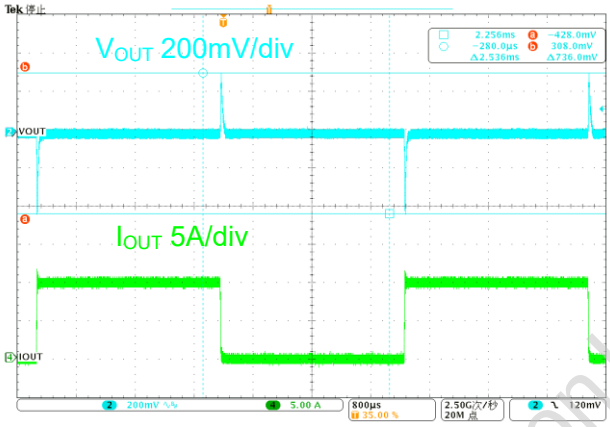
V_{IN}=48V Time(8ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 9. Short Protection and Recovery



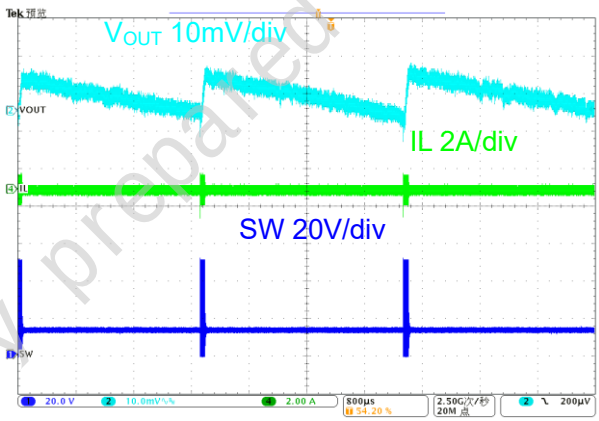
V_{IN}=48V Time(0.8ms/div) V_{OUT}=12V I_{OUT}=5A-10A

Figure 10. Load Transient



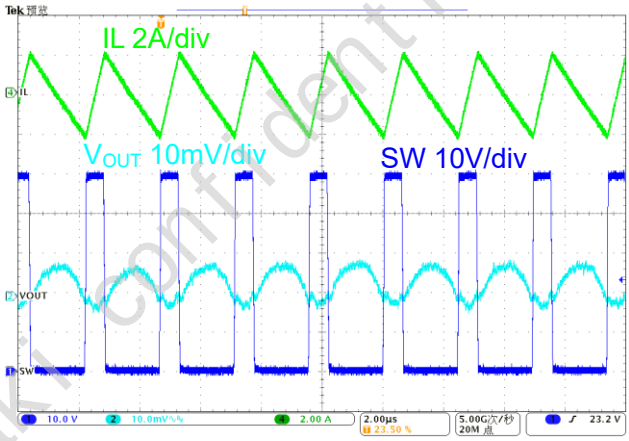
V_{IN}=48V Time(0.8ms/div) V_{OUT}=12V I_{OUT}=0A~10A

Figure 11. Load Transient



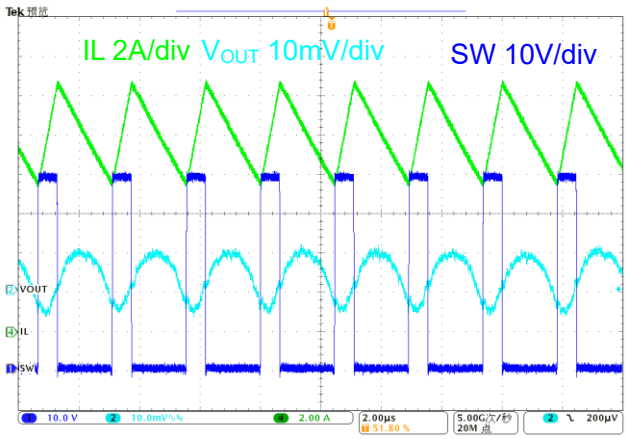
V_{IN}=48V Time(0.8ms/div) V_{OUT}=12V I_{OUT}=0A

Figure 12. Output Ripple (Diode Emulation Mode)



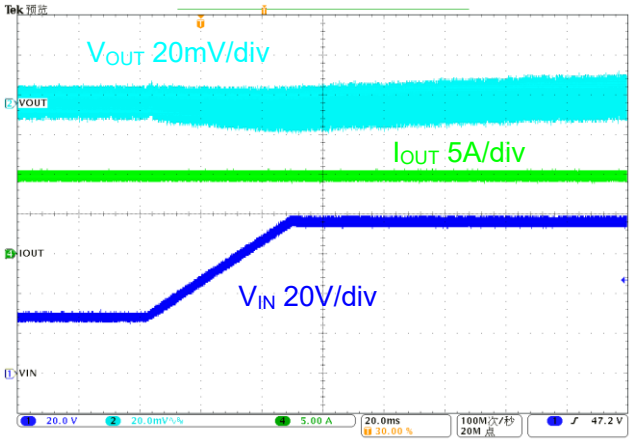
V_{IN}=48V Time(2us/div) V_{OUT}=12V I_{OUT}=0A

Figure 13. Output Ripple (FPWM)



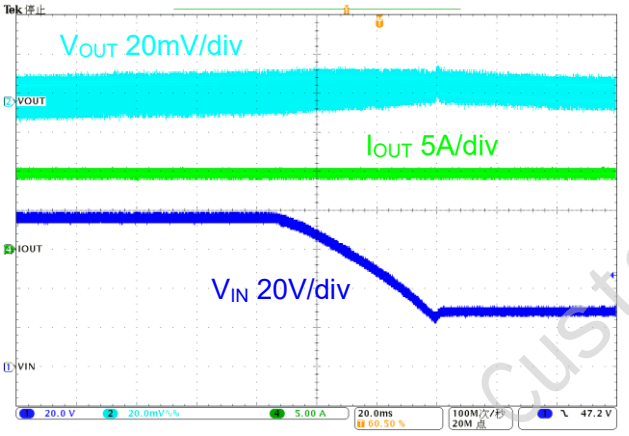
V_{IN}=48V Time(2us/div) V_{OUT}=12V I_{OUT}=10A

Figure 14. Output Ripple



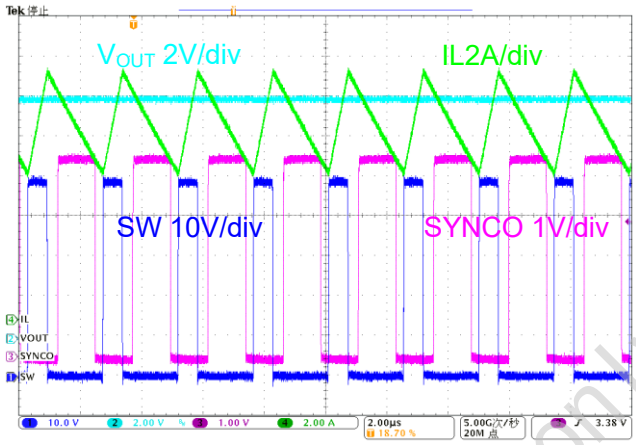
V_{IN}=48V Time(20ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 15. Line Transient Response, 25 V to 75 V



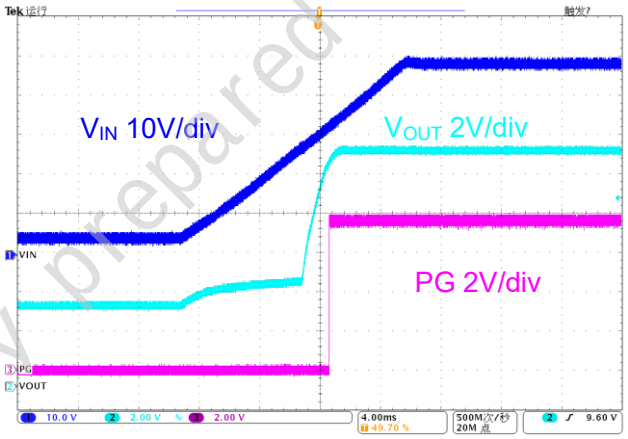
V_{IN}=48V Time(20ms/div) V_{OUT}=12V I_{OUT}=10A

Figure 16. Line Transient Response, 75 V to 25 V



V_{IN}=48V Time(2us/div) V_{OUT}=12V I_{OUT}=10A

Figure 17. SYNCO and SW and IL



V_{IN}=48V Time(4ms/div) V_{OUT}=12V I_{OUT}=0A

Figure 18. Prebias Startup

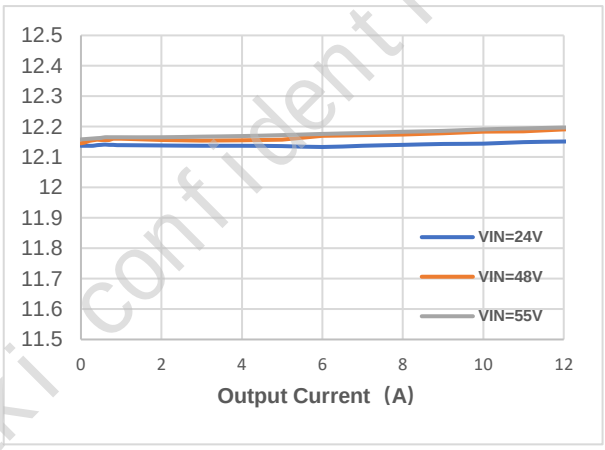


Figure 19. Load and Line Regulation

7.7 Temperature Characteristics

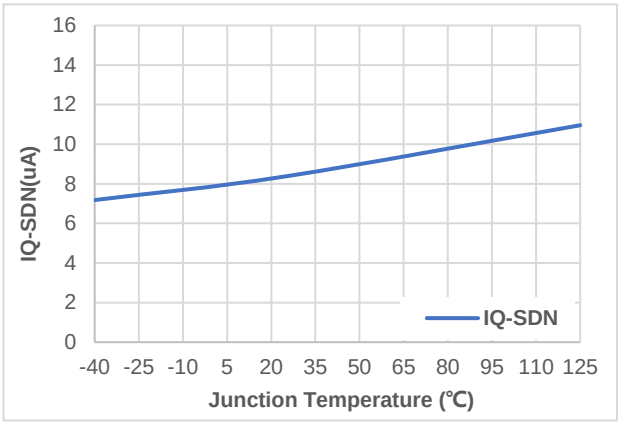


Figure 20. $I_{Q\text{-}SDN}$ vs Junction Temperature

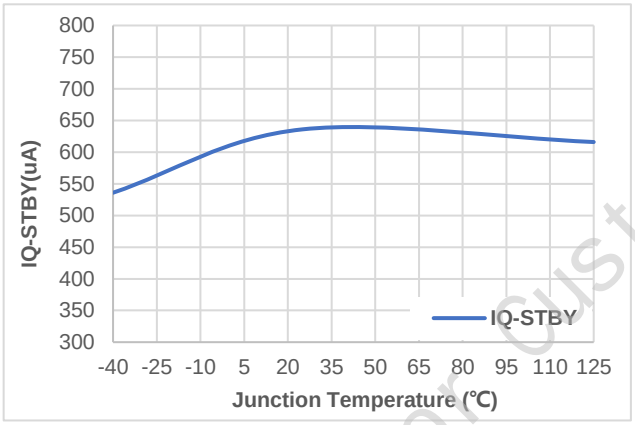


Figure 21. $I_{Q\text{-}STBY}$ vs Junction Temperature

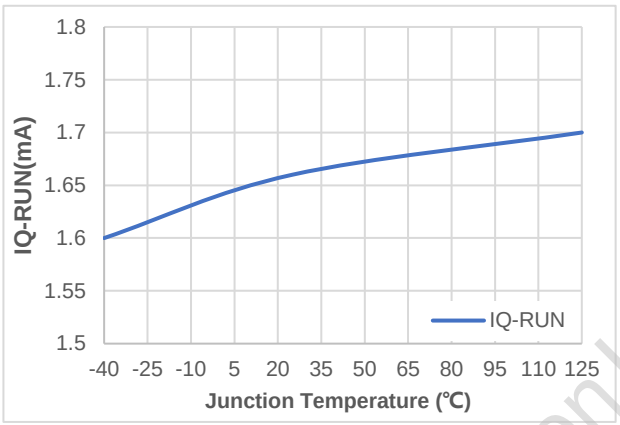


Figure 22. $I_{Q\text{-}RUN}$ vs Junction Temperature

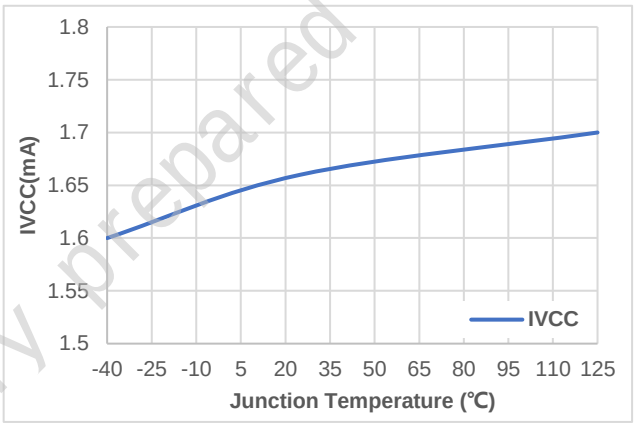


Figure 23. I_{VCC} vs Junction Temperature

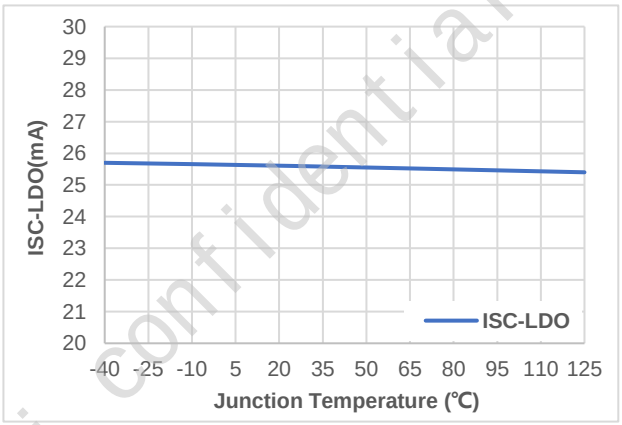


Figure 24. $I_{SC\text{-}LDO}$ vs Junction Temperature

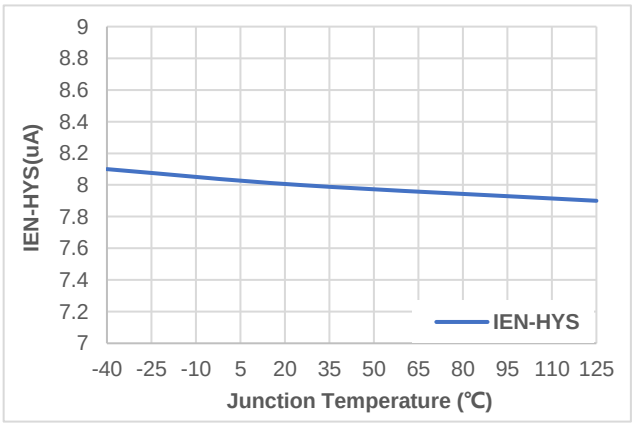


Figure 25. $I_{EN\text{-}HYS}$ vs Junction Temperature

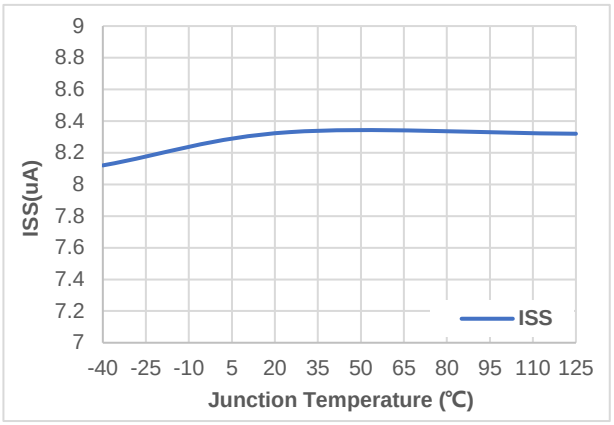


Figure 26. I_{SS} vs Junction Temperature

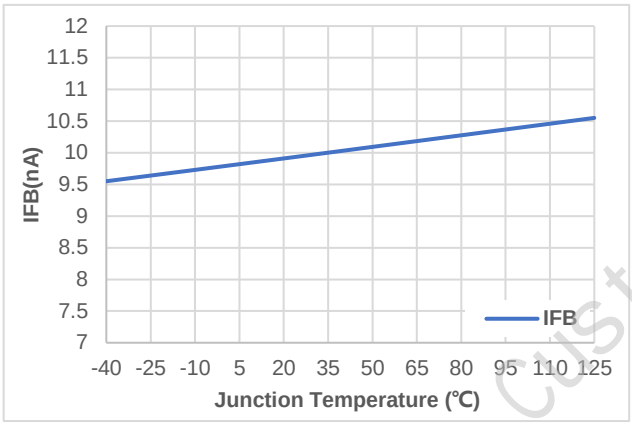


Figure 27. I_{FB} vs Junction Temperature

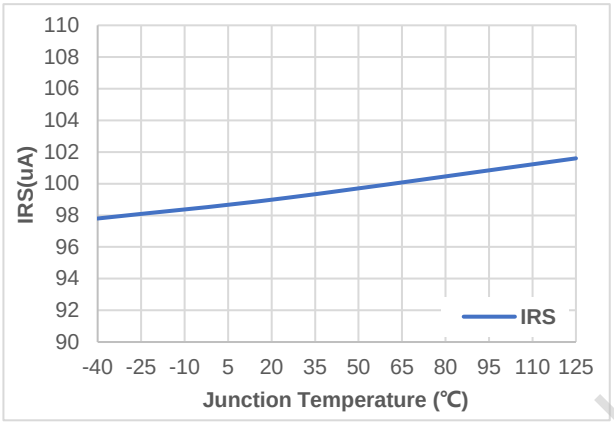


Figure 28. I_{RS} vs Junction Temperature

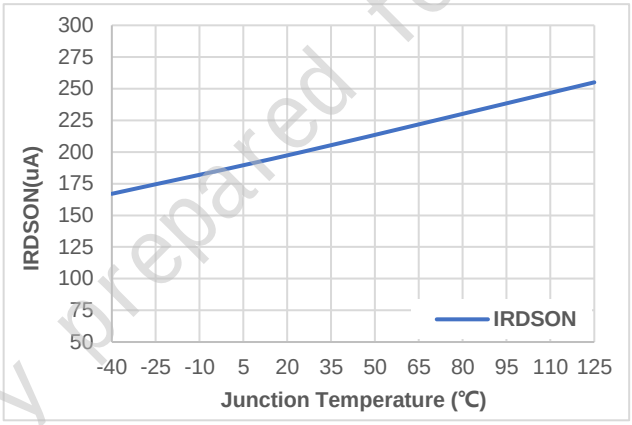


Figure 29. I_{RDSON} vs Junction Temperature

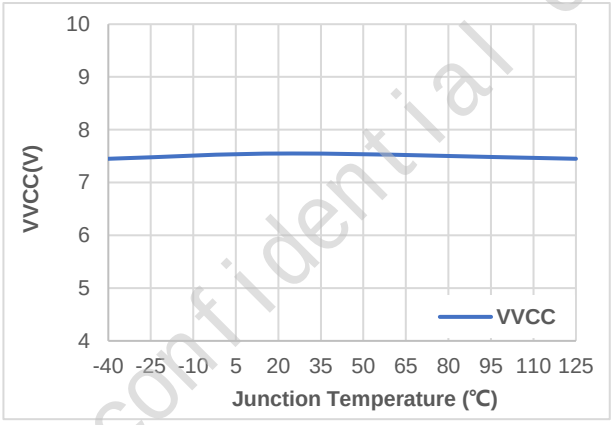


Figure 30. V_{VCC} vs Junction Temperature

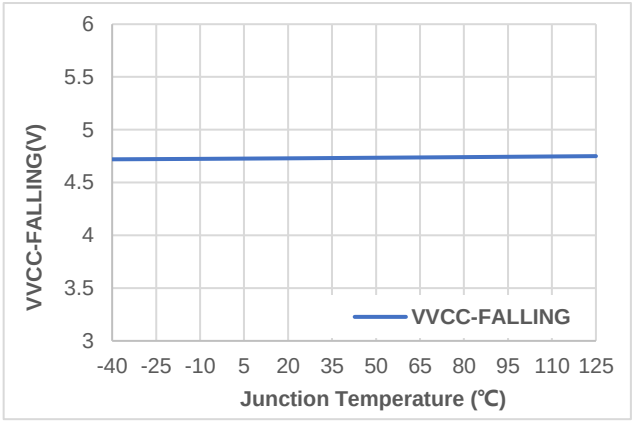


Figure 31. $V_{VCC\text{-}FALLING}$ vs Junction Temperature

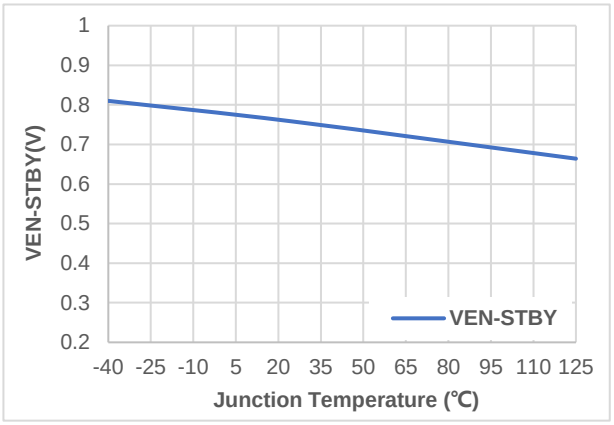


Figure 32. $V_{EN-STBY}$ vs Junction Temperature

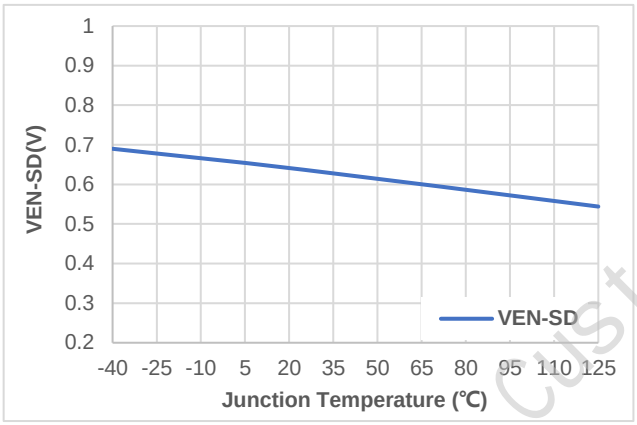


Figure 33. V_{EN-SD} vs Junction Temperature

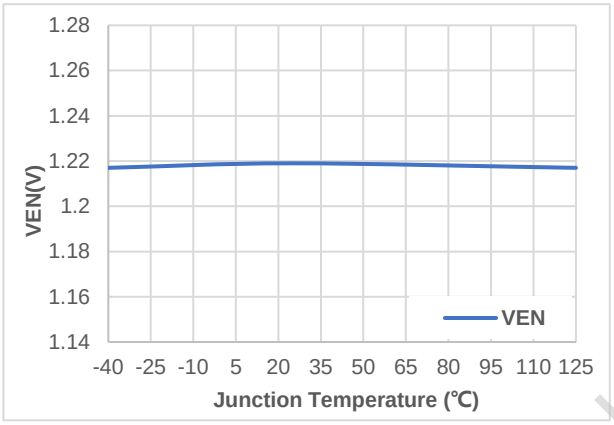


Figure 34. V_{EN} vs Junction Temperature

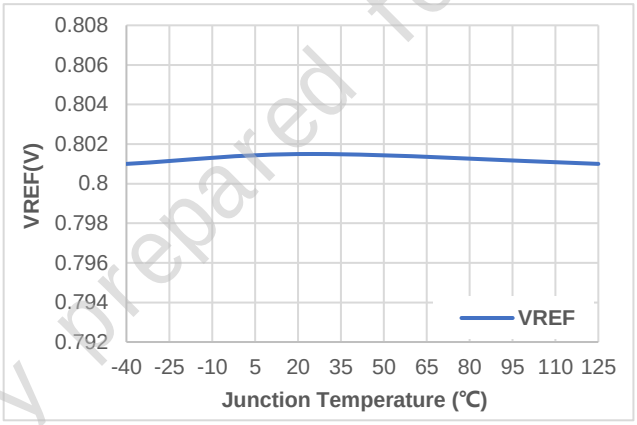


Figure 35. V_{REF} vs Junction Temperature

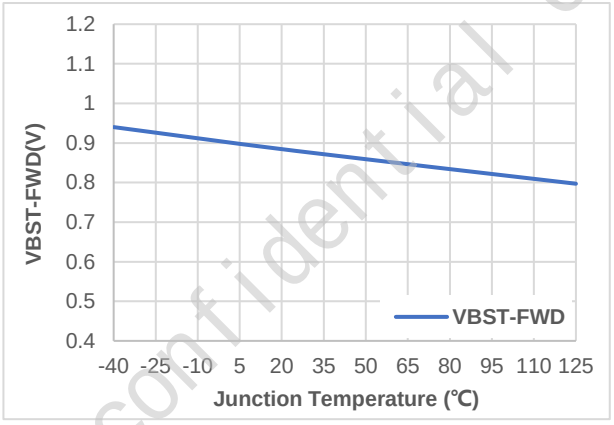


Figure 36. $V_{BST-FWD}$ vs Junction Temperature

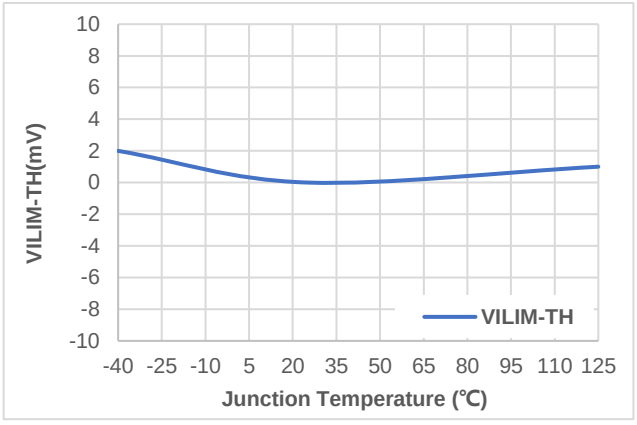


Figure 37. $V_{ILIM-TH}$ vs Junction Temperature

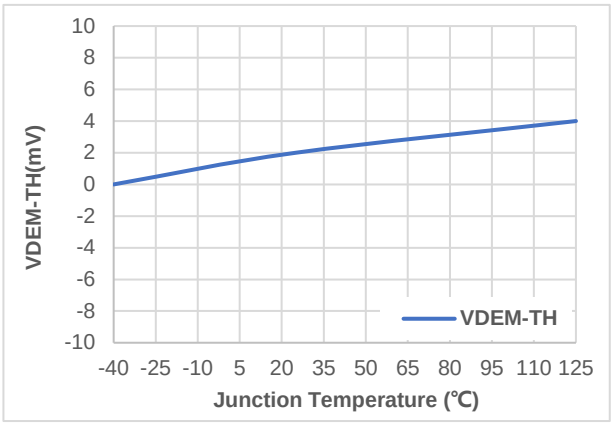


Figure 38. V_{DEM-TH} vs Junction Temperature

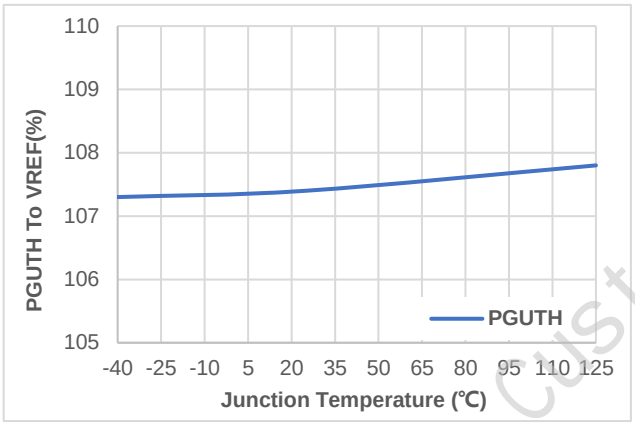


Figure 39. PG_{UTH} vs Junction Temperature

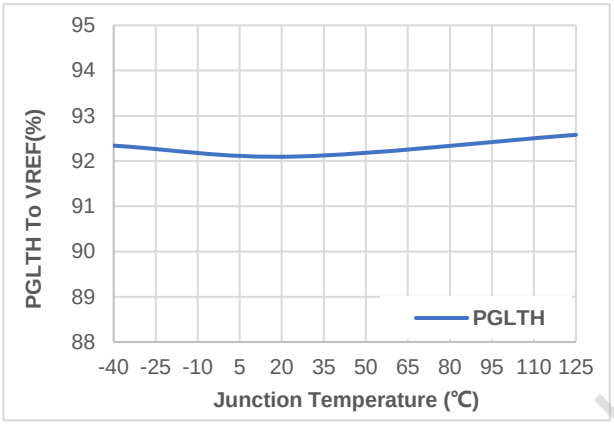


Figure 40. PG_{LTH} vs Junction Temperature

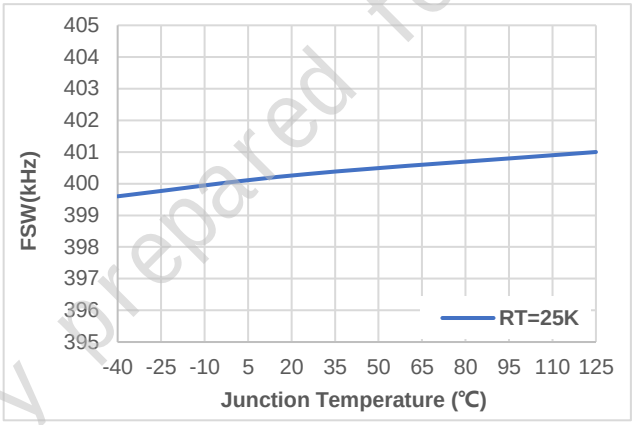


Figure 41. F_{SW} vs Junction Temperature

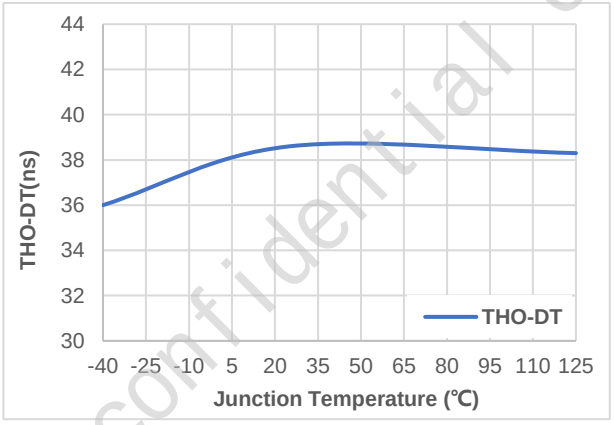


Figure 42. T_{HO-DT} vs Junction Temperature

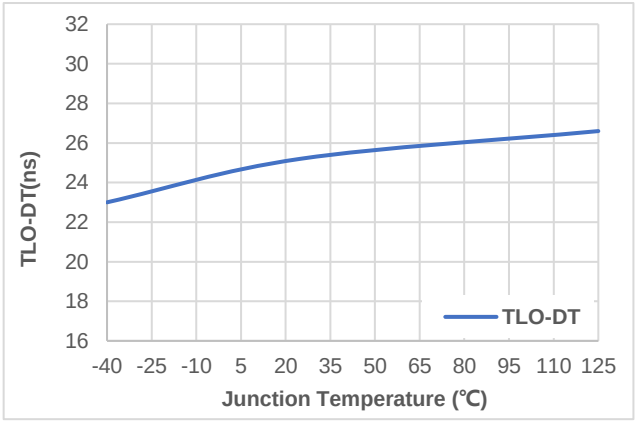


Figure 43. T_{LO-DT} vs Junction Temperature

8. Detailed Description

8.1 Overview

The MK9286 operates over a wide input voltage range from 6V to 85V. With appropriate high-side and low-side MOSFET and inductance, the MK9286 delivers up to 30A output current.

The MK9286 adopts a voltage mode control architecture to achieve excellent accurate voltage output. The switching frequency is adjustable up to 1 MHz, which also can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications.

MK9286 supports Forced-PWM (FPWM) and Diode Emulation Mode; FPWM operation eliminates switching frequency variation to minimize EMI, while useing selectable diode emulation lowers current consumption at light-load condition.

MK9286 offers wide duty cycle from 1% to 98% under appropriate switching frequency, so wide range of input and output voltages can be easily supported.

The MK9286 provides a power good (PG) flag pin to indicate output voltage.

The MK9286 operates with a single power supply input with an internal LDO output (VCC pin). With an external bias power supply applied to VCC, improved total efficiency can be achieved.

8.2 Functional Block Diagram

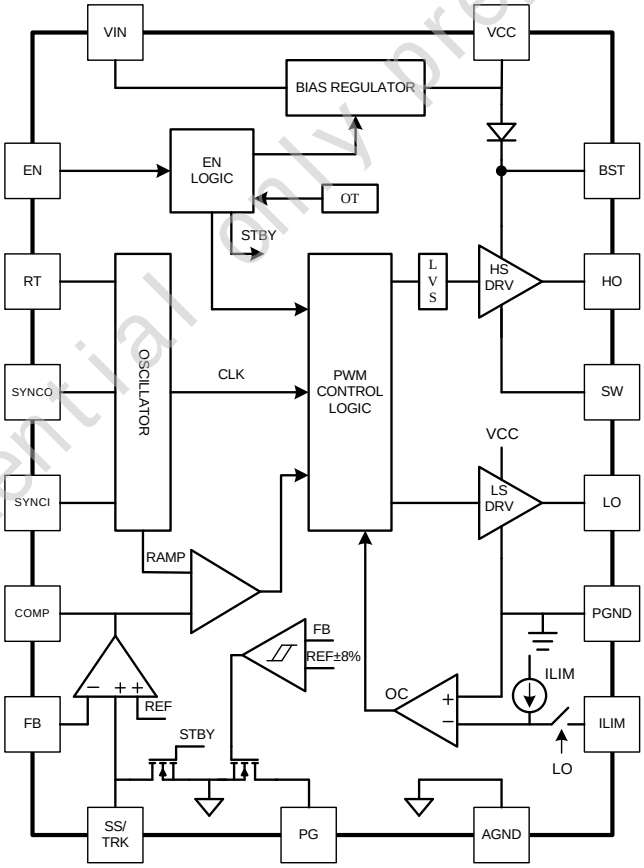


Figure 44 Block Diagram

8.3 Feature Description

8.3.1 Enable (EN)

An external logic signal can be used to turn output ON and OFF for system power up/down sequencing and protection. MK9286 has accurate 1.2V comparator reference to determine EN voltage states, and provides tri-state modes.

VEN＜0.75V,shutdown mode, VIN to VCC LDO shutdown；

0.75V≤VEN＜1.2V,standby mode, VIN to VCC LDO regulated to 7.5V；

VEN＞1.2V,operating mode, start to operating；

EN pin can be directly connected to VIN, which allows self start-up of MK9286 when VCC is within its valid operating range. By connecting this pin to VIN through resistor divider, a programmable UVLO can be achieved to benefit many application requirements. In this case, the UVLO turn-on voltage is calculated as:

$$V_{UVLO} = (1 + \frac{R_{EN-H}}{R_{EN-L}}) \times V_{EN-H}$$

V_{EN-H} is EN rising threshold voltage, typical is 1.2V.

The UVLO hysteresis is accomplished with an internal 8uA current source that is switched on or off into the impedance of the set-point divider. When the voltage at the EN pin exceeds the rising threshold, the current source is activated to quickly raise the voltage at the EN pin. The hysteresis can be calculated as:

$$V_{hys}(\mathrm{V}) = R_{EN-H} \times 8\mathrm{uA}$$

8.3.2 Switching Frequency (RT, SYNCI)

When SYNCI is floating or tied to GND, the switch frequency of MK9286 is set by the frequency resistor RT. As shown below, 24.9kΩ resistor sets the switching frequency at 400kHz.

$$F_{SW}(kHz) = \frac{10^4}{R_T(k\Omega)}$$

When SYNCI is connected to an external clock synchronization signal, the switching frequency is determined by the external clock signal.

Note that the final switching frequency is affected by component tolerance.

Note that the external clock signal frequency must between 0.8× F_{SW} to 1.5× F_{SW}.

8.3.3 Soft Start and Tracking (SS/TRK)

A capacitor from the SS/TRK pin to GND defines the SS/TRK time, T_{SS}. The MK9286 enters into soft-start immediately after EN exceeds its rising threshold of 1.2 V. Tss is set by Css as shown below:

$$T_{SS} = \frac{V_{REF}(0.8V) \times C_{SS}}{I_{SS}(8uA)}$$

If an external voltage source is connected to the SS/TRK pin, the internal 8uA for external soft-start capability of MK9286 is disabled. The regulated output voltage level rises following the external SS/TRK rising slope, before the SS/TRK pin reaches the 0.8V reference voltage level.

8.3.4 Voltage-Mode Control Loop (COMP)

The MK9286 integrates the voltage mode control loop implementation with input voltage feed forward to eliminate the input voltage dependence of the PWM modulator gain. For more detail design application information, refer to MK9286 reference design parameters; For the loop calculation, refer to Section 12.18 Control Loop Compensation.

8.3.5 Feed Back (FB)

Feedback input, which connects to the negative input of internal Error Amplifier (EA), is used to program the output voltage by choosing appropriate R_{F1} and R_{F2}. For targeted V_{OUT} setpoint, calculate R_{F1} and R_{F2} using below equation:

$$V_{OUT} = 0.8\text{V} \times (1 + \frac{R_{F2}}{R_{F1}})$$

R_{F1} in the range of 2kΩ to 5kΩ is recommended for most applications. Larger feedback resistance consumes less DC current, which is important if light-load efficiency is critical. But too large of resistance is not recommended as the feedback path would become more susceptible.

The feedforward capacitor C_{FF} is strongly recommended, which can improve the system stability and transient responses.

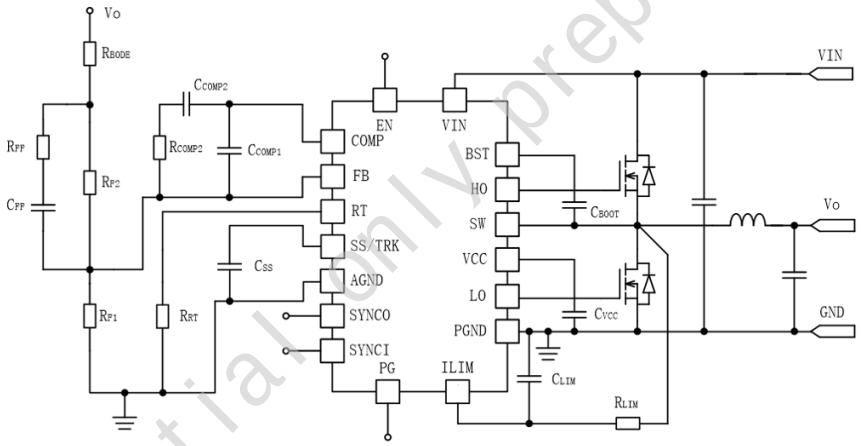


Figure 45. FB Connection

8.3.6 Clock Synchronization and Diode Emulation Mode (SYNCI,SYNCO)

There are 3 functions for SYNCI pin.

When SYNCI is floating or tied to GND, MK9286 works in diodes emulation mode, and its switching frequency is set by the frequency resistor connected at RT pin.

When SYNCI is connected to an external synchronization clock, MK9286 works in FPWM mode, and its switching frequency is determined by the external clock.

When SYNCI is connected to VCC, MK9286 works in FPWM mode, and its switching frequency is set by the frequency resistor connected at RT pin

SYNCO is an output pin, which is nearly delayed 180° of the HO pin.

8.3.7 Power Good (PG)

MK9286 provides a Power Good (PG) flag pin to indicate whether the output voltage is within the regulation range. PG is an open-drain output that requires a pullup resistor to a DC source which voltage is less than 14V (If necessary, use a resistor divider to decrease the voltage from a higher pullup voltage rail). The typical range of pullup resistance is about 10kΩ to 100 kΩ. When the FB voltage exceeds 95% of the reference, the internal switch will be turned off and PG can be pulled high by the pullup resistor. If the FB voltage falls below 92% of the reference or rises above 108% of the reference, the switch will be turned on and PG is pulled low to indicate the output voltage is out of regulation. The function of PG is to set start-up sequencing of downstream converters, fault protection, and output monitoring.

8.3.8 Current Sensing and OCP (ILIM)

The MK9286 use the negative drop across the low-side FET or current sense resistor at the end of the "OFF" time to measure the inductor current. Allowing for 30% over minimum current limit for transient recovery and 20% rise in RDS(on)-LS for self-heating of the MOSFET, the voltage drop across the low-side FET at current limit and application diagram is given by below:

$$R_{LIM} = \frac{I_o - \Delta I_L/2}{I_{RDS(on)-LS}} \times R_{DS(on)-LS}$$

Meraki recommends setting the OCP current at 1.8 times the rated output current.

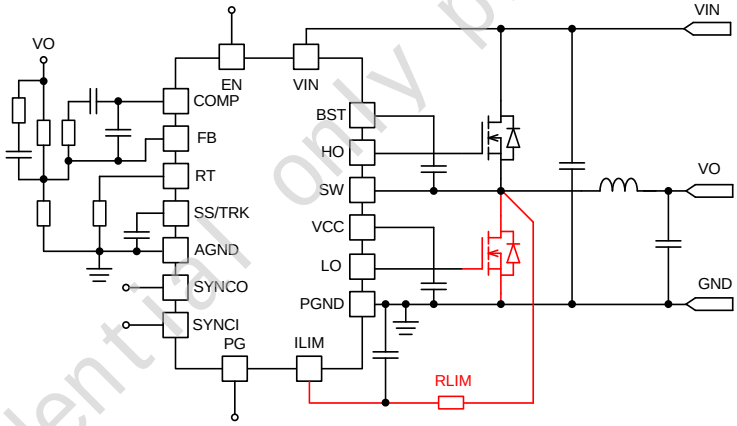


Figure 46. Low-side FET Current Sense

When use current sense resistor, the voltage drop across the current sense resistor at current limit and application diagram is given by below:

$$R_{LIM} = \frac{I_o - \Delta I_L/2}{I_{RS}} \times R_{RS}$$

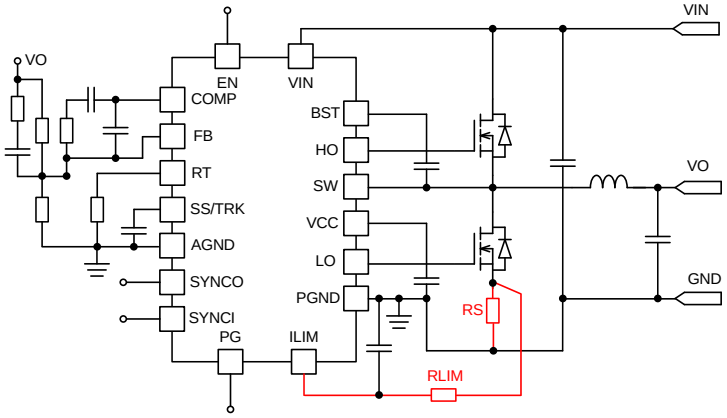


Figure 47. RS Current Sense

8.3.9 Gate Drivers (LO, HO)

The MK9286 provides high drive capability up to 2.5A/3.5A. By selecting suitable Rg to reduce switching speed, better EMI performance is achieved.

8.3.10 High-Voltage Bias Supply Regulator (VCC)

MK9286 supports 85V high-voltage input. VCC is the high voltage LDO output pin, and the output voltage of LDO is 7.5V. Connect a ceramic decoupling capacitor from 1uF to 5uF as close as possible to the VCC and AGND pins of MK9286 for stability.

When the output voltage of the whole application is between 8.5V to 14V, or the system board has an 8.5V to 14V voltage rail, the voltage can be connected to VCC through diodes instead of using the internal high-voltage LDO, which can reduce power loss of internal high voltage LDO. This is very helpful for reducing chip loss and heat generation, especially in scenarios where the input bus voltage is high, such as applications with an input greater than 60V. An application diagram is given below:

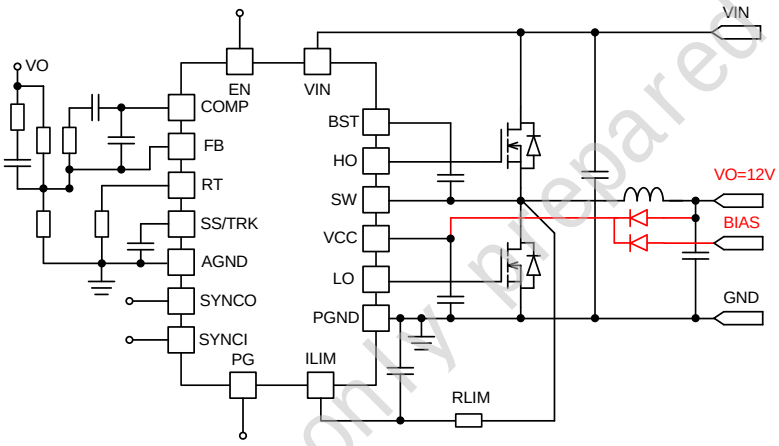


Figure 48. External VCC Supply

Note that if BIAS voltage is used to provide VCC supply, VIN also needs to connect to VIN-BUS to offer startup voltage and current.

Note that if BIAS voltage is used to provide VCC supply and VIN voltage is less than the BIAS voltage, an extra diode is needed to connect VIN and VIN-BUS as shown below:

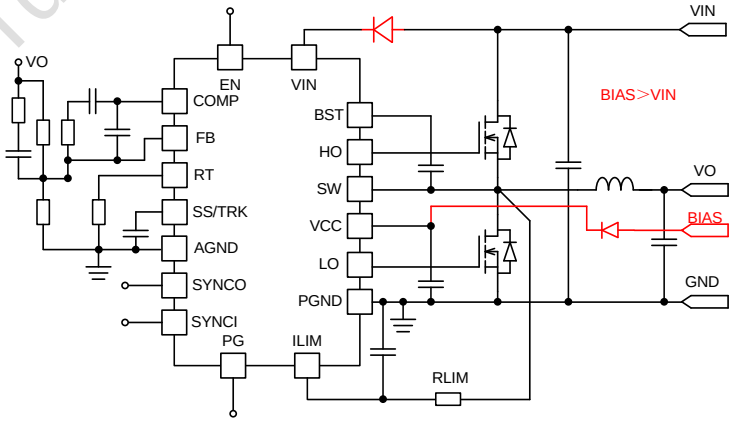


Figure 49. BIAS VCC Supply(BIAS＞VIN)

8.3.11 Boot-strap and Switching Node (BST, SW)

A high-quality COG 100nF ceramic capacitor connected between the BST pin and the SW pin is recommended, which provides the energy for a high-side gate driver Also, a RC series net can be used for slowing down the turn-on speed of the high side MOSFET.

8.3.12 Over Temperature Protection

MK9286 supports OTP (over temperature protection). The threshold of thermal shutdown is about 175°C with 20°C hysteresis. The OTP is a non-latching protection.

8.3.13 High-Voltage Input (V_{IN}) and Input Capacitor (C_{IN})

MK9286 supports 85V high-voltage input, which is also the input pin for high voltage LDO. VIN is also used to provide PWM feedforward Gain (V_{IN}/VRAMP), so VIN must be connected to VIN-BUS.
An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck converter at every switching cycle. The input ripple voltage ΔV_{IN} at the input capacitor is calculated as:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR}$$

The capacitance of the input capacitor is calculated as:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1-D)}{F_{SW} \times (\Delta V_{IN} - I_{OUT} \times R_{ESR})}$$

To minimize the potential noise problem, an X7R or better grade capacitor with a sufficient voltage rating is recommended. This capacitor should be close to the VIN and GND pins to minimize the loop area formed by C_{IN} and VIN/GND pins. In this application, a 0.1uF low ESR ceramic capacitor is recommended.

8.3.14 Output Inductor (L)

It is recommended to choose the ripple current of an inductor that is 30% to 50% of the rated load current I_{OUT} (max) for most applications. The inductance is calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The peak current of inductor is calculated as:

$$I_L(\text{peak}) = I_{OUT}(max) + \frac{\Delta I_L}{2}$$

The saturation current rating of the inductor must be greater than I_L (peak). An inductor which saturation current is above the current limit setting of the MK9286 will be the best choice. Note that the inductor saturation current levels generally decrease as the inductor temperature increases.

8.3.15 Output Capacitor (Cout)

The output capacitor limits the capacitive voltage ripple at the converter output. This voltage ripple is generated from the triangular inductor current ripple flowing into and out of the capacitor and can be calculated as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times F_{SW} \times C_{OUT}}$$

The above equation only takes the steady state ripple into consideration. The transient requirements also must be taken into consideration when selecting the output capacitor. The X7R or a better grade ceramic capacitor larger than 220uF is recommended.

8.3.16 Control Loop Compensation

The MK9286 integrates the voltage mode control loop implementation and feeds the input voltage forward to eliminate the dependence of the input voltage on the PWM modulator gain. The voltage mode buck control loop is shown below:

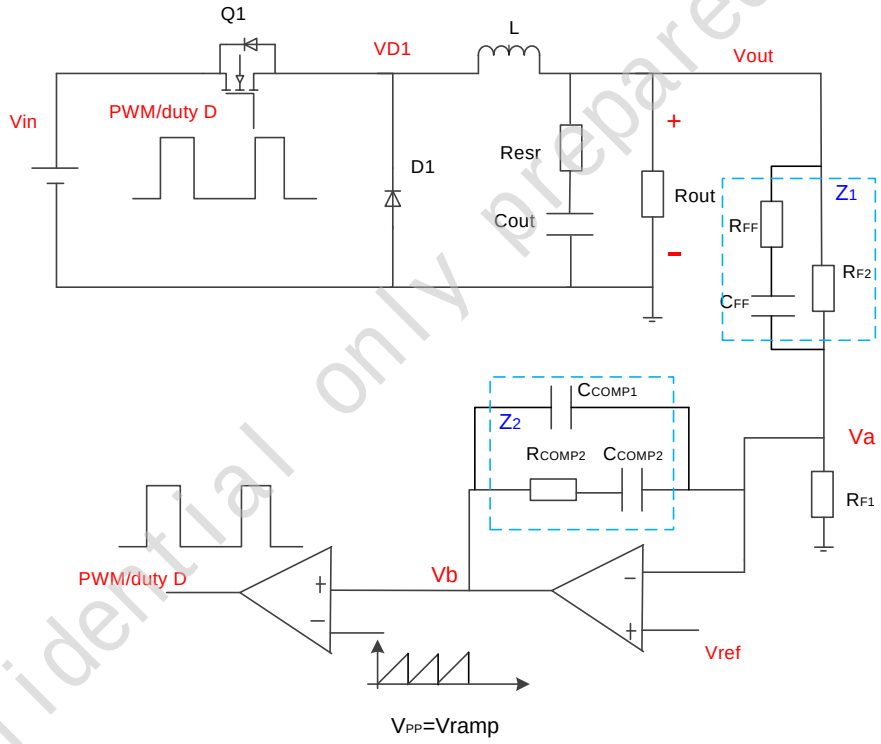


Figure 50. Buck Circuit Voltage Loop Control Diagram

Figure 27 is the equivalent control block diagram, where kf(s) and Gv(s) are the transfer functions of the regulator, kd is the transfer function from the regulator output to the duty cycle D, Kpwm is the transfer function from the duty cycle D to the diode voltage VD1, andG1(s) is the transfer function from VD1 to the output voltage.

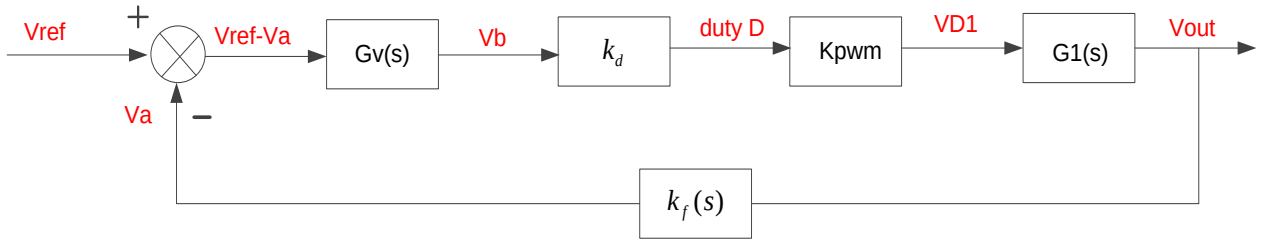


Figure 51. Buck Equivalent Control Block Diagram

Step1、Calculate $k_f(s) \times G_v(s)$

$$\begin{cases} V_a = \dfrac{R_{F1}}{R_{F1}+Z_1}V_{out} \Rightarrow V_{ref}-V_a = V_{ref} - \dfrac{R_{F1}}{R_{F1}+Z_1}V_{out} = \dfrac{(R_{F1}+Z_1)V_{ref} - R_{F1}V_{out}}{R_{F1}+Z_1} \\ \dfrac{V_{out}-V_{ref}}{Z_1} = \dfrac{V_{ref}}{R_{F1}} + \dfrac{V_{ref}-V_b}{Z_2} \Rightarrow \dfrac{(Z_1+R_{F1})V_{ref} - R_{F1}V_{out}}{Z_1 R_{F1}} = \dfrac{-V_{ref}+V_b}{Z_2} \end{cases}$$

then

$$\begin{cases} G_v(s) = \dfrac{V_b}{(V_{ref}-V_a)} = \dfrac{Z_2 \times (Z_1+R_{F1})}{Z_1 R_{F1}} \\ k_f(s) = \dfrac{R_{F1}}{Z_1+R_{F1}} \end{cases}$$

To get the loop compensation function result:

$$k_f(s) \times G_v(s) = \frac{Z_2}{Z_1}$$

Step2、Calculate K_d

The regulator output voltage Vb is compared with the sawtooth wave of amplitude Vramp to get the duty cycle D, and the transfer function of this link is Kd.

$$k_d = \frac{D}{V_b} = \frac{1}{V_{ramp}}$$

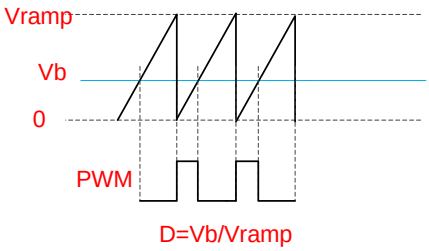


Figure 52. V_{RAMP} Wave

Step3、Calculate Kpwm

The PWM signal is applied to the switch Q1

0~DT period (T is the switching period): Q1 is turned on, and the voltage across the diode D1 is Vin;

During DT~T: Q1 is off, the inductor current flows through D1, and the voltage across the diode D1 is 0.

Therefore, the average value of the voltage across the diode D1 is DVin.

$$k_{pwm} = \frac{V_{D1}}{D} = \frac{DV_{in}}{D} = V_{in}$$

Step4、Calculate G1(s):

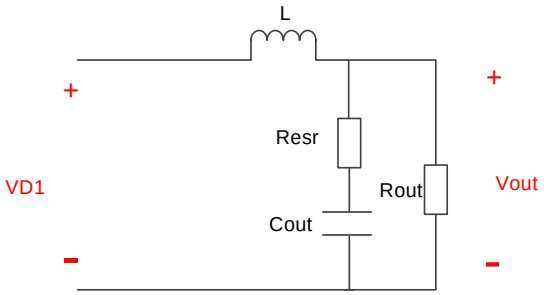


Figure 53. Vout Vs V_{D1}

$$G_1(s) = \frac{V_{out}(s)}{V_{D1}(s)} = \frac{1 + R_{esr}C_{out}s}{\frac{L * R_{out}C_{out} + L * R_{esr}C_{out}}{R_{out}}s^2 + \frac{L + R_{out}R_{esr}C_{out}}{R_{out}}s + 1}$$

Resr<<Rout, to further simplify the transfer function,

$$G_1(s) = \frac{V_{out}(s)}{V_{D1}(s)} = \frac{1 + R_{esr}C_{out}s}{L * C_{out}s^2 + \frac{L}{R_{out}}s + 1}$$

The transfer function has a zero and a double pole.

Zero frequency:

$$f_{ESR} = \frac{1}{2\pi \times R_{esr}C_{out}}$$

Double pole frequency:

$$f_{LC} = \frac{1}{2\pi\sqrt{L * C_{out}}}$$

Step5、Regulator parameter design

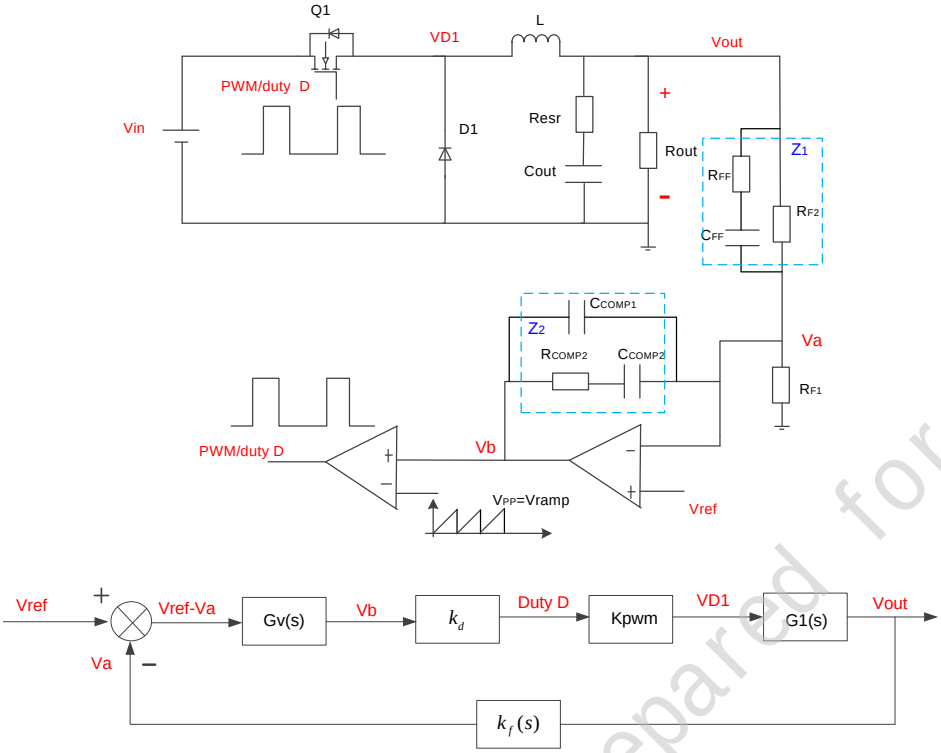


Figure 54. Control Loop and Equivalent Control Block

To obtain the open-loop transfer function of the system：

$$G_o(s) = k_f(s) \times G_v(s) \times k_d \times k_{pwm} \times G_1(s)$$

$$G_o(s) = \frac{Z_2(s)}{Z_1(s)} \times \frac{k_{pwm}}{V_{ramp}} \times \frac{1 + R_{esr}C_{out}s}{L * C_{out}s^2 + \frac{L}{R_{out}}s + 1}$$

$$\frac{Z_2(s)}{Z_1(s)} = \frac{1}{sR_{F2}(C_{COMP2} + C_{COMP1})} \times \frac{(R_{COMP2}C_{COMP2}s + 1)((R_{F2} + R_{FF})C_{FF}s + 1)}{(\frac{R_{COMP2}C_{COMP2}C_{COMP1}}{C_{COMP2} + C_{COMP1}}s + 1)(R_{FF}C_{FF}s + 1)}$$

In order to simplify the regulator transfer function design process, when designing regulator parameters, take C_{COMP2}>>C_{COMP1}. Then,

$$\frac{Z_2(s)}{Z_1(s)} = \frac{1}{sR_{F2}C_{COMP2}} \times \frac{(R_{COMP2}C_{COMP2}s + 1)((R_{F2} + R_{FF})C_{FF}s + 1)}{(R_{COMP2}C_{COMP1}s + 1)(R_{FF}C_{FF}s + 1)}$$

The regulator has two poles:

$$f_{p1} = \frac{1}{2\pi \times R_{FF}C_{FF}}, f_{p2} = \frac{1}{2\pi \times R_{COMP2}C_{COMP1}}$$

Two zeros:

$$f_{z1} = \frac{1}{2\pi \times R_{COMP2}C_{COMP2}}, f_{z2} = \frac{1}{2\pi \times (R_{F2} + R_{FF})C_{FF}}$$

The two poles and two zeros are shown as below：

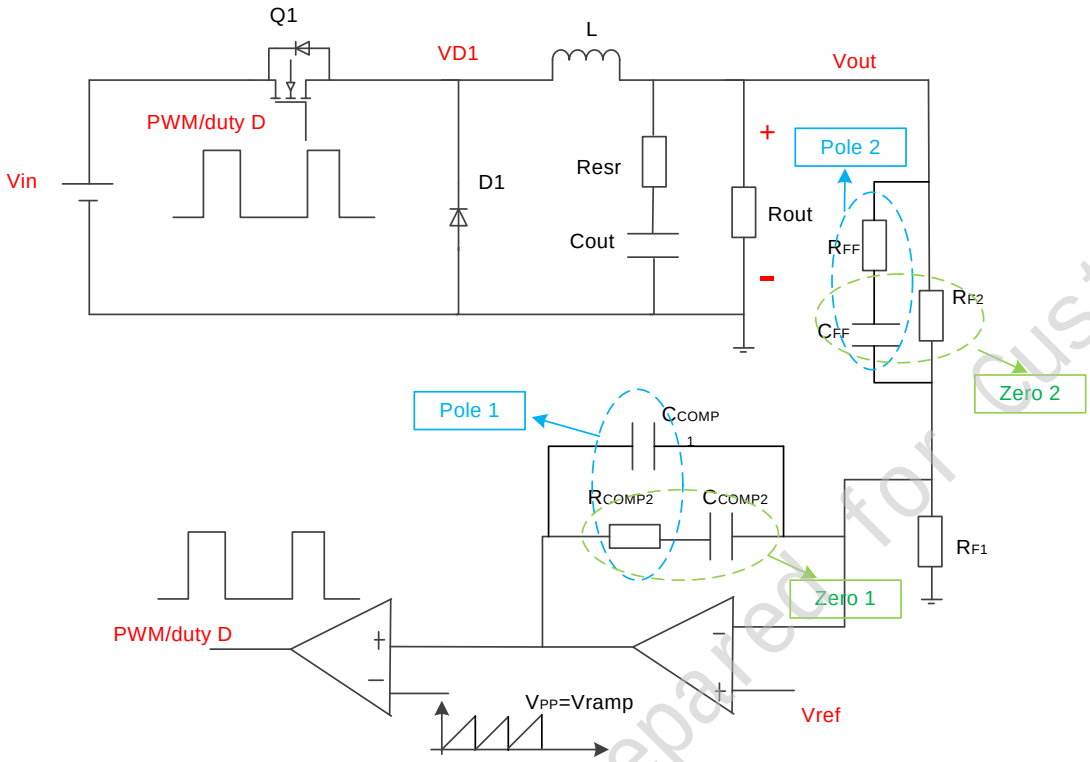


Figure 55. Control Loop With Poles and Zeros

And the final open loop transfer function：

$$G_o(s) = \frac{1}{sR_{F2}C_{COMP2}} \times \frac{(R_{COMP2}C_{COMP2}s+1)((R_{F2}+R_{FF})C_{FF}s+1)}{(R_{COMP2}C_{COMP1}s+1)(R_{FF}C_{FF}s+1)} \times \frac{V_{in}}{V_{ramp}} \times \frac{1+R_{esr}C_{out}s}{L*C_{out}s^2+\frac{L}{R_{out}}s+1}$$

$$= \frac{V_{in}}{V_{ramp}} \times \frac{1}{R_{F2}C_{COMP2}} \times \frac{1}{s} \times \frac{(R_{COMP2}C_{COMP2}s+1)((R_{F2}+R_{FF})C_{FF}s+1)}{(R_2C_3s+1)(R_3C_2s+1)} \times \frac{1+R_{esr}C_{out}s}{L*C_{out}s^2+\frac{L}{R_{out}}s+1}$$

Step6、Calculate compensation component parameters：

The crossover frequency of the open loop gain is set to 1/5~1/10 of the switching frequency；

$f_c = (\frac{1}{10}\sim\frac{1}{5})f_{sw}$ f_c is crossover frequency, f_{sw} is switching frequency；

$\frac{V_{in}}{V_{ramp}} \times \frac{1}{R_{F2}C_{COMP2}} \times \frac{1}{k_1} = 2\pi f_c (f_{LC} << f_c$,get $k_1)$

Usually，RF2 and RF1 can be set first according to Vout, so

$$C_{COMP2} = \frac{V_{in}}{V_{ramp}\times\pi f_c \times R_{F2}\times 2k_1} \quad ①$$

The first pole is equal to the zero caused by the out capacitor esr：

$$f_{p1} = \frac{1}{2\pi\times R_{FF}C_{FF}} = f_{esr} = \frac{1}{2\pi\times R_{esr}C_{out}} \quad ②$$

The second pole is equal to half of the switching frequency：

$$f_{p2} = \frac{1}{2\pi \times R_{COMP2} C_{COMP1}} = f_{p2} = \frac{1}{2} f_{sw} \quad ③$$

Two zero points of the regulator (f_{Z1}: compensate the first zero point, f_{Z2}: compensate the second zero point)

$$f_{z1} = \frac{1}{2\pi \times R_{COMP2} C_{COMP2}} = k_1 f_{LC} \ \ (k_1 = 0.5 \sim 1) \quad ④$$

$$f_{Z2} = \frac{1}{2\pi \times (R_{F2} + R_{FF}) C_{FF}} = f_{LC} \quad ⑤$$

By the formula ①－⑤,Calculate the compensation component parameters：

$$C_{COMP2} = \frac{V_{IN}}{V_{ramp} \times \pi f_c \times R_{F2} \times 2k_1}$$

$$R_{COMP2} = \frac{V_{ramp}}{V_{IN}} \frac{f_c}{f_{LC}} R_{F2}$$

$$C_{COMP1} = \frac{1}{\pi \times R_{COMP2} \times f_{sw}}$$

$$R_{FF} = \frac{f_{LC}}{f_{esr} - f_{LC}} R_{F2}$$

$$C_{FF} = \frac{1}{2\pi \times f_{esr} \times R_{FF}}$$

For example：

V_{in}=6.5-85V,Vout=5V,Iout=0-20A,Fsw=230kHz,V_{in}/V_{RAMP}=18,
L=3.3uH,Cout=549uF,ESR=3mΩ,R_{F2}=23.2kΩ,R_{F1}=4.42kΩ。

$$f_{LC} = \frac{1}{2\pi\sqrt{L * C_{out}}} = 3.74kHz$$

$$f_{ESR} = \frac{1}{2\pi \times R_{esr} C_{out}} = 97kHz$$

$$f_c = \frac{1}{8.6} f_{sw} = 27\text{kHz} \quad (f_c \ is \ usually \ (\frac{1}{10} \sim \frac{1}{5}) \ of \ f_{sw}$$

$$C_{COMP2} = \frac{V_{in}}{V_{ramp} \times \pi \times f_c \times R_{F2} \times 2k_1} = 5.7nF (k_1=0.8)$$

$$R_{COMP2} = \frac{V_{ramp}}{V_{in}} \frac{f_c}{f_{LC}} R_{F2} = 9.3k$$

$$C_{COMP1} = \frac{1}{\pi \times R_{COMP2} \times f_{sw}} = 149pF$$

$$R_{FF} = \frac{f_{LC}}{f_{esr} - f_{LC}} R_{F2} = 930$$

$$C_{FF} = \frac{1}{2\pi \times f_{esr} \times R_{FF}} = 1.6nF$$

9. Application and Implementation

9.1 Reference Design 1

V_{in}=6.5-80V

Vout=5V

Iout=0-20A

Fsw=230kHz

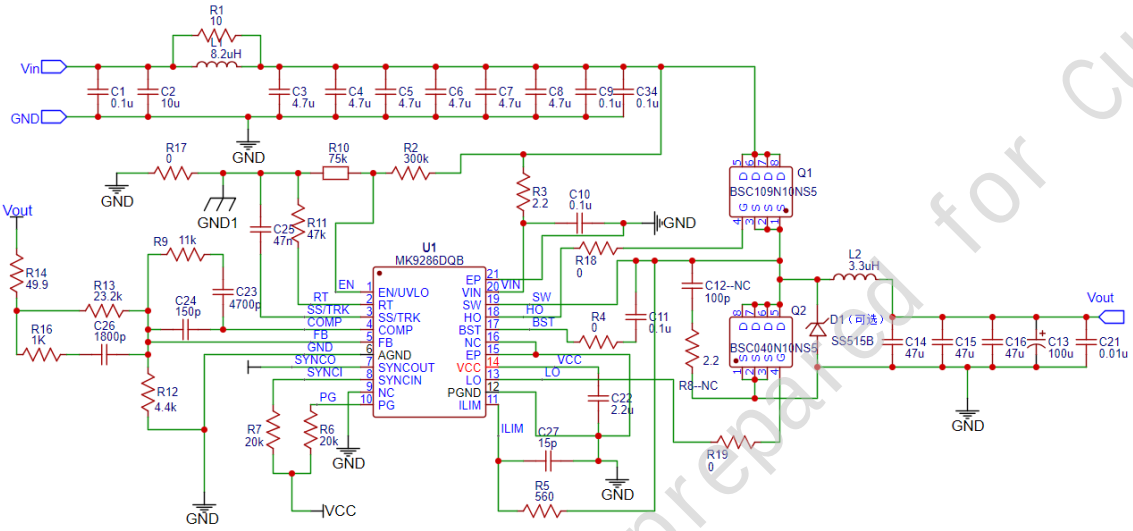


Figure 56. Reference Design 1

9.2 Reference Design 2

Vin=15-80V

Vout=12V

Iout=0-12A

Fsw=400kHz

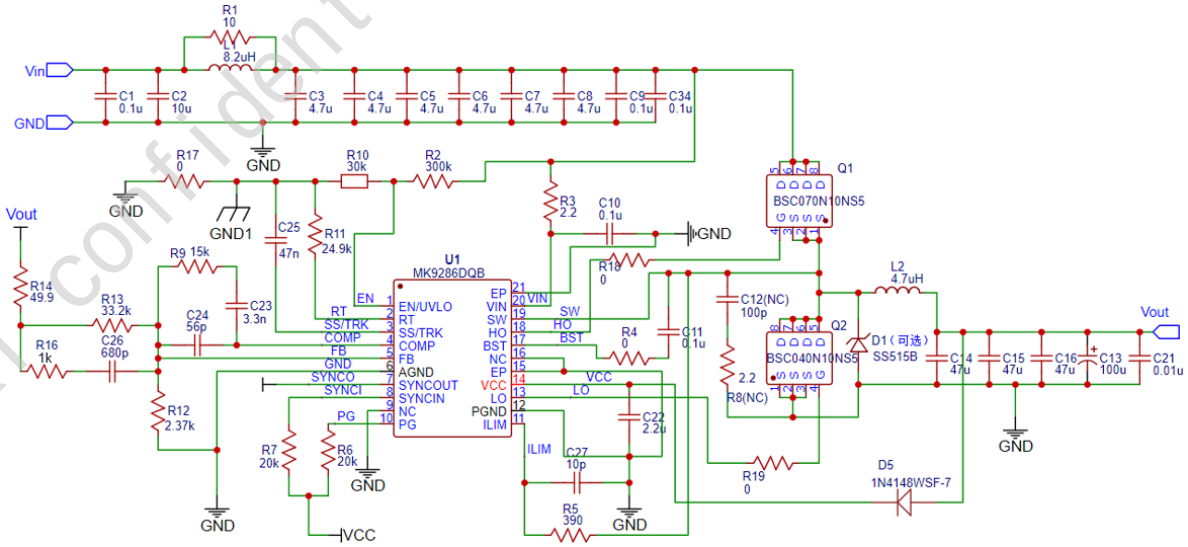


Figure 57. Reference Design 2

9.3 Reference Design 3

Vin=28-80V
Vout=24V
Iout=0-6A
Fsw=400kHz

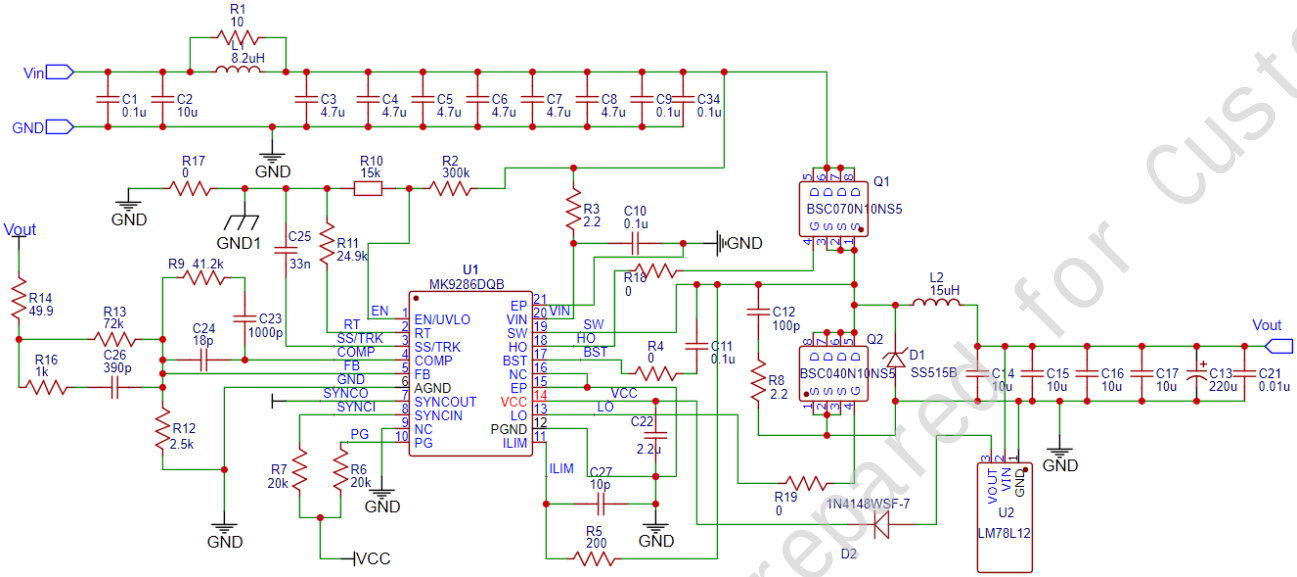


Figure 58. Reference Design 3

10. Power Supply Recommendations

11. Layout

11.1 Layout Guidelines

To achieve high performance of the MK9286, the following layout tips must be followed:

- At least one low-ESR ceramic bypass capacitor VCC must be used. Place the capacitor as close as possible to the MK9286 VCC and GND pins.
- Minimize the loop area formed by C_{IN} connections to VIN and GND pins, refer to Figure 59.
- Inductor must be placed close to the SW pin. Minimize the area of SW trace to avoid the potential noise problem.
- Maximize the PCB area connecting the GND pin and thermal pad. If it is allowed, a ground plane can be used as noise shielding and heat dissipation path.
- Place the feedback resistors, R_{f1} and R_{f2}, close to the FB pin. Route the feedback V_{OUT} sense path away from noisy nodes such as the SW net.
- The RT pin is sensitive to noise. The frequency set resistor R_T must be close to the device.
- BST capacitor to high-side MOS gate path width is better to be wider than 15mil (demo is 20mil);
- VCC capacitor to low-side MOS gate path width is better to be wider than 15mil (demo is 20mil), it recommended that 2 vias placed near to VCC capacitor GND to reduce driver path resistance.

11.2 Layout Example

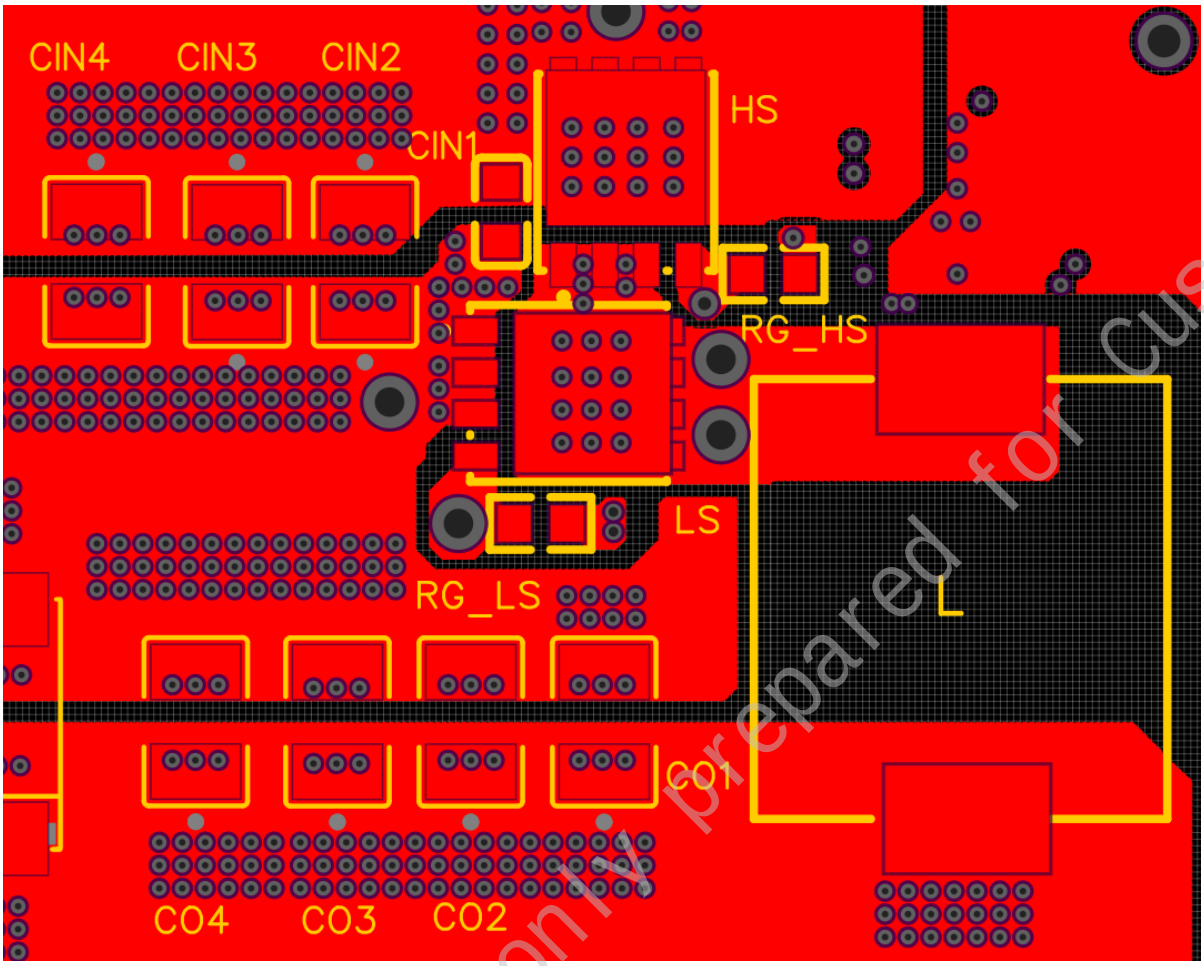


Figure 59 MK9286 Power Loop Layout Example

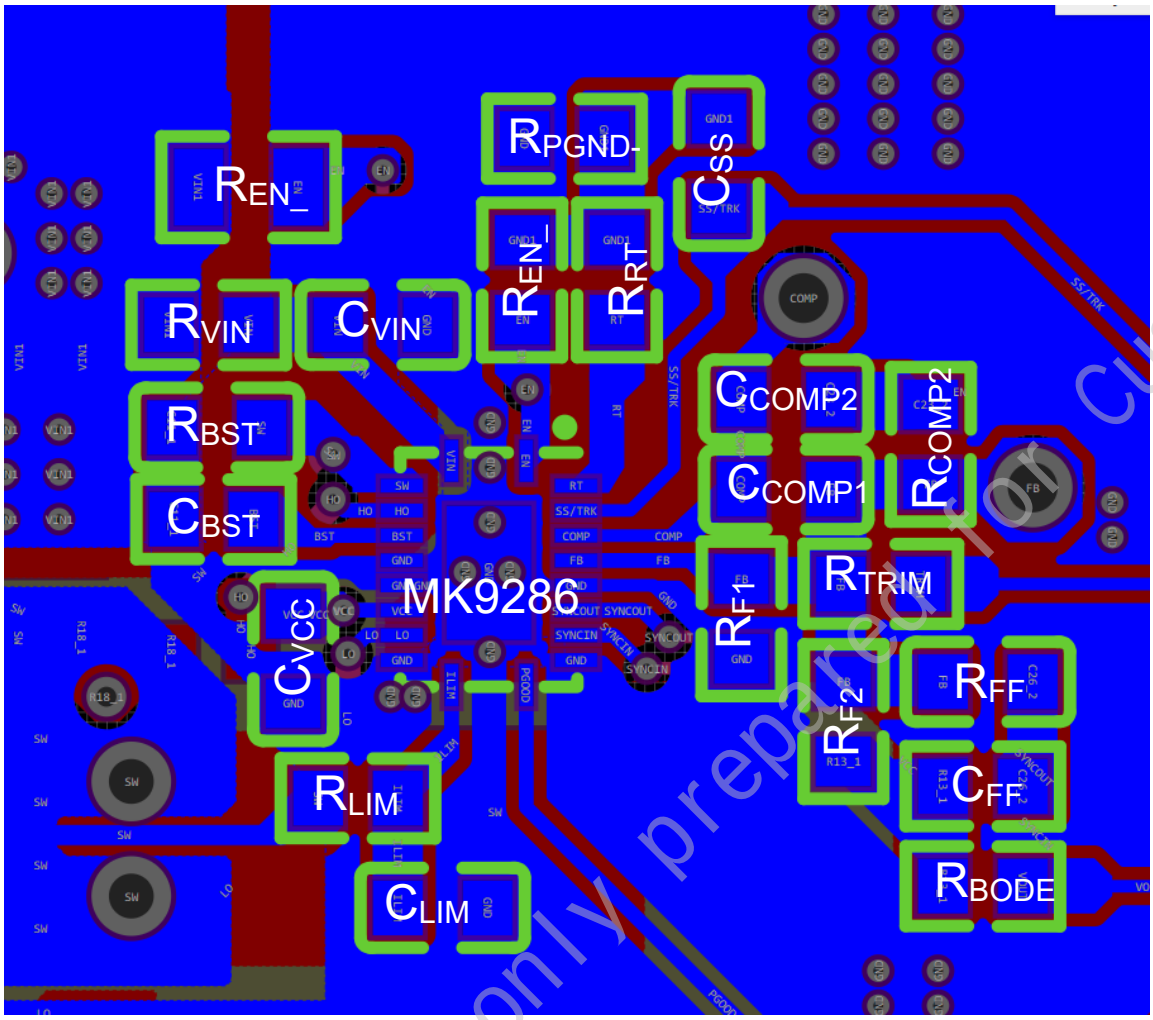


Figure 60 MK9286 Controller Loop Layout Example

12. Mechanical, Packaging

12.1 Package Size

12.1.1 MK9286DQB Package Size

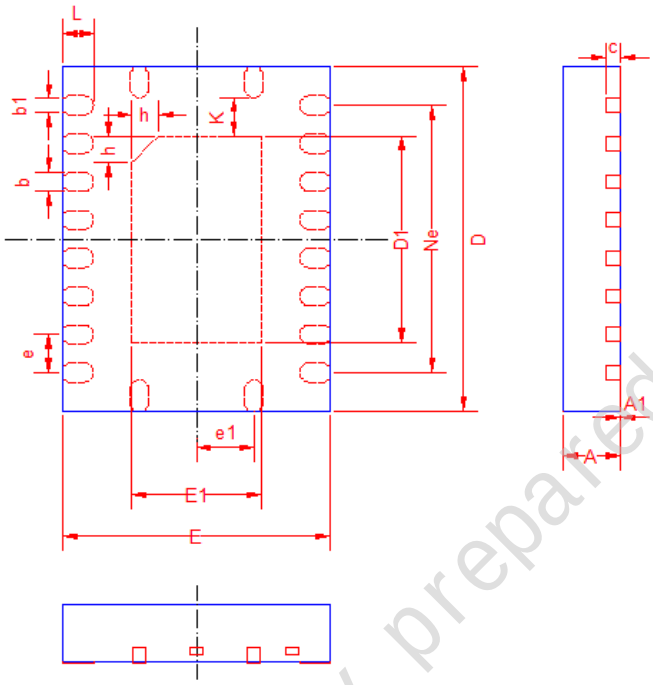


Figure 61 Package Dimensions

Table 2 Package Dimensions

SYMBOL	Dimensions(mm)		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	4.40	4.50	4.60
D1	2.60	2.70	2.80
e	0.50BSC		
e1	0.75BSC		
Ne	3.50BSC		
E	3.40	3.50	3.60
E1	1.60	1.70	1.80
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Notes:

(1) This drawing is subject to change without notice

(2) The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

12.1.2 Recommended Land Pattern

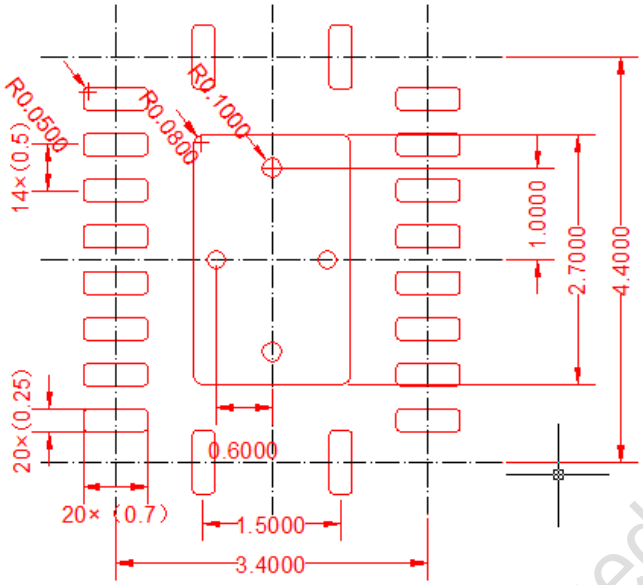


Figure 62 Recommended Land Pattern

Notes：

(1) All linear dimensions are in millimeters.

(2) It is recommended that vias under paste be filled, plugged or tented.

12.2 Recommended Stencil Design

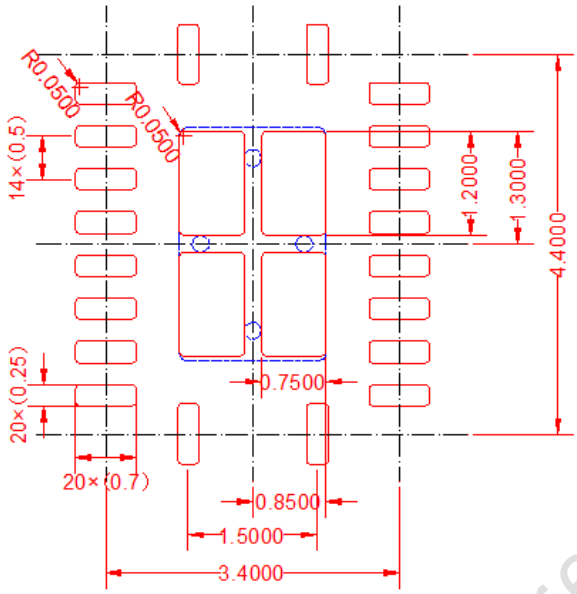


Figure 63 Recommended Stencil Design

Note：

(1) All linear dimensions are in millimeters.

12.3 Reel and Tape Information

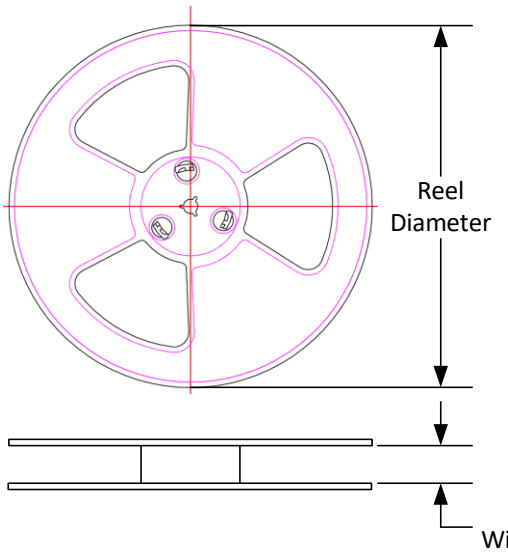


Figure 64 Reel Dimensions

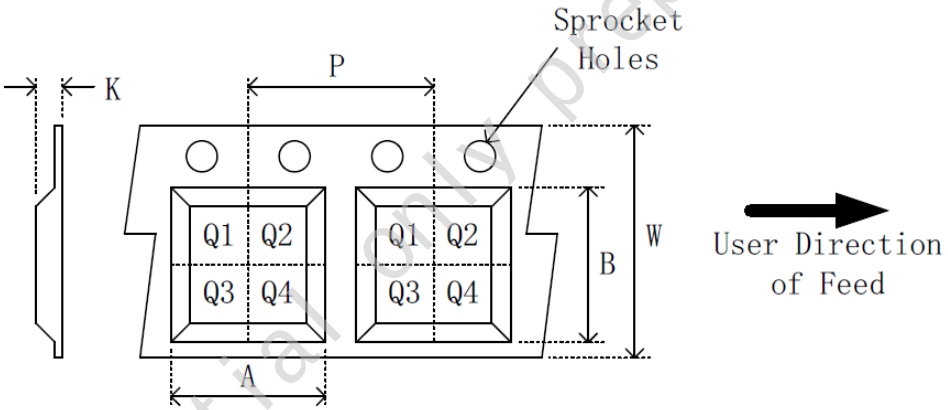


Figure65. Tape Dimensions

Device	Package Type	Pins	Quantities (PCS)	Reel Diameter (mm)	Reel Width W1(mm)	A (mm)	B (mm)	K (mm)	P (mm)	W (mm)	Pin1 Quadrant
MK9286	QFN-20	20	3000	329	12.4	3.8	4.8	1.18	8	12	Q1

12.4 Reel Box Dimensions

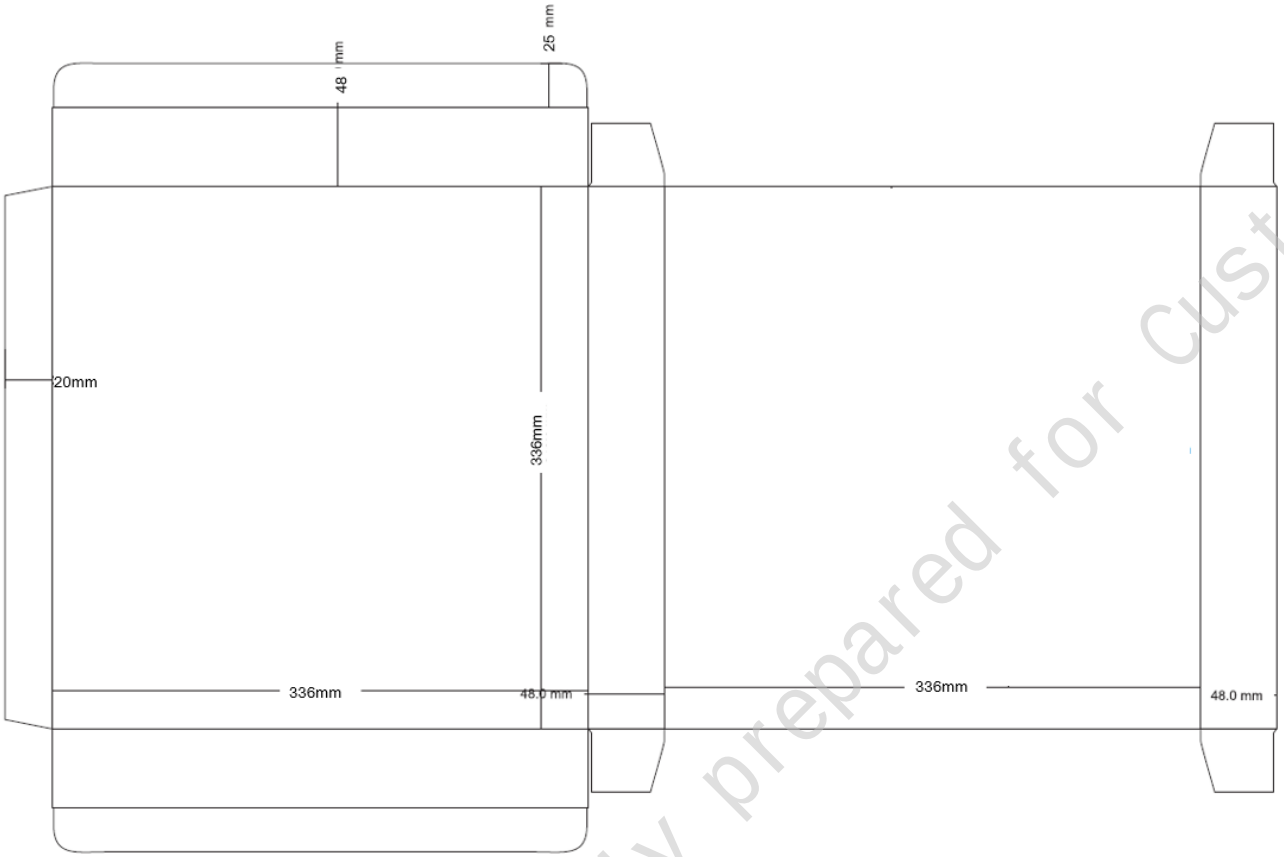


Figure66. Rell Box Dimensions

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.