MK2554A Continuous Conduction Mode PFC Controller

1. Description

The MK2554A family are continuous conduction mode (CCM) power factor correction (PFC) controllers designed for high performance AC/DC power systems. With multimode control strategy, the MK2554A achieves ultralow THD and near-unity power factor across various operating conditions. It features an internally fixed frequency, along with frequency dithering to enhance EMI performance.

The MK2554A operates within a wide supply voltage range from 11V to 28V, making it suitable for diverse application scenarios. MK2554A integrates open/short protections for feedback and sense pins to reduce the risk of system damages. Additional system-level protection features include peak current limiting, input brown-out detection, and output over-voltage/under-voltage detection. An accurate reference voltage ensures precise and reliable protection thresholds, while internal clamp circuitry limits the gate drive voltage to below 15.5 V.

2. Applications

- Boost PFC Power Converters
- Industrial Power Supplies
- Server and Desktop Power Supplies
- High Power LED Power Supplies

3. Features

- Wide VCC Voltage Range: 11V to 28V
- Ultra-Low Startup Current: < 55uA
- Accurate Fully Integrated Oscillator: 65kHz / 130kHz / 200kHz
- Dynamic Load Enhancer
- Frequency Dithering
- Soft−Start for Smoothly Startup Operation
- ±1% Voltage Reference
- Multimode Operation (Optimized for Line/Load Range Performance)
- Feedback and Sense Pin Open/Short Protection
- Available in SOP-8 Package

4. Typical Application

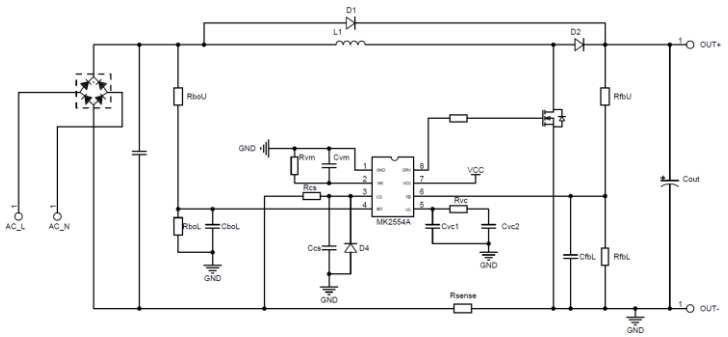

Figure 1. Typical Application Diagram

5. Order Information

Order Part Number	Descriptions
MK2554AX65AB	SOP-8, tape, 4000 pcs/reel
MK2554AX130AB	SOP-8, tape, 4000 pcs/reel
MK2554AX200AB	SOP-8, tape, 4000 pcs/reel
MK2554AA130AB	SOP-8, tape, 4000 pcs/reel
MK2554AA200AB	SOP-8, tape, 4000 pcs/reel

6. Pin Configuration and Functions

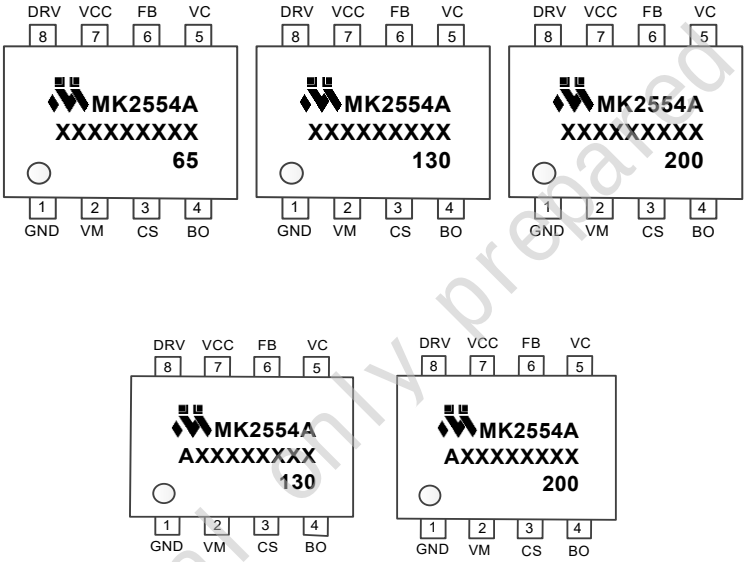

Figure 2. Pin Connection (top view)

Table 1. Pin Functions

Pin		Descriptions
NO.	Name	
1	GND	Device ground reference.
2	VM	This pin generates a voltage signal VM for the PFC duty cycle modulation, with pin open/short protection. Connect a resistor R_{VM} between the VM pin and GND, which value is proportional to the input impedance of the PFC circuits, allowing designers to fine-tune the maximum delivered power by the PFC stage. The addition of an external capacitor C_{VM} between the VM pin and GND determines the current-mode control strategy. The device operates in average current mode if C_{VM} is present. Otherwise, it operates in peak current mode.
3	CS	This pin sources a current I_{CS} that is proportional to the inductor current. The sensed current I_{CS} provides a feedback signal for PFC duty cycle modulations. I_{CS} also supports critical safety functions, including inrush current detection, overcurrent protection (OCP) and zero current crossing detection (ZCD).
4	BO	This pin is used for input brown-out (BO) protection and overpower limitation (OPL). It needs to be connected to the rectified main input voltage through a resistor divider. Additionally, a capacitor must be connected between the BO pin and ground (GND). The BO pin detects a voltage signal that is proportional to the average input voltage (after rectification).
5	VC	This pin is the output of the transconductance error amplifier, referred to as the VC pin. The VC pin must be connected to external type−2 compensation components that limit the bandwidth of the VC signal to typically below 20Hz to ensure the system achieve near-unity power factor. This pin also has pin open/short protection.
6	FB	This pin serves as the inverting input of the transconductance error amplifier. It receives feedback information about the PFC converter's output voltage via a resistor divider.
7	VCC	This pin is the positive supply of the IC, responsible for powering the device. The device begins operation when the VCC voltage rises above the turn-on threshold $V_{CC\text{-}ON}$ and shuts down when VCC drops below the turn-off threshold $V_{CC\text{-}OFF}$. After successful start−up, the device operates within a range of 11V to 28V.
8	DRV	This pin integrated a push-pull gate driver designed to control one or more external power MOSFETs. It provides a peak source current of 1.5A and a peak sink current of 1.5A. The gate driver 's output voltage is clamped at 15.5 V.

7. Specifications

7.1 Absolute Maximum Ratings (1)

Symbol	Parameter	Min	Max	Unit
VCC	supply voltage VCC	-0.3	30	V
DRV (2)	output gate driver	-0.3	20	
FB/VC/BO/VM (2)	voltage on pin FB, VC, BO, VM	-0.3	8	
CS	voltage on pin CS	-3	8	
T_J	operating junction temperature,	-40	150	°C
T_{stg}	storage temperature	-55	150	
T_{sld}	soldering temperature (10 second)		260	

Notes:

(1) Stresses beyond the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in "RECOMMENED OPERATING CONDITIONS". Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Output pin not to be voltage driven.

7.2 ESD Ratings

		Value	Unit
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±2000	

Notes:

（1） JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

（2） JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Moisture Sensitivity Level

Moisture Sensitivity Level	SOP-8	MSL1

7.4 Recommended Operating Conditions

		Min	Max	Unit
Recommended Operation Conditions	VCC supply voltage	11	28	V
	operating junction temperature (T_J)	-40	125	°C

7.5 Thermal Information

			Value	Unit
Package Thermal Resistance (1)	SOP-8	θ_{JA} (Junction to ambient)	128	°C/W
		θ_{JC} (Junction to case)	75	

Note:

（1） Measured on JESD51-7, 4-layer PCB.

7.6 Electrical Characteristics

-40°C ≤ T_A = T_J ≤ 125°C. V_{CC} = 15V_{DC}, 1µF from VCC to GND. All voltages are measured with respect to ground (pin 1). Currents are positive when flowing into the IC, unless otherwise specified.

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
Supply Voltage Management						
V_{CC_ON}	V_{CC} UVLO Rising		9.50	10.70	11.50	V
V_{CC_OFF}	V_{CC} UVLO Falling		8.25	9.10	9.75	V
V_{CC_HYST}	V_{CC} UVLO Hysteresis			1.6		V
I_{ST}	Start-up Current	Before turn-on, V_{CC}=9V			55	µA
I_{OP}	Operating Current	V_{CC}=15V, no load, no switching, T_J=25℃		0.8	1.5	mA
I_{STDN}	Shutdown Mode Current	V_{CC}=15V, V_{FB}=0V		156	260	uA
Regulation Block						
V_{REF}	Voltage Reference	V_{CC}=15 V	2.43	2.50	2.57	V
V_{REF}	Voltage Reference	V_{CC}=15 V; T_J=25℃	2.475	2.500	2.525	V
I_{EA}	Error Amplifier Current Capability (1)	V_{CC}=15 V		±28		µA
G_{EA}	Error Amplifier Gain (1)	V_{CC}=15 V		230		µS
I_{FB}	Pin 6 Bias Current	V_{FB} = V_{REF}	-500		800	nA
V_{C_MAX}	Maximum Control Voltage	V_{FB} = 2 V		3.6		V
V_{C_MIN}	Minimum Control Voltage	V_{FB} = 3 V		0.6		V
ΔV_C	ΔV_C = V_{C_MAX} – V_{C_MIN}		2.8	3.0	3.2	V
V_{FB_ODE} /V_{REF}	V_{OUT} Low Detect Threshold/V_{REF}		92.0	94.7	98.0	%
V_{FB_ODE} $_{(HYS)}$ /VREF	V_{OUT} Low Detect Hysteresis/V_{REF}			2		%
Current Sense Block						
I_S	Overcurrent Protection Threshold	T_J=25℃	190	200	210	µA
Power Limitation Block						
I_{OPL}	Overpower Limitation Threshold	I_{OPL} = I_{CS} *V_{BO}		200		µVA

$I_{CS\ (OPL1)}$	Overpower Current Threshold	V_{BO} = 0.9 V, V_M = 3 V	175	210	245	μA
$I_{CS\ (OPL2)}$	Overpower Current Threshold	V_{BO} = 2.7 V, V_M = 3 V	60	75	90	μA
PWM Block						
D_{CYCLE}	Duty Cycle Range (1)			0-97		%
T_{LEB}	Leading Edge Blanking Time (1)			300		ns
Oscillator Block						
F_{SW}	Central Frequency	MK2554AX65AB, T_J=25℃	60	65	70	kHz
F_{SW}	Central Frequency	MK2554AX130AB, MK2554AA130AB T_J=25℃	120	130	140	kHz
F_{SW}	Central Frequency	MK2554AX200AB, MK2554AA200AB T_J=25℃	184	200	216	kHz
Brown-out Detection Block						
V_{BOH}	Brown-out Voltage Threshold (rising)		1.23	1.30	1.37	V
V_{BOL}	Brown-out Voltage Threshold (falling)		0.65	0.70	0.75	V
I_{BO}	Pin 4 Input Bias Current	V_{BO} = 1 V	-300		300	nA
Current Modulation Block						
I_{M1}	Multiplier Output Current	C_{VC} = 30 nF, V_{BO} = 0.9 V, I_{CS} = 25 μA, V_{FB} = 2 V		1.9		μA
I_{M2}	Multiplier Output Current	C_{VC} = 30 nF, V_{BO} = 0.9 V, I_{CS} = 75 μA, V_{FB} = 2 V		5.8		μA
I_{M3}	Multiplier Output Current	C_{VC} = 30 nF, V_{BO} = 1.5 V, I_{CS} = 75 μA, V_{FB} = 2 V	7.5	10.0	12.5	μA
I_{M4}	Multiplier Output Current	V_C = 0.8 V, V_{BO} = 0.9 V, I_{CS} = 25 μA, V_{FB} = 2 V		28		μA
I_{M5}	Multiplier Output Current	V_C = 0.8 V, V_{BO} = 0.9 V, I_{CS} = 75 μA, V_{FB} = 2 V		80		μA
Overvoltage Protection						
V_{OVP}/V_{REF}	Ratio (Overvoltage Threshold/ V_{REF})		102	105	108	%

$V_{OVP(HYS)}$ /V_{REF}	Ratio (Overvoltage Threshold Hysteresis / V_{REF})			3		%
Undervoltage Protection						
$V_{UVP(ON)}$ /V_{REF}	UVP Activate Threshold Ratio		5	8	11	%
$V_{UVP(OFF)}$ /V_{REF}	UVP Deactivate Threshold Ratio		10	12	14	%
$V_{UVP(H)}$ /V_{REF}	UVP Lockout Hysteresis			4		%
Thermal Shutdown						
T_{SD}	Thermal Shutdown Threshold (1)		150			°C
H_{SD}	Thermal Shutdown Hysteresis (1)			30		°C
Gate Driver						
T_{RR}	Gate Drive Voltage Rise Time from 1 V to 11V	C_{LOAD} = 2.2nF R_{GS} = 10kΩ V_{CC} = 12V		58		ns
T_{RF}	Gate Drive Voltage Fall Time from 11 V to 1 V	C_{LOAD} = 2.2nF R_{GS} = 10kΩ V_{CC} = 12V		30		ns
I_{VG_H}	Maximum Source Current (1)			1.5		A
I_{VG_L}	Maximum Sink Current (1)			1.5		A
R_{sink}	Pull-down Impedance	I_{LOAD}= 100mA		1		Ω
V_{VG_H}	Pin 8 Clamp Voltage	V_{CC} = 18V		15.5		V

Note:

(1) Values are guaranteed by design and verified by characterization on bench, not tested in production.

7.7 Typical Characteristics

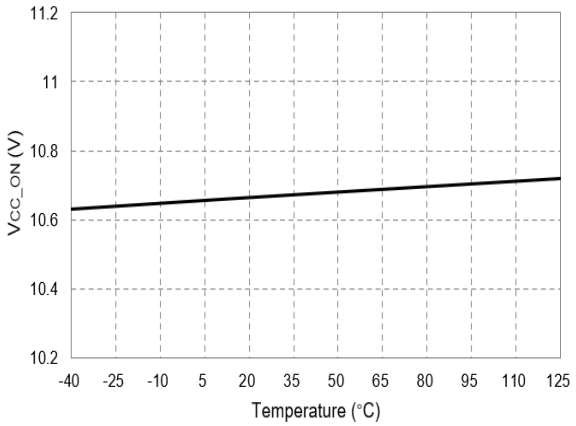

Figure 3. VCC UVLO Rising vs. Temperature

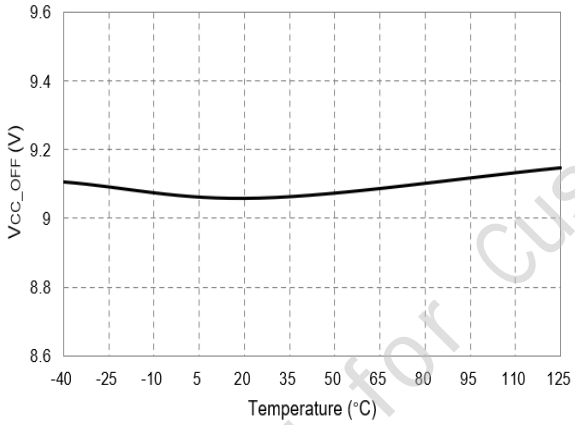

Figure 4. VCC UVLO Falling vs. Temperature

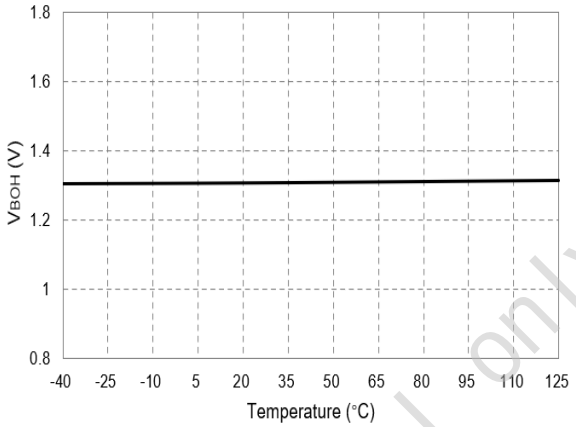

Figure 5. Brown-out Voltage (Rising) vs. Temperature

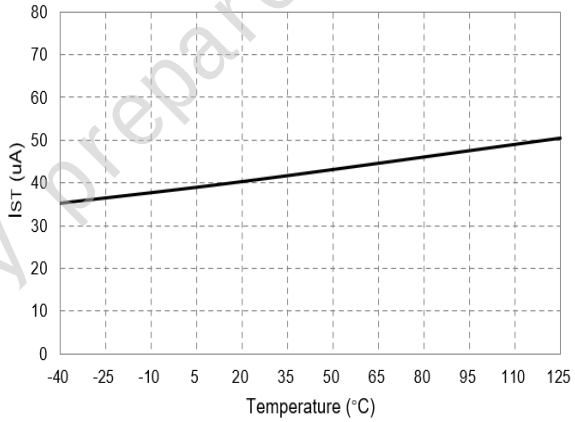

Figure 6. Start-Up Current (Before Turn-On) vs. Temperature

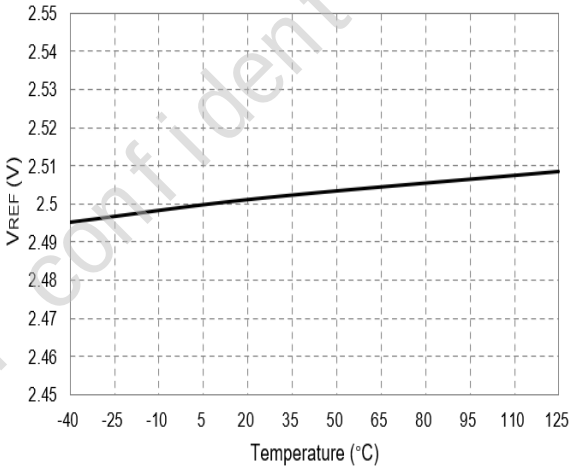

Figure 7. Reference Voltage vs. Temperature

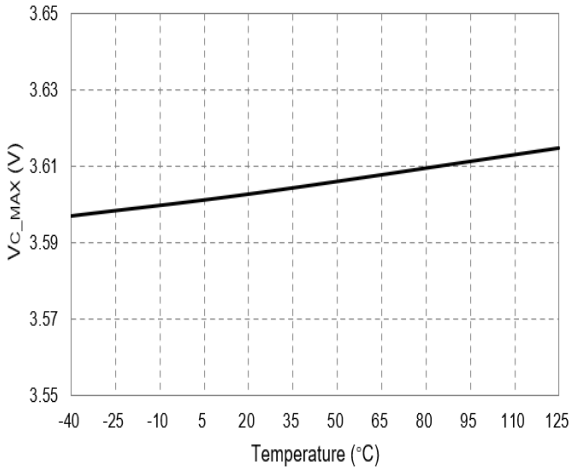

Figure 8. Maximum Control Voltage vs. Temperature

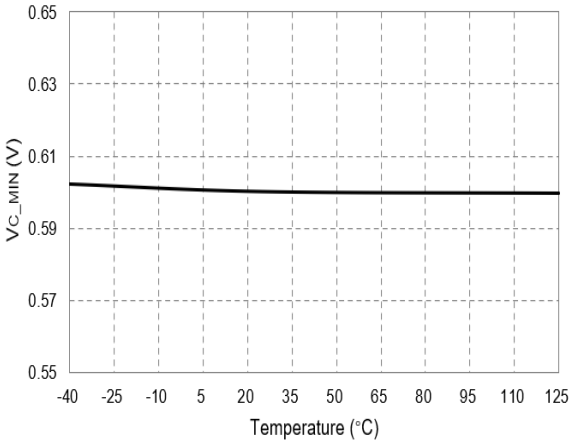

Figure 9. Minimum Control Voltage vs. Temperature

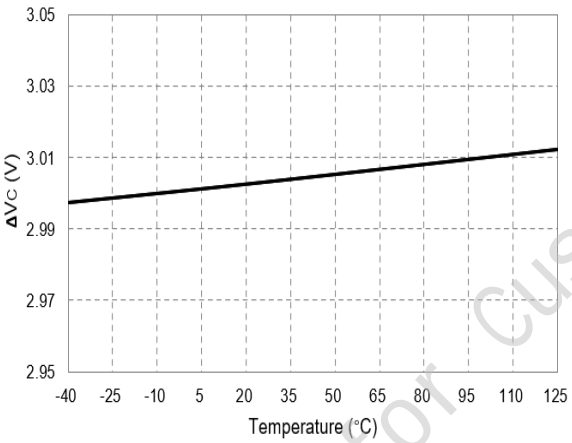

Figure 10. ΔVc vs. Temperature

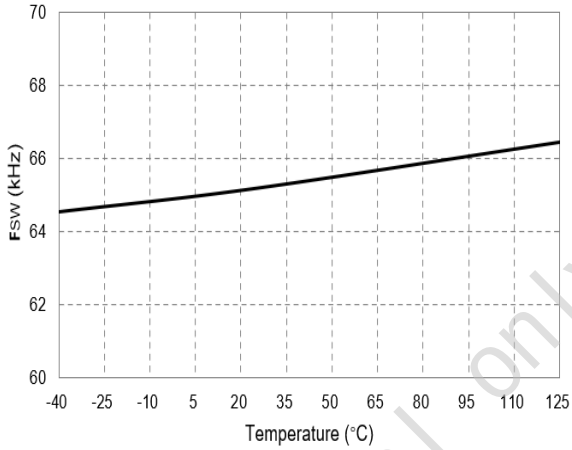

Figure 11. Switching Frequency (Based on 65 kHz) vs. Temperature

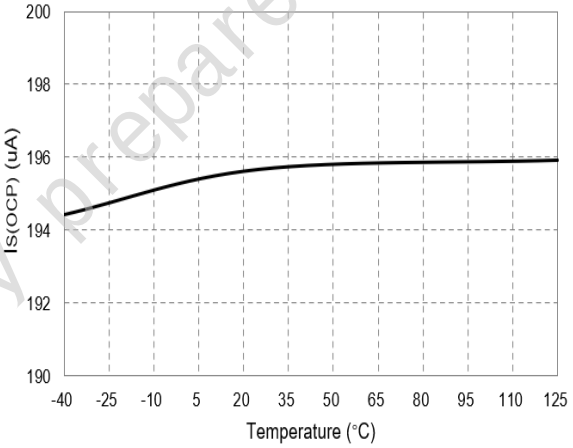

Figure 12. Overcurrent Protection Threshold vs. Temperature

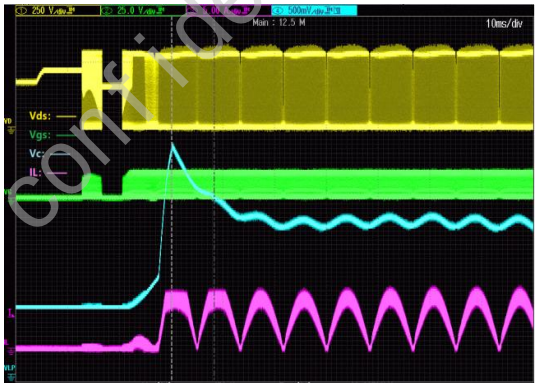

Figure 13. Dynamic Load Enhancer

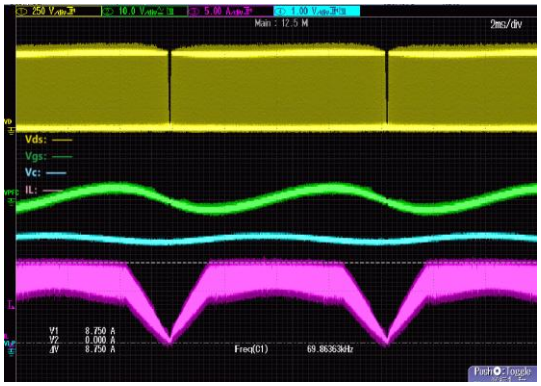

Figure 14. Overcurrent Protection

8. Detailed Description

8.1 Overview

The MK2554A family comprises continuous conduction mode (CCM) PFC controllers designed to operate at a fixed switching frequency. Leverage a multimode control strategy, the devices achieve ultralow THD and near-unity power factor across diverse operating conditions. Additionally, the family integrates frequency dithering—a feature that spreads the noise spectrum to reduce potential radiated electromagnetic interference (EMI).

In CCM operation, the lower peak current and reduced di/dt (current change rate) minimized power losses, directly enhancing system efficiency. An accurate internal voltage reference voltage ensures the reliability of both internal logic circuits and protection mechanisms. By simplifying the design of peripheral PFC circuits, the MK2554A shortens production development cycles.

The MK2554A is pin-compatible with other PFC controllers of similar functionality but offers enhanced features have been implemented to reduce bill of materials (BOM) cost. System performance is further optimized through: An expanded operating voltage range, paired with an improved startup strategy, enabling easier to startup even in high-power systems; An innovative dynamic output voltage protection enhancement circuit, which boosts stability under dynamic load conditions (e.g., sudden changes in load current); A soft-start function and optimized operating currents, which reduce current stress on components and lower overall power consumption.

Robust system reliability is ensured by a suite of intelligent protection functions, including gate driver output voltage clamp, feedback and sense pin open/short protection, brown-in and brown-out protection (monitors input voltage stability), output overvoltage protection (OVP) and undervoltage protection (UVP), overcurrent protection (OCP), and smart overpower limitation (OPL).

8.2 Functional Block Diagram

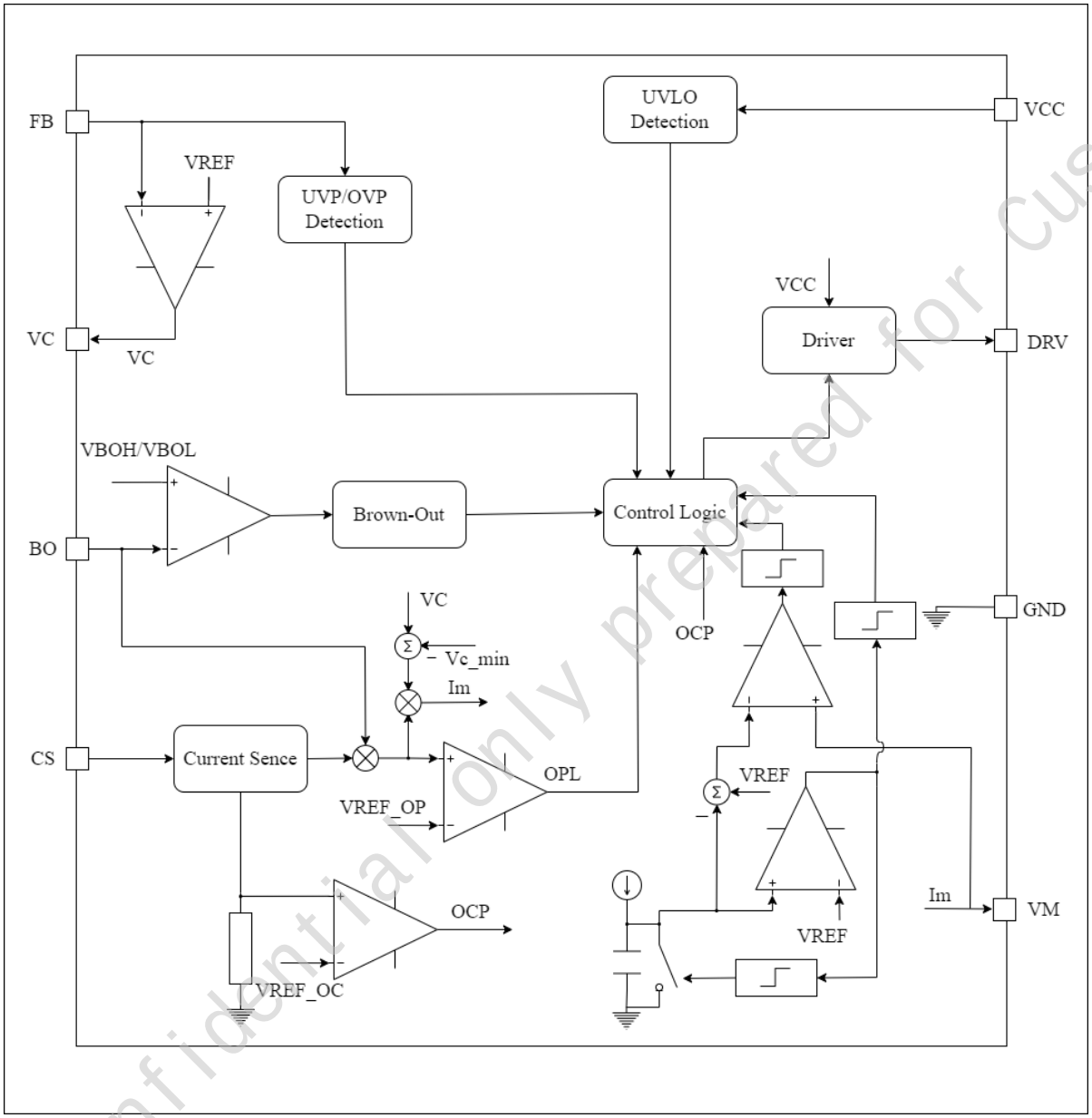

Figure 15. Block Diagram

8.3 Feature Description

8.3.1 VCC Power Supply and Undervoltage Lockout (UVLO)

The MK2554A operates with a VCC voltage range of 11V to 28V, making it adaptable to diverse application scenarios. For optimal performance, a typical 0.1uF decoupling capacitor is recommended—this should be placed as close as possible to the VCC and GND pins to stabilize the supply voltage. Additionally, a 1uF to 10uF VCC bypass capacitor, connected in parallel with the decoupling capacitor, is advised to suppress noise ripple generated during switching operation.

The MK2554A integrates an undervoltage lockout (UVLO) protection mechanism in its VCC supply circuit, ensuring the controller remains in a safe state until power conditions are stable. When the VCC voltage rises above the turn-on threshold $V_{CC\text{-}ON}$, the controller exits the UVLO state and activates its internal circuitry. If the VCC voltage drops below the turn-off threshold $V_{CC\text{-}OFF}$, the controller re-enters the UVLO state to prevent improper operation under insufficient voltage.

To protect external power MOSFETs from overvoltage damage, the MK2554A includes a gate driver voltage clamp. When the VCC supply voltage exceeds 18V, the voltage at the DRV pin (Pin 8) is clamped to a safe level V_{VG_H}. This prevents excessive gate voltage from degrading or destroying the MOSFETs' gate oxide layers, even under high VCC conditions.

8.3.2 Brown−In and Brown−Out Protection

When the power line voltage decreases, the input current must rise to maintain a constant output voltage for a given load. This increase in current can lead to higher RMS input current, which may cause excessive thermal stress on the system. Brownout protection mitigates this risk by preventing such stress from exceeding safe operating limits.

The MK2554A implements input undervoltage (brownout) protection by detecting the rectified input voltage via BO pin (Pin 4). A key component in this process is the filter capacitor C_{BO}, typically a 0.47 µF device connected to the VBO pin. This capacitor converts the RMS value of the input voltage into an average voltage signal—smoothing out fluctuations to provide a stable detection reference. Figure 16 and Figure 17 illustrate the V_{BO} waveforms: the former shows the unfiltered signal (reflecting the rectified input's RMS characteristics), while the latter displays the filtered signal (the average value, stabilized by C_{BO}). V_{BO} voltage is defined in Equation 1, where V_{AC} is the RMS value of input voltage.

$$V_{BO} = \frac{2\sqrt{2}}{\pi} V_{AC} \times \frac{R_{BOL}}{R_{BOL} + R_{BOU}} \quad (1)$$

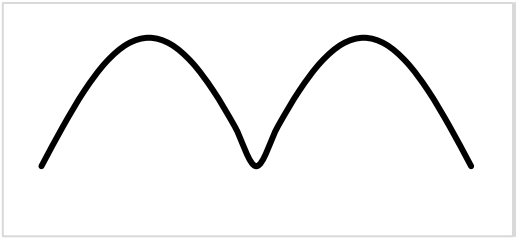

Figure 16. Before Average

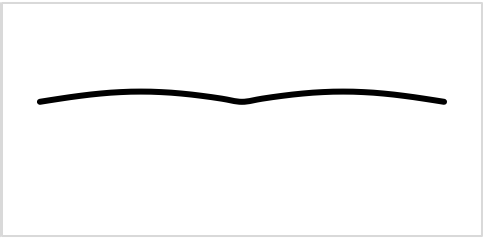

Figure 17. After Average

When the rectified input voltage V_{BO} exceeds V_{BOH} (1.3V, typical) and the VCC supply voltage exceeds V_{CC-ON}, the PFC power stage initiates a soft start. During this phase, the VC pin voltage rises at a controlled rate, gradually ramping up the gate driver output to prevent inrush currents and voltage overshoot. If the BO pin voltage V_{BO} drops below V_{BOL} (0.7 V, typical), indicating a brown-out condition, the gate driver output is not immediately disabled. Instead, the controller waits for a deglitch time to confirm the voltage drop is sustained, avoiding false triggers from transient noise. The large hysteresis between V_{BOL} (brownout threshold) and V_{BOH} (brown in threshold) prevents rapid cycling (chattering) when the input voltage hovers near the critical level. This design allows the MK2554A to maintain stable operation even under marginal input conditions, ensuring reliable performance in applications with varying power line quality.

8.3.3 Overcurrent Protection (OCP) and Overpower Limitation (OPL)

Under conditions like inrush, brown-out recovery, and output over-load, the PFC power stage experiences high currents. Protecting power devices from switching under these conditions is critical to prevent damage.

Real-time sampling of inductance current is achieved using two resistors R_{sense} and R_{CS}. A low value resistor R_{sense} placed in the return path of input rectifier, connected between the rectifier and system ground. The voltage across R_{sense} (always negative) is sensed on the rectifier side. The MK2554A controller maintains the CS pin at 0 V by sourcing a current I_{CS}, which is proportional to the inductor current I_L via the relationship shown in Equation 2. This equation allows the controller to accurately represent the inductor current using I_{CS}. The current I_{CS} is used in the PFC duty modulation to generate the multiplier voltage VM, overcurrent protection (OCP) and overpower limitation (OPL).

$$I_{cs} = \frac{R_{sense}}{R_{cs}} I_L \quad (2)$$

The I_{CS} current serves three key functions: Duty Cycle Modulation - I_{CS} is used to generate the multiplier voltage VM for PFC duty cycle control; Overcurrent Protection (OCP) - If I_{CS} exceeds the OCP threshold (I_S), the MOSFET is turned off until reset by the clock signal; Overpower Limitation (OPL) – If the product of I_{CS} and V_{BO} (I_{CS}* V_{BO}) exceeds the OPL threshold, the MOSFET is similarly disabled. When either OCP or OPL is triggered, the MOSFET gate driver is immediately turned off, and the PWM latch remains latched off until reset by the clock signal, ensuring a full switching cycle elapses before reactivation.

8.3.4 Overvoltage Protection (OVP) and Undervoltage Protection (UVP)

The MK2554A's internal reference voltage (V_{REF}) for the output regulation exhibits high precision, maintaining an accuracy of less than ±3% over the temperature range and less than ±1% at room temperature. The output voltage V_{out} is monitored at the FB pin through a resistor divider (R_{FBL} and R_{FBU}). The relationships are defined by Equation 3:

$$V_{out} = \frac{R_{FBL} + R_{FBU}}{R_{FBL}} V_{REF} \quad (3)$$

And Equation 4:

$$V_{FB} = \frac{R_{FBL}}{R_{FBL} + R_{FBU}} V_{out} \quad (4)$$

The MK2554A continuously monitors the FB pin voltage. If V_{FB} exceeds the overvoltage protection (OVP) threshold, the driver signal is immediately halted to prevent damage. Protection is maintained until V_{FB} drops below the OVP threshold minus a hysteresis value, ensuring stable operation and preventing rapid cycling.

When V_{FB} falls below the UVP threshold, the MK2554A enters a low power shutdown state to minimize power consumption. To restart, V_{FB} must rise above the UVP threshold plus a hysteresis value, providing a controlled recovery mechanism.

The controller includes additional safeguards: Resistor Divider Faults - If the lower resistor R_{FBL} is shorted to ground or the upper resistor R_{FBU} is open, the MK2554A triggers protection and shuts down; VC/VM Pin Protection – Similar fault detection mechanisms are implemented for the VC and VM pins, ensuring robust operation even under component failures.

These features collectively enhance system reliability by preventing operation outside safe voltage limits and detecting critical faults in the feedback network.

8.3.5 Dynamic Load Enhancer (DLE)

The output voltage of PFC stages may experience excessive overshoots or undershoots when subjected to load steps or input voltage fluctuations. These transients can strain the system, as the low-bandwidth voltage loop—optimized for steady-state performance—responds too slowly to correct them in time. The MK2554A's dynamic load enhancer addresses this by accelerating the loop response during large disturbances, ensuring fast and stable voltage regulation.

As illustrated in Figure 18, the mechanism activates when the output voltage deviates from its regulated setpoint. If the output voltage drops below a predefined threshold V_{FB_ODE}, the internal comparator COMP switches to a high state, activating the dynamic load enhancer. Once activated, an additional current source is enabled. The current from this source is proportional to the difference between the FB pin voltage V_{FB} and the internal reference voltage V_{REF} (i.e., V_{FB} - V_{REF}). This extra current rapidly raises the voltage at the VC pin. By boosting the VC pin voltage quickly, the PFC duty cycle adjusts faster than the standard low-bandwidth loop would allow. This prevents the output voltage from dropping excessively and significantly improves transient response—minimizing undershoots during load or input voltage changes.

The dynamic load enhancer bridges the gap between the steady-state stability of a low-bandwidth loop and the need for rapid correction during transients. It ensures the PFC output remains within acceptable limits even under sudden load or input voltage variations, enhancing overall system robustness.

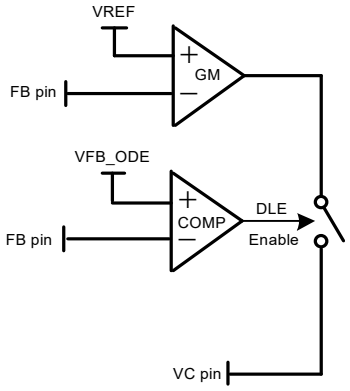

Figure 18. Dynamic Load Enhancer

8.3.6 Multiplier Voltage

The multiplier in the MK2554A serves two core functions: power protection and loop control.

The first key role of the multiplier is to enable overpower protection by generating a product of the sense current I_{CS} and the BO pin voltage V_{BO}, denoted as I_{CS}* V_{BO}. This product is a direct indicator of the input power: I_{CS} is proportional to the inductor current (I_L), and V_{BO} is proportional to the RMS input voltage (V_{AC}). Together, they reflect the real-time power flowing through the PFC stage. If I_{CS}* V_{BO} exceeds the overpower threshold I_{OPL}, the controller shuts off the MOSFET to prevent excessive power stress, triggering OPL.

The second role is to generate a control current I_M that regulates the PFC loop, determining the operating mode (average or peak current control) based on external components. The current I_M is defined by Equation 5:

$$I_M = k \frac{I_{CS} * V_{BO}}{V_C - V_{C\_min}} \quad (5)$$

Where, k is the current gain (a fixed internal parameter); V_{BO} is the input voltage at the BO pin (proportional to RMS input voltage, as covered in earlier sections); I_{CS} is the sense current proportional to the inductor current I_L as described in 8.3.3; V_C is the control voltage from the transconductance error amplifier (OTA output, at the VC pin); V_{C_min} is fixed minimum threshold voltage (constant).

I_M flows out of the VM pin and creates a voltage V_M across the external resistor R_{VM} (V_M=I_M*R_{VM}). The presence of an external capacitor (C_{VM}) at the VM pin determines the control mode. If C_{VM} is connected, it bypasses high-frequency noise in the VM signal, stabilizing the loop. The controller operates in average current mode, which offers better stability and noise immunity. If C_{VM} is omitted, the controller defaults to peak current mode, simplifying the circuit but with slightly reduced stability under certain conditions (e.g., high duty cycles).

The MOSFET's on-time is determined by three key signals (see Figure 19): reference voltage V_{REF}, multiplier voltage V_M, and ramp voltage V_{RAMP}. By comparing these signals, the controller adjusts the on-time dynamically to maintain the desired output voltage and power factor, even as input voltage or load changes.

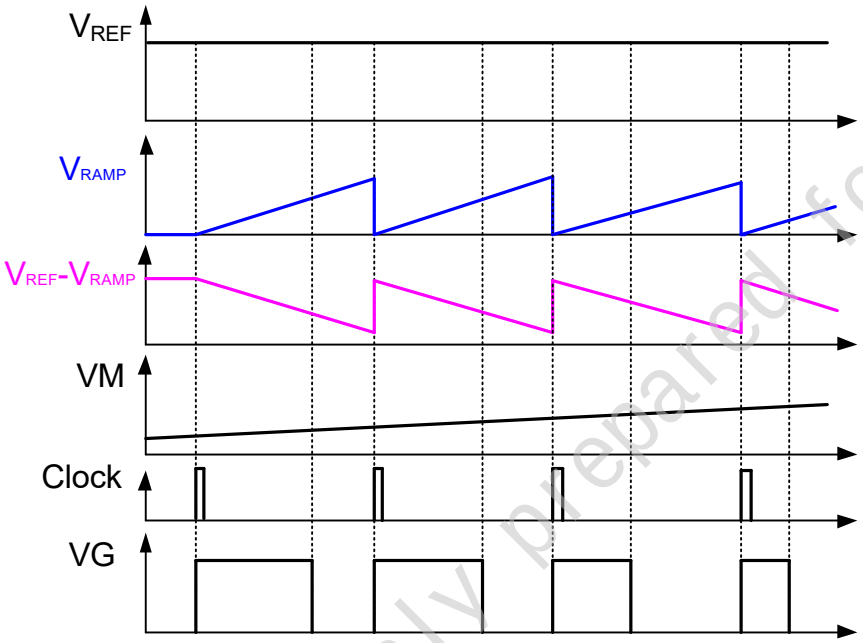

Figure 19. MK2554A Modulation and Timing Diagram

8.3.7 Dither Frequency

Dither technology is a technique that introduces small-range frequency fluctuations into the fixed-frequency signals of electronic devices. In power electronic systems (e.g., switching power supplies), this technology significantly optimizes system performance—particularly in electromagnetic interference (EMI) control. For switching power supplies using fixed-frequency PWM control chips, dither disperse harmonic energy across a wider frequency range, effectively reducing EMI peak amplitudes. This helps equipment meet relevant electromagnetic compatibility (EMC) standards.

The following table are the dither parameter configurations of each model in the MK2554A series:

Table 2. Dither Parameters of MK2554A Series Models

Model	Central Frequency	Dither Range
MK2554AX65AB	65kHz	±5kHz
MK2554AX130AB	130kHz	±10kHz
MK2554AX200AB	200kHz	±15kHz
MK2554AA130AB	130kHz	±5kHz
MK2554AA200AB	200kHz	±5kHz

9. Application and Implementation

9.1 Typical Applications

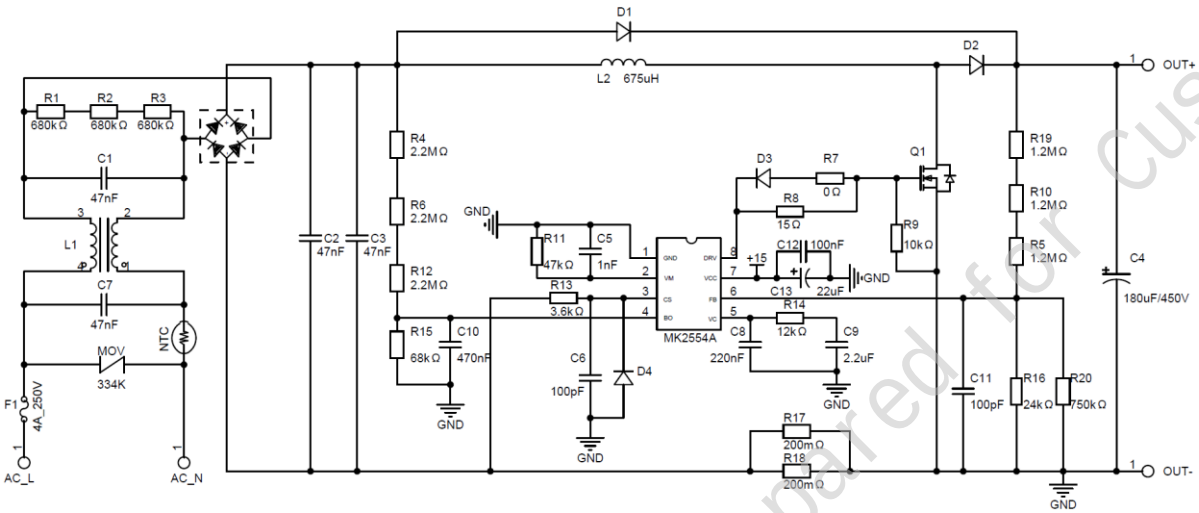

Figure 20. Reference Design Circuit

10. Power Supply Recommendations

11. Layout

11.1 Layout Guidelines

To ensure the MK2554A operates at its optimal performance and maintains noise immunity, stability, and reliability, the following layout guidelines must be strictly followed:

1. Use separate, dedicated traces for the VCC and GND pins. This prevents noise from the power path (e.g., switching transients) from coupling into sensitive signal paths, ensuring stable power delivery to the IC.
2. Include at least one low-ESR ceramic bypass capacitor (100nF) and place it as close as possible to the MK2554A's VCC and GND pins. This capacitor filters high-frequency noise from the supply voltage, suppressing voltage spikes that could disrupt internal logic or protection circuits.
3. Connect the GND pin to the ground plane using either a short, wide trace (to minimize resistance and inductance), or a direct connection to a ground plane layer beneath the IC. This ensures low-impedance grounding, critical for noise dissipation and stable reference voltages.
4. Ensure clean ground returns for signal pins. The effectiveness of filter capacitors on signal pins (BO, VC, VM) depends entirely on a low-noise ground return path. These pins handle sensitive signals (e.g., input voltage detection, control loop feedback), so their filter capacitors must connect to a quiet ground to avoid noise injection.
5. Leverage pinout for noise separation. The MK2554A's pinout is designed to physically separate high-noise and low-noise paths: high di/dt noise from the power ground (e.g., MOSFET switching) is isolated from low-current "quiet" signal ground (required for accurate sensing and control). This inherent separation reduces noise coupling into sensitive circuits.
6. Create a "star point" ground connection at the MK2554A's GND pin by adding a small cutout in the ground plane. This design consolidates all critical ground connections (e.g., signal, power, and bypass capacitor grounds) at a single point, minimizing ground loops that could introduce noise.
7. Ground CS and FB capacitors on CS and FB to quiet ground. Capacitors connected to the CS (current sense) and FB (feedback) pins must be returned directly to the quiet portion of the ground plane (separated from power ground noise). These pins handle ultra-sensitive signals (inductor current sensing, output voltage feedback), and noise here would degrade regulation accuracy or trigger false protections.
8. Minimize DRV pin trace length. The trace from the DRV pin to the MOSFET gate must be as short as possible. Long traces introduce parasitic inductance, which slows down MOSFET switching, increases switching losses, and generates EMI. Short traces ensure fast, clean gate drive signals, optimizing efficiency and reducing noise.

11.2 Layout Example

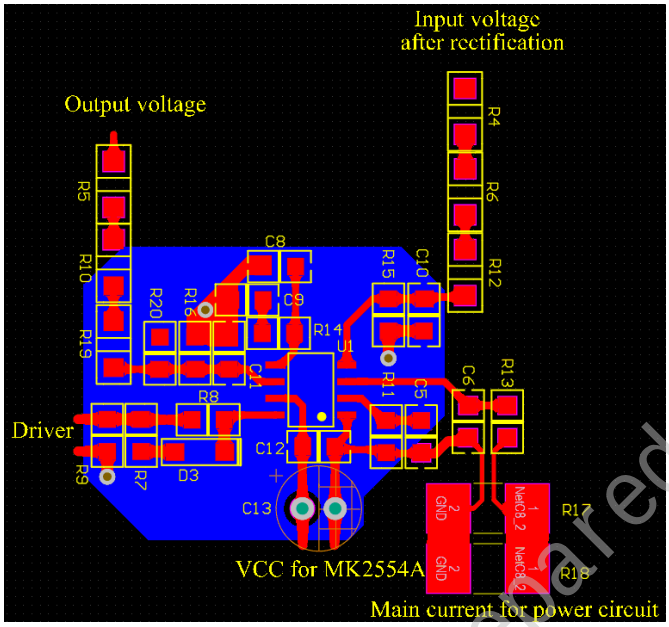

Figure 21. MK2554A Layout Example

12. Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13. Mechanical, Packaging

13.1 Package Size

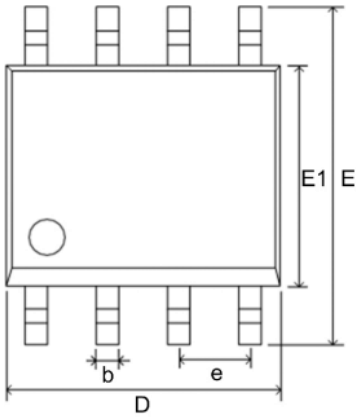

Figure 22. SOP-8 Top View

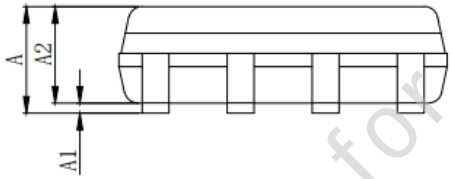

Figure 23. SOP-8 Side View

Figure 24. SOP-8 Side View

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.30	1.55	1.75
A1	0.05	-	0.25
A2	1.25	1.40	1.65
b	0.33	-	0.51
c	0.20	-	0.25
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27(BSC)		
L	0.4	-	1.27
θ	0°	-	8°

Note:

（1）This drawing is subject to change without notice

13.2 Recommended Land Pattern

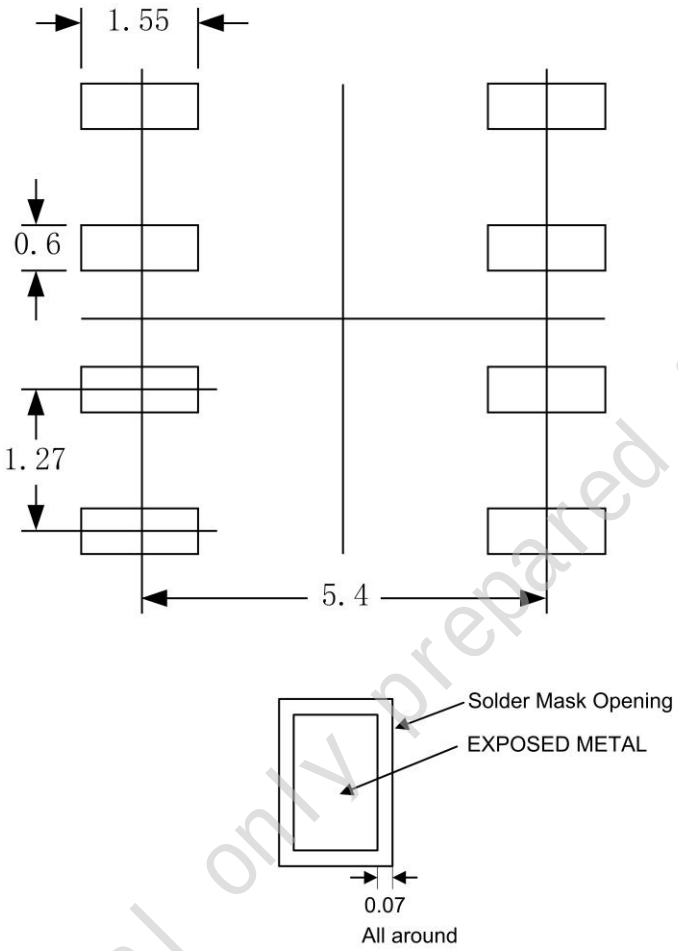

Figure 25. Recommended Land Pattern

Notes: (continued)

（1） All linear dimensions are in millimeters.

（2） It is recommended that vias under paste be filled, plugged or tented.

14. Reel and Tape Information

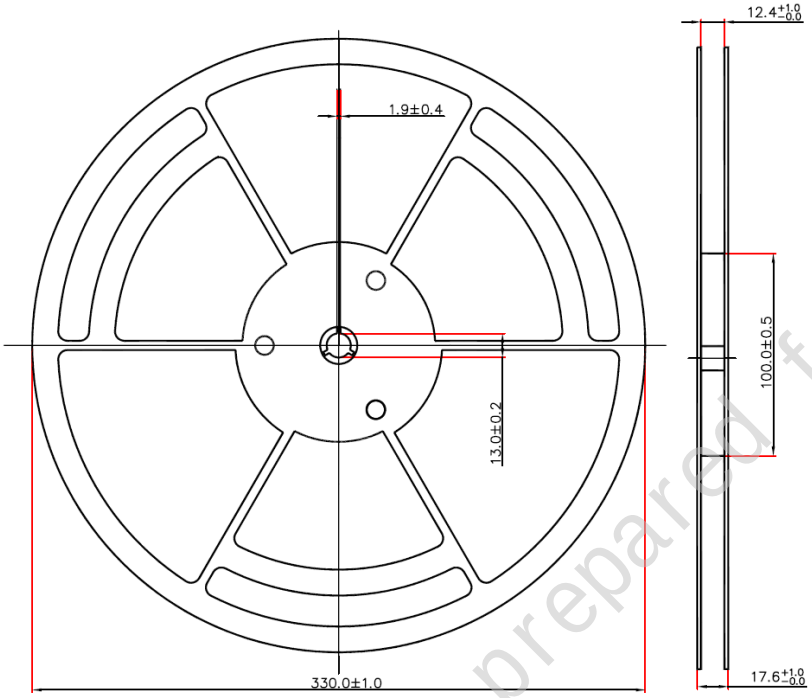

Figure 26. Reel Dimensions

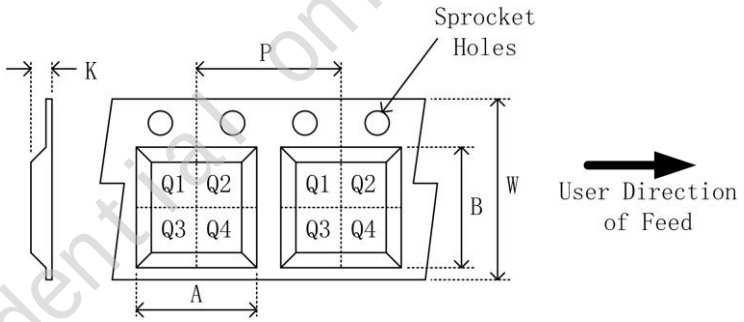

Figure 27. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
MK2554AX65AB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	12±0.1	Q1
MK2554AX130AB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	12±0.1	Q1
MK2554AX200AB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	12±0.1	Q1
MK2554AA130AB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	12±0.1	Q1
MK2554AA200AB	SOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	12±0.1	Q1

15. Tape and Reel Box Dimensions

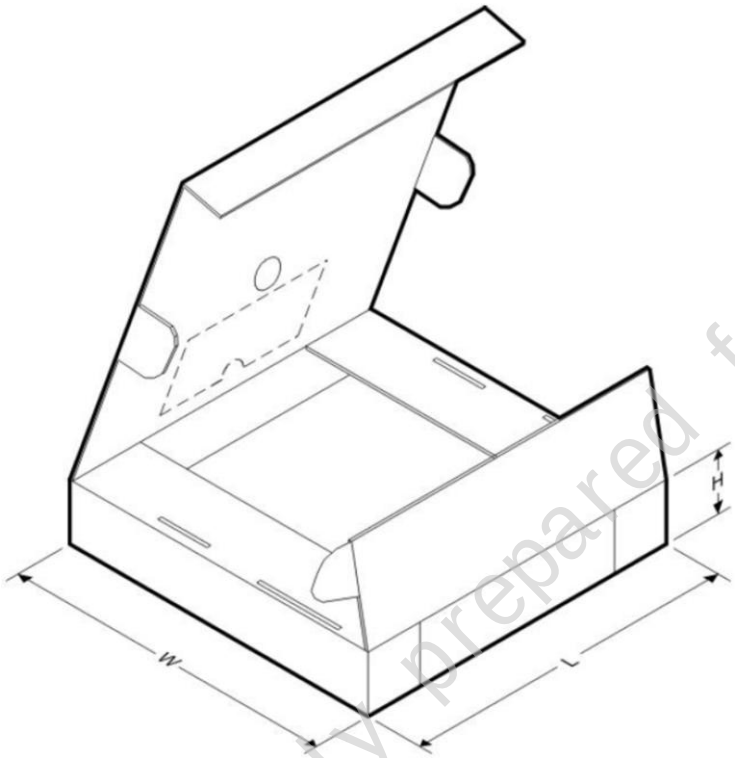

Figure 28. Box Dimensions

Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MK2554AX65AB	SOP-8	8	8000	360	360	65
MK2554AX130AB	SOP-8	8	8000	360	360	65
MK2554AX200AB	SOP-8	8	8000	360	360	65
MK2554AA130AB	SOP-8	8	8000	360	360	65
MK2554AA200AB	SOP-8	8	8000	360	360	65