High Voltage Resonant Controller

1. Descriptions

MK2189/L/D is a voltage mode LLC controller. It can be used with LLC SR controller MK1620/1 to achieve high efficiency and high reliability LLC design.

Output voltage regulation is obtained by modulating the operating frequency. A fixed deadtime inserted between the turn-off and the turn-on for high reliability.

The IC provides pin (CSS) that allows the user to program the frequency of the oscillator externally. At start-up, the switching frequency starts from a programmable maximum value and progressively decays until it reaches the steady-state value determined by the control loop. This frequency shift is non-linear to minimize output voltage overshoots, and its duration is programmable as well.

At light load, MK2189/L/D will naturally enter burst mode operation, reducing the switching loss of system devices.

A higher level OCP latches off the IC if the first-level protection is not sufficient to control the primary current. Their combination offers complete protection against overload and short circuits.

An additional protected input (DIS) allows easy implementation of OTP or OVP.

2. Applications

- AC/DC adapter
- High-Power density DC/DC
- Datacenter and telecom
- LCD and PDP TV

3. Features

- Wide VCC voltage ranges up to 26V max
- Adjustable dead time from 250ns to 1us （MK2189D）
- 50% duty cycle, variable frequency control
- Two-level OCP: frequency-shift and restart
- High-accuracy oscillator
- Up to 500 kHz operating frequency
- Burst mode operation at light load
- Burst mode acoustic noise reduction
- Burst soft ON and fast EXIT（MK2189D）
- 0.3A source and 0.8A sink driver capability
- Non-linear soft start
- Input for power ON/OFF sequencing or brownout protection
- Safe-start procedure prevents hard switching at startup
- Protection function: Auto restart （MK2189/D）or latch off（MK2189L）
- SOP-16 package

4. Typical Application

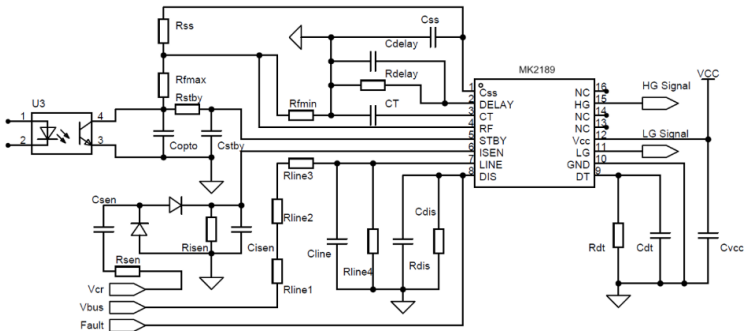


Figure 1. Typical Application Diagram

5. Order Information

Order No.	Description
MK2189XAC	SOP-16, tape, 3000 pcs/reel
MK2189LXAC	SOP-16, tape, 3000 pcs/reel
MK2189DXAC	SOP-16, tape, 3000 pcs/reel

6. Pin Configuration and Functions

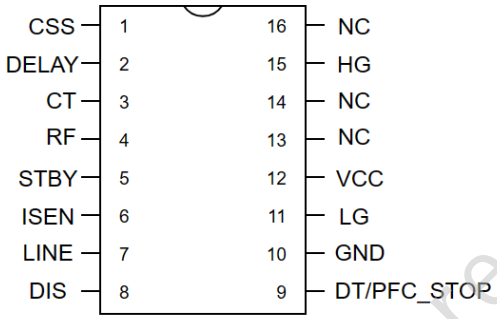


Figure 2. MK2189 Package (Top View)

Table 1. Pin Functions

Pin NO.	Name	Function	Description
1	CSS	Soft start	With an external capacitor connected between this pin and GND and a resistor connected between this pin and RF pin (Pin 4), it sets both the maximum oscillator frequency and the time constant for the frequency shift during starts up (soft-start). An internal switch discharges the external capacitor every time the chip turns off (any of VCC < UVLO, LINE < 1.24 V or > 6 V, DIS > 1.85 V, ISEN > 1.5 V, DELAY > 2 V happens) to make sure it is able to soft-start next time.
2	DELAY	Delayed shutdown	A capacitor and a resistor are connected from this pin to GND to set the maximum duration of an overcurrent condition before the IC stops switching, and the delay after which the IC restarts switching.
3	CT	Timing capacitor	A capacitor connected from this pin to GND is charged and discharged by internal current generator programmed by the external network connected to pin 4 (RF), which determines the switching frequency of the converter.
4	RF	Minimum oscillator frequency setting	This pin provides a precise 2 V reference, and a resistor connected from this pin to GND defines a current that is used to set the minimum oscillator frequency.
5	STBY	Burst mode	Burst mode operation threshold. The pin senses some voltage related to the feedback control.
6	ISEN	Current sense input	The pin senses the primary current through a sense resistor or a capacitive divider for lossless sensing. This input is not intended for a cycle-by-cycle control.
7	LINE	Line sensing input	The pin is connected to the high-voltage input bus with a resistor divider to perform either AC or DC (in systems with PFC) brownout protection.

8	DIS	Protection disable	With an internal comparator, when the voltage on this pin exceeds 1.85 V, the IC is shut down and brings its consumption almost to a “before startup” level. Tie the pin to GND if the function is not used.
9	DT/ PFC_STOP	PFC controller	This pin, normally open, is intended for stopping the PFC controller in order to protect PFC or save power. Leave the pin unconnected if not used. For the MK2189D, it can also be used to program dead time.
10	GND	Chip ground	Common ground connection for sensing networks and DRV outputs.
11	LG	Low side driver	Low-side gate drive output.
12	VCC	Supplies the controller	This supply pin accepts up to 26 Vdc. The pin is connected to an external auxiliary voltage.
13	NC	NC	-
14	NC	NC	-
15	HG	High side driver	High-side gate drive output.
16	NC	NC	-

7. Specifications

7.1 Absolute Maximum Ratings

		Min	Max	Units
Input Voltages	VCC to GND	-0.3	26	V
	DT/PFC_STOP to GND	-0.3	26	
	HG, LG to GND	-0.3	16	
	CSS, DELAY, RF, CT, ISEN, STBY, DIS to GND	-0.3	8	
	I_{RF}	0	3	mA
	I_{DELAY}	0	0.25	
Operating Junction Temperature		-40	150	°C
Storage Temperature		-55	150	
Soldering Temperature (10 second)			260	

Note:
(1) Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in “Recommended Operating Conditions”. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		Value	Units
Electrostatic Discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	V

Notes:
(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

7.3 Recommended Operating Conditions

		Min	Max	Units
Recommended Operation Conditions	VCC Voltage	9	25	V
	DIS Voltage	-0.3	3.3	
	LINE Voltage	-0.3	5	
	IRF Current	0	2	mA
	ICT Current	0	2	
	Operating Junction Temperature	-40	+125	°C

7.4 Thermal Information

		Value	Units
Package Thermal Resistance	θ_{JA} (Junction to ambient)	96	°C/W
	θ_{JC} (Junction to case)	35	°C/W

7.5 Electrical Characteristics

TJ = -40 to 125 °C, VCC = 16 V, C_{HG}=C_{LG}= 1 nF; CF = 470 pF; RF_{min}= 12 kΩ; unless otherwise specified.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IC supply voltage						
VCC	Operating range	After device turn-on	9	-	26	V
VCC_{on}	Turn-on threshold	Voltage rising @-40~125℃	9.4	10.2	11	V
		Voltage rising @25℃	9.5	10.2	11	V
VCC_{off}	Turn-off threshold	Voltage falling @-40~125℃	7.4	8.3	9	V
		Voltage falling @25℃	7.5	8.3	9	V
VCC_{hys}	Hysteresis	-		2.0		V
VZ	VCC clamp voltage	I_{clamp}= 15 mA	27	29	31	V
Supply current						
$I_{start-up}$	Startup current	Before device turn-on VCC=VCC_{on}-0.2 V	-	160	210	μA
Iq	Quiescent current	Device on, V_{STBY} = 1 V	-	0.8	1.2	mA
I_{op}	Operating current	Device on, V_{STBY} = V_{RF}	-	2.75	4	mA
Iq	Residual consumption	V_{DIS} > 1.85 V or V_{DELAY} > 3.5 V or V_{LINE} < 1.24 V or V_{LINE} = V_{clamp}	-	500	-	μA
Overcurrent comparator						
I_{ISEN}	Input bias current	V_{ISEN}=0 to $V_{ISENdis}$	-	-	-1	μA
T_{LEB}	Leading edge blanking (1)	After V_{HG} and V_{LG} low-to-high transition	-	280	-	ns
V_{ISEN}	Frequency shift threshold	Voltage rising (1)	0.77	0.8	0.83	V
$V_{ISENhys}$	Hysteresis	Voltage falling	-	50	-	mV
$V_{ISENdis}$	Restart threshold	Voltage rising (1)	1.45	1.51	1.57	V
td(H-L)	Delay to output	-	-	300	400	ns

Line sensing						
V_{th}	Threshold voltage	Voltage rising or falling (1)	1.2	1.25	1.3	V
I_{Hys}	Current hysteresis	V_{LINE} = 1.1 V	10	15	20	μA
V_{clamp}	Clamp level	I_{LINE} = 1 mA	5	-	8	V
DIS function						
I_{DIS}	Input bias current	V_{DIS} = 0 to V_{th}	-	-	-1	μA
V_{th}	Disable threshold	Voltage rising (1)	1.78	1.85	1.92	V
Oscillator						
D	Output duty cycle (1)	Both HG and LG	48	50	52	%
f_{osc}	Oscillation frequency	R_{RF} = 6.5 kΩ CT=470pF	-	100	-	kHz
		Maximum recommended			500	kHz
TD	Deadtime	Between HG and LG	0.28	0.35	0.42	μs
V_{ref}	Voltage reference at pin 4(1)	-	1.93	2	2.07	V
DT/PFC_STOP function						
I_{leak}	High level leakage current	V_{PFC_STOP} = VCC, V_{DIS} = 0 V	-	-	1	μA
R_{PFC_STOP}	ON-state resistance (1)	I_{PFC_STOP} = 1 mA, V_{DIS} = 1.5 V	-	120	-	Ω
VL	Low saturation level	I_{PFC_STOP} = 1 mA, V_{DIS} = 1.5 V	-	-	0.2	V
Dead time	Adjustable dead time	$R_{DT=}$ 20kΩ For 2189D only		350		ns
		$R_{DT=}$0 Ω For 2189D only		1000		ns
Soft-start function						
I_{leak}	Open-state current	V_{CSS}= 2 V	-	-	0.5	μA
R	Discharge (1) resistance	V_{ISEN} > V_{ISENx}	-	120	-	Ω
Standby function						
I_{DIS}	Input bias current	V_{DIS} = 0 to V_{th}	-	-	-1	μA
V_{th}	Disable threshold	Voltage falling (1)	1.2	1.25	1.3	V

Hys	Hysteresis (1)	Voltage rising	-	50	-	mV
Delayed shutdown function						
I_{leak}	Open-state current	V_{DELAY} = 0	-	-	0.5	μA
I_{CHARGE}	Charge current	V_{DELAY} = 1 V, V_{ISEN} = 0.85 V	100	140	180	μA
V_{th1}	Threshold for forced operation at max. frequency	Delay Voltage rising (1)	1.92	2.00	2.08	V
V_{th2}	Shutdown threshold	Delay Voltage rising (1)	3.35	3.5	3.65	V
Low-side gate driver (voltages referred to GND)						
V_{LGL}	Output low voltage	I_{sink} = 200 mA	-	-	1.5	V
V_{LGH}	Output high voltage	C_{load}=1000pF R_{load}=10K		13.5		V
$I_{sourcepk}$	Peak source current (1)	-	-0.3	-	-	A
I_{sinkpk}	Peak sink current (1)	-	0.8	-	-	A
t_f	Fall time	-	-	30	-	ns
t_r	Rise time	-	-	60	-	ns
$T_{on\ max}$	Max turn on time	Only MK2189		14(1)		us
Hight -side gate driver (voltages referred to GND)						
V_{HGL}	Output low voltage	I_{sink}= 200 mA	-	-	1.5	V
V_{HGH}	Output high voltage	C_{load}=1000pF R_{load}=10K		13.5		V
$I_{sourcepk}$	Peak source current (1)	-	-0.3	-	-	A
I_{sinkpk}	Peak sink current (1)	-	0.8	-	-	A
t_f	Fall time	-	-	30	-	ns
t_r	Rise time	-	-	60	-	ns
$T_{on\ max}$	Max turn on time	Only MK2189		14(1)		us

Notes:

(1) Design guarantee

(2) Values are verified by characterization on bench, not tested in production.

7.6 Typical Characteristics

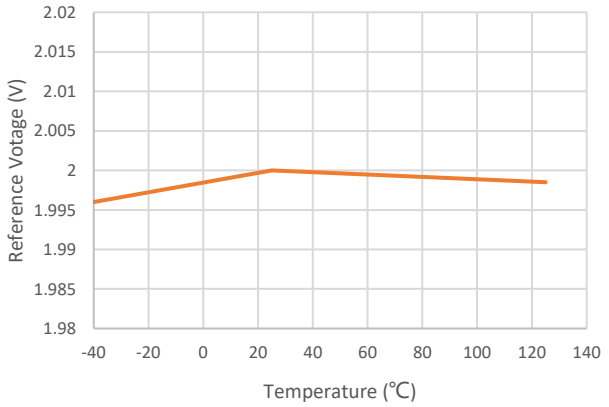


Figure 3. Reference voltage vs Temperature

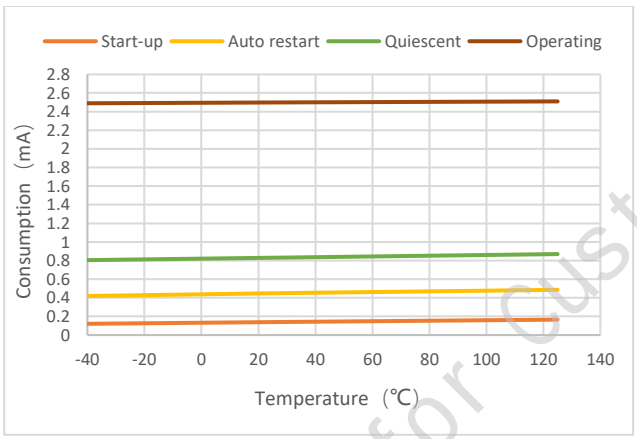


Figure 4. IC consumption vs temperature

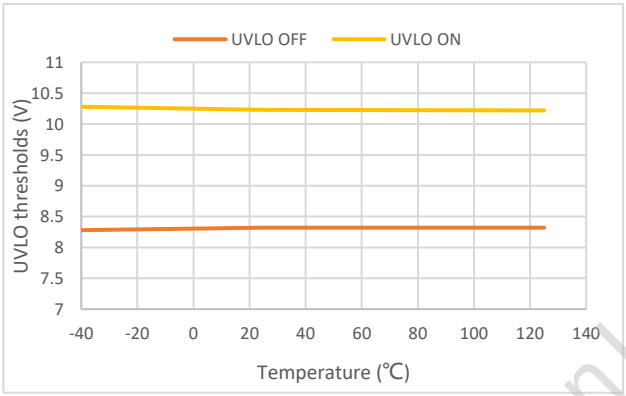


Figure 5. UVLO thresholds vs temperature

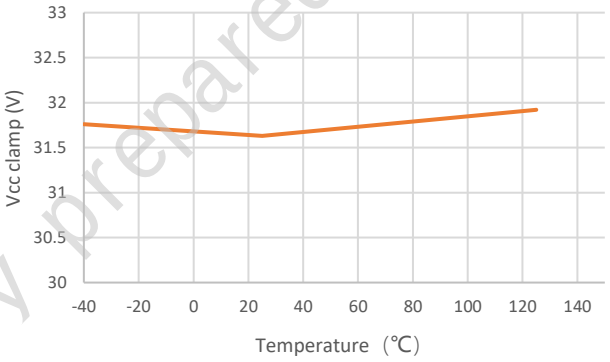


Figure 6. VCC clamp voltage vs temperature

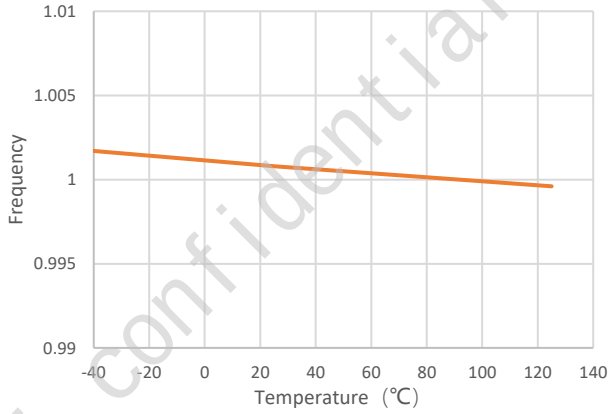


Figure 7. Frequency vs temperature

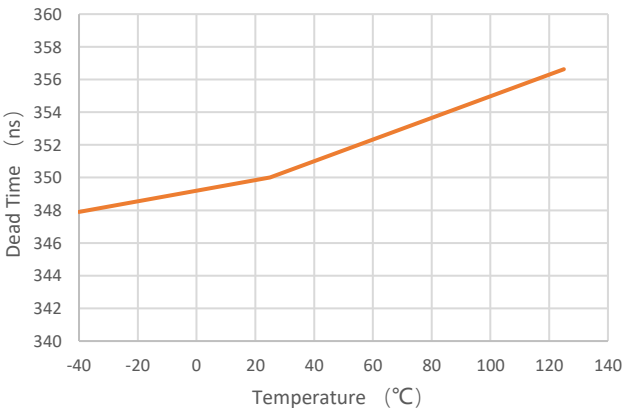


Figure 8. Dead time vs temperature

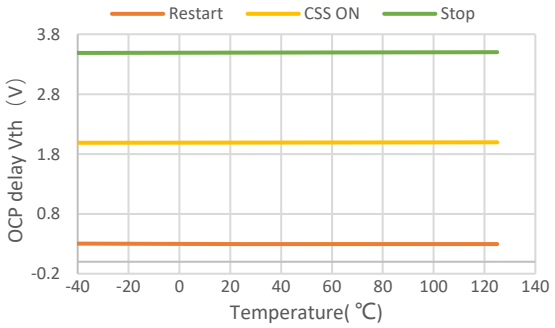


Figure 9. OCP delay thresholds vs temperature

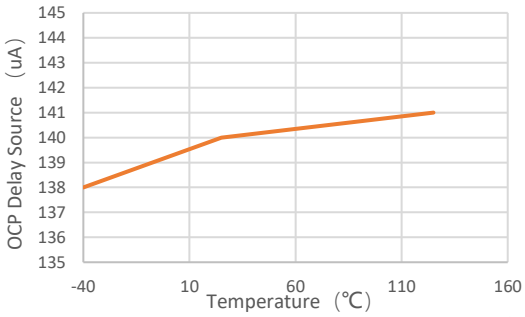


Figure 10. OCP delay source current vs temperature

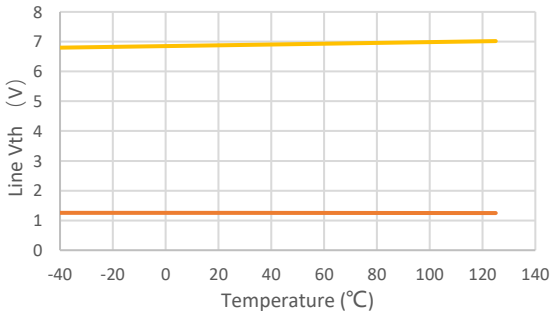


Figure 11. Line thresholds vs temperature

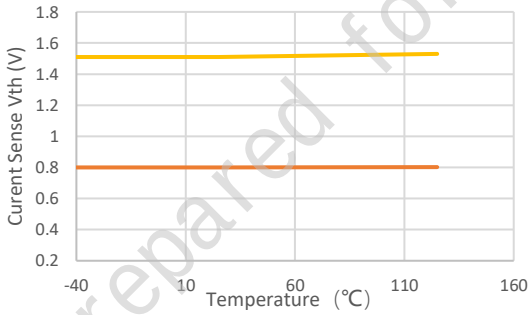


Figure 12. Current sense thresholds vs temperature

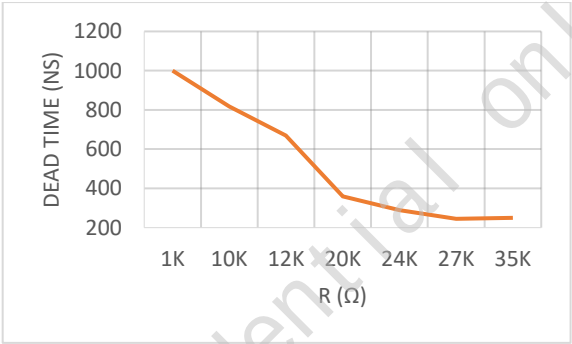


Figure 13. dead time vs Rdt

8. Detailed Description

8.1 Overview

The MK2189/L/D is an advanced double-ended controller specific for resonant half-bridge topology. In these converters the switches (MOSFETs) of the half-bridge leg are alternately switched ON and OFF (180° out of phase) for exactly the same time. This is commonly referred to as operation at "50% duty cycle", although the real duty cycle, that is the ratio of the on-time of either switch to the switching period, is actually less than 50%. The reason is an internally fixed dead-time T_D, inserted between the turn-off of one MOSFET and the turn-on of the other one, so that both MOSFETs are off during this dead time. This dead time ensures the correct operation of the converter, which ensures soft switching and low EMI at high frequency operation.

In order to guarantee the output voltage scaling ratio of the converter, the device must be able to operate in different operating modes, which depend on the load conditions. Variable frequency at heavy load, medium and light load, the relaxation oscillator generates an asymmetrical triangular waveform. At this time, the MOS switch is locked, and the frequency of the waveform is related to load, which modulates the feedback circuit. As a result, the tank circuit driven by the half-bridge accepts the frequency determined by the feedback loop and keeps the output stable. When the load is below a current threshold set by users, i.e. at no load or light load, the system enters burst mode. In burst mode, the controller skips several cycles, and two MOSFETs are kept off for this time duration, so that the equivalent switching frequency is reduced. As the load decreases, the non-switching time duration increases to reduce the switching frequency further. When the converter is completely at no load, the average switching frequency can be reduced to as low as hundreds of Hertz.

In order to meet the different needs of users, three different part numbers are offered.

The main differences between the devices are as follows:

Part NO.	Protection	Startup mode	Ton max	Dead time
MK2189DXAC	Auto-restart	asymmetry	disable	Adjustable dead time
MK2189LXAC	Latch-up	symmetry	disable	Fixed dead time
MK2189XAC	Auto-restart	asymmetry	14us max	Fixed dead time

8.2 Functional Block Diagram

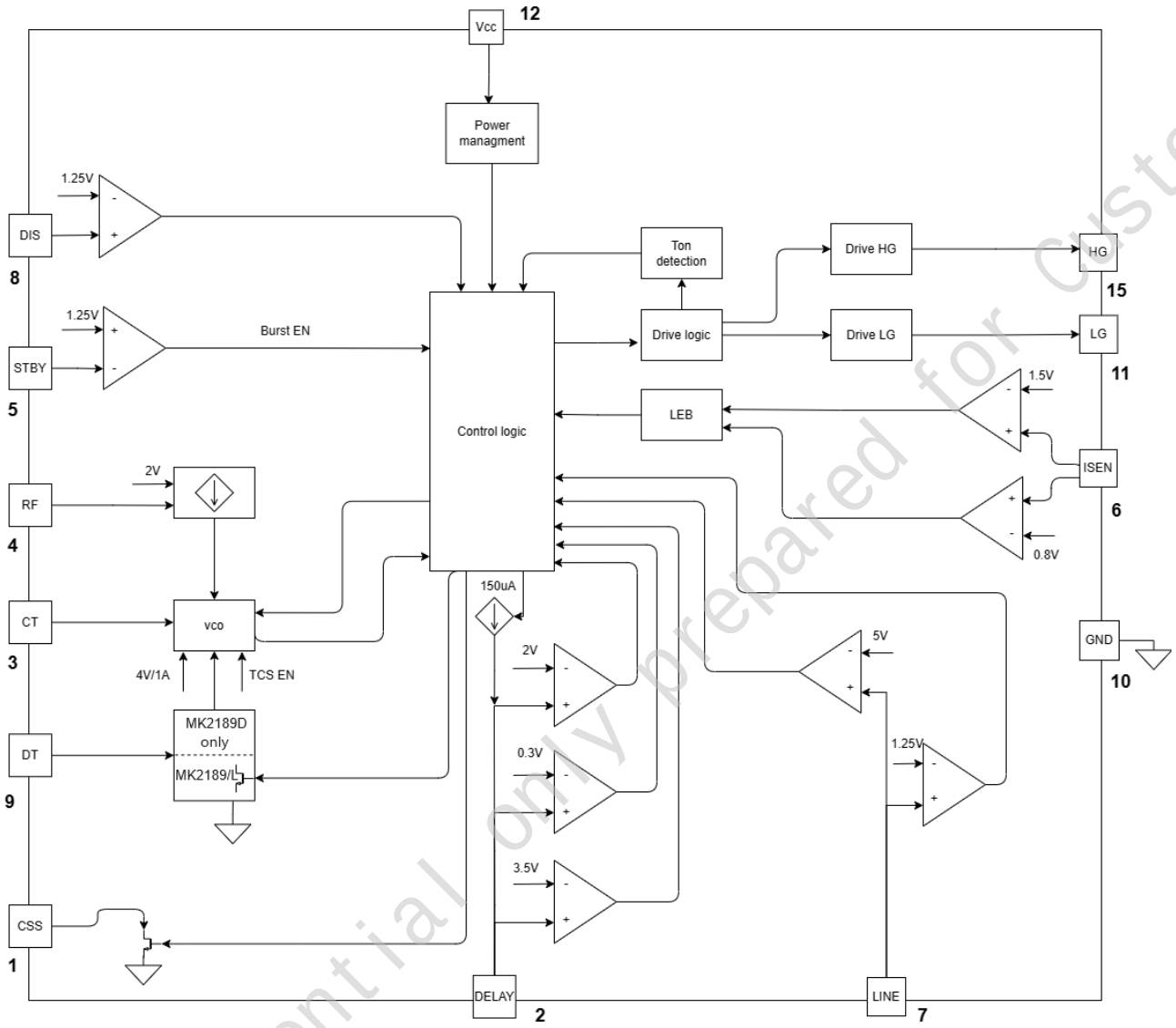


Figure 14. Block Diagram

8.3 Feature Description

8.3.1 Soft-start

In general, the purpose of soft-start is to gradually increase converter's power capability during start-up to avoid excessive inrush current. In resonant converters, the deliverable power depends inversely on frequency, therefore soft- start is done by sweeping the operating frequency from an initial high value until the control loop takes over. The MK2189/L/D converter's initial soft-start frequency can be set with an R-C series circuit from pin 4 RF to ground.

Initially, the capacitor Css is totally discharged, so that the series resistor Rss is effectively in parallel to RF_{min} resistor, and the resulting initial frequency is determined by Rss and RF_{min} only, since the optocoupler's photo-transistor is cut off as long as the output voltage is not too far away from the regulated value:

$$f_{start} = \frac{1}{3 * CF * (RFmin||Rss)}$$

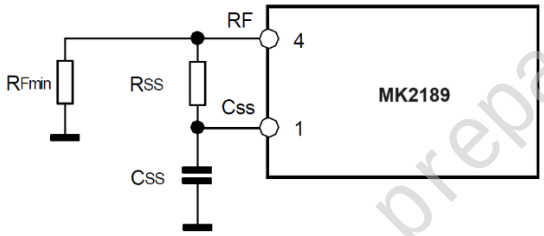


Figure 15. Soft-start circuit

The Css capacitor is gradually charged until its voltage reaches the reference voltage 2V, and the current through Rss goes to zero. This soft-start time generally takes 5 times of Rss·Css time constant. However, before that time, the output voltage will have to get close to the regulated value and the feedback loop taken over, so that it will be the optocoupler's phototransistor to determine the operating frequency afterward. During this frequency sweeping phase, the operating frequency will decrease exponentially to the charges of Css. This counteracts the non-linear frequency dependency of the LLC tank circuit so that converter's power capability changes little as frequency away from resonant frequency and changes very quickly as frequency approaching resonance frequency.

In order to further reduce the high stress, the MK2189/D has optimized its turn on pulses. In the first few cycles, a dedicated Startup Sequence as shown on Figure 16, is used to reduce the stress during start-up.

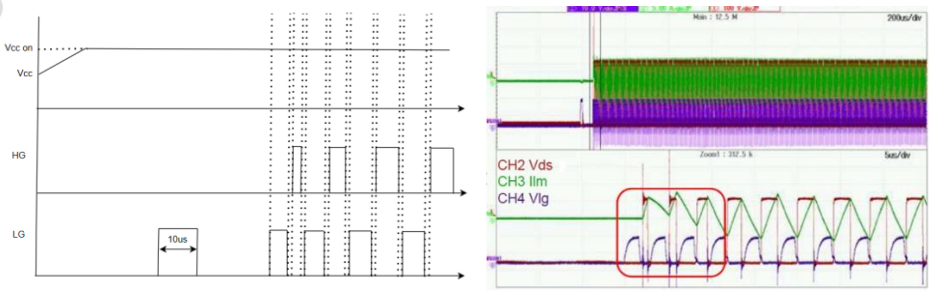


Figure 16. Detailed Dedicated Startup Sequence for MK2189/D

8.3.2 Line sensing function

This function basically stops the IC from switching as the input voltage falls below the specified range, and lets it restart as the voltage rises above the range. The sensed voltage can be either the rectified and filtered main bus voltage or the output voltage of the system's PFC stage. The function works as brownout protection when it senses the main bus voltage, and serves as power-on and power-off sequencing when it is used in systems with PFC pre-regulator front-end.

The MK2189 is turned off with an internal comparator when the input voltage of LINE pin (Pin 7) is below 1.25V reference voltage, as shown in Figure 17. At this under-voltage condition, the soft start is not allowed, and the DT/PFC_STOP pin (Pin 9) is pulled high to stop PFC controller and reduce power consumption of the system. An internal 15uA pull-down current source at Pin LINE is used to program the hysteresis with external resister divider. Once the LINE voltage is above the 1.25V reference, the controller is re-enabled and start switching again. Once the input line's rising threshold V_{INON} and falling threshold V_{INOFF} are designed with hysteresis is equal to V_{INON}-V_{INOFF}, the external resister divider R_H and R_L can be calculated by below equations:

$$R_H = \frac{V_{inon} - V_{inoff}}{15 \cdot 10^{-6}}$$

$$R_L = R_H \frac{1.25}{V_{inoff} - 1.25}$$

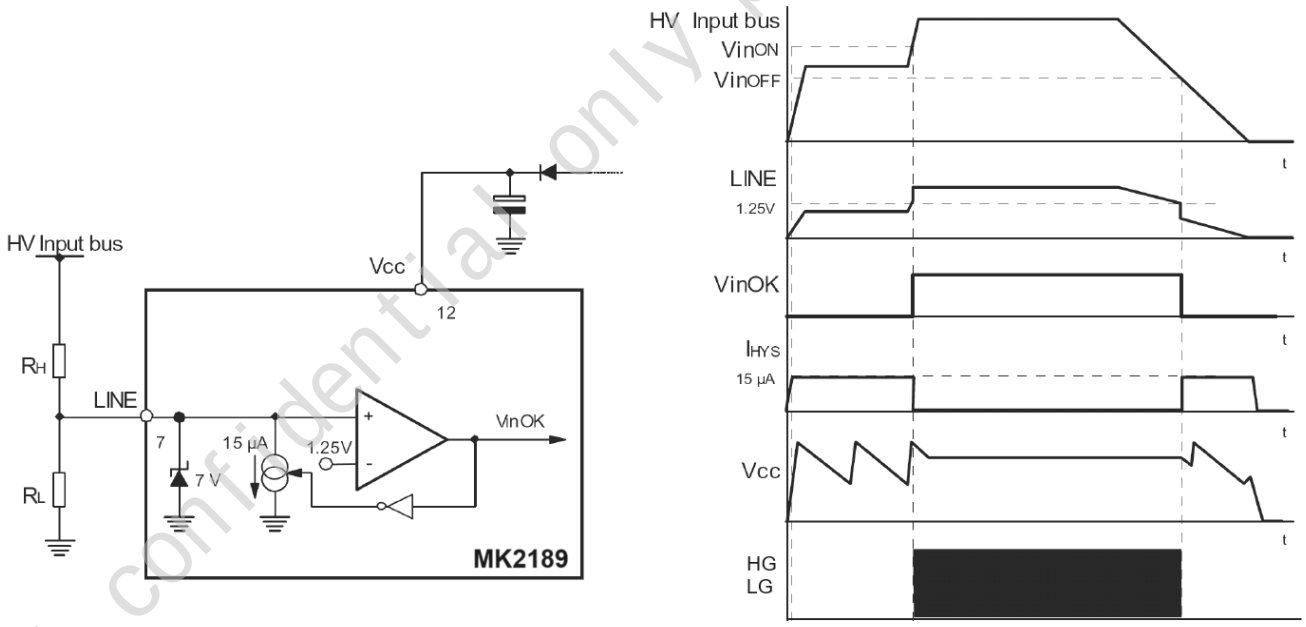


Figure 17. Line sensing function

As an additional safety consideration, MK2189/L/D is shutdown if the voltage on the pin exceeds 7V(TYP). Under normal operations, the resister divider at LINE pin is generally designed with very high values to reduce power consumption. Thus it is prone to pick up noise from such as lightning or ESD events, which falsely turned off the device. It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind from happening. If the function is not used, the pin has to be connected to a voltage greater than 1.3V but lower than 5V.

8.3.3 Oscillator

The oscillator frequency is adjusted externally by a capacitor CF connected from PIN 3 (CT pin) to GND. The capacitor CF is alternately charged and discharged by the network connected to PIN 4 (RF pin). An accurate 2 V reference with about 2 mA source capability is provided internally at this pin. The higher the current sourced by the pin is, the higher the oscillator frequency will be.

The network that loads the RF pin generally comprises three branches:

1. A resistance RF_{min} is connected between this pin and GND, which determines the minimum operating frequency.
2. A resistor RF_{max} connected between this pin and the collector of the (emitter-grounded) photo-transistor that transfers the feedback signal from the secondary side back to the primary side; while in operation, the photo-transistor will modulate the current through this branch - hence modulating the oscillator frequency - to perform output voltage regulation; the value of RF_{max} determines the maximum frequency the half-bridge will be operated at when the phototransistor is fully saturated;
3. An R-C series circuit (CSS + RSS) connected between this pin and ground that enables to set up a frequency shift at start-up. Note that the contribution of this branch is phased-out during steady-state operation.

The operating frequency is approximately calculated based on the below formula.

$$f_{min} = \frac{1}{3 \cdot CF \cdot RF_{min}}$$

$$f_{max} = \frac{1}{3 \cdot CF \cdot (RF_{min} || RF_{max})}$$

After the CF is set in the range of several hundred pF or nF, the values of RF_{min} and RF_{max} will be determined according to the selected oscillator frequency, from the lowest frequency to the highest frequency, within which the voltage should be stabilized.

$$RF_{min} = \frac{1}{3 \cdot CF \cdot f_{min}}$$

$$RF_{max} = \frac{RF_{min}}{\frac{f_{max}}{f_{min}} - 1}$$

In Figure 18, the relationship between the oscillation waveform and the gate drive signal is given.

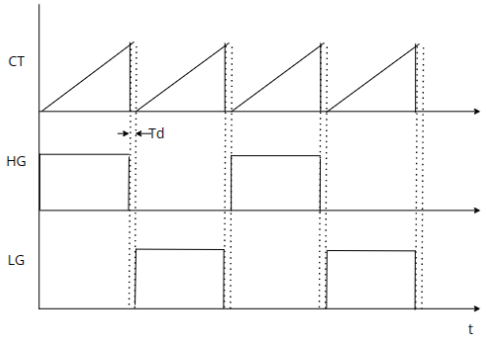


Figure 18. Oscillator waveforms relationship with gate-driving signals

8.3.4 Current Sensing and OCP (ILIM)

The resonant half-bridge is basically a voltage type control, so the current sensing input is only used for OCP protection. Unlike PWM controlled converters, the energy flow is controlled by the duty cycle of the primary switch. In resonant half bridge, the duty cycle is fixed, and the energy flow is controlled by the switching frequency, which also affects the implementation of the current limiting method. In this case, the PWM-controlled transform energy flow can be limited by the termination of switch conduction, which can be limited when the current is detected to exceed the certain threshold. In the resonant half bridge, the oscillator frequency must be increased quickly to be close to switching frequency. At least oscillator frequency change should be seen in the next resonant switching period. That is to say the frequency must be effectively increased in order to increase energy flow effectively. However frequency change rate must be slower than the frequency itself. In this way, the energy flow is limited cycle by cycle so that the primary current information detected by current input signal must be average value. The time must not be too long to let the primary current reaching or exceeding the maximum limited value.
Figure 19 shows a typical application circuit with high efficiency.

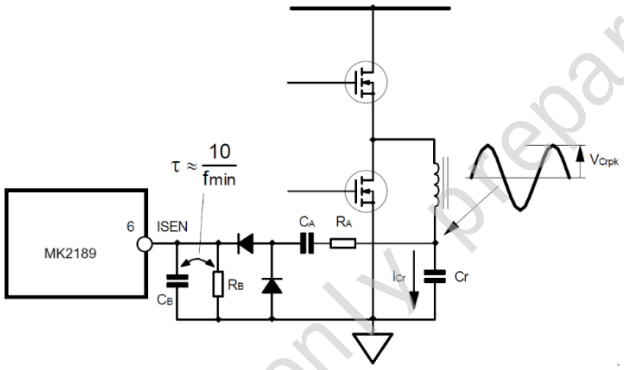


Figure 19. Lossless current sensing technique, with capacitive shunt

The device provides current sensing input pin ISEN (Pin 6) and an over current management function. The ISEN pin is connected to the first comparator referenced to 0.8 V voltage, and the second comparator referenced to 1.5 V. If the voltage at this pin higher than 0.8 V, the first comparator is triggered and the soft capacitor starts to be discharged. This will rapidly increase the frequency of the oscillator, thereby limiting energy transfer. The discharge will continue until the ISEN Pin voltage has dropped by 50mV within the average time of about $10/f_{min}$, and ensure the rise of the effective frequency. When the output of the system is shorted, this operation results in a nearly constant peak primary current.
When the ISEN voltage reaches 1.5V, the second comparator is triggered, and MK2189/D will be shutdown (MK2189L will be latched). Once the device is shutdown, gate drive pins and the DT/PFC_STOP pin are all pulled low too. Since the whole system is turned off.
When the power supply VCC voltage drop below UVLO first and then rise above the starting level, MK2189L can be restarted again.

8.3.5 OVP or OTP protection （DIS pin）

The DIS pin can be used to implement over-voltage protection or over-temperature protection which is realized by an internal comparator with 1.25V reference voltage.

Connected with NTC resistor divider or through the optocoupler sampling output voltage, the system overtemperature protection or overvoltage protection can be realized respectively. When the voltage at this pin is greater than 1.25V, the internal comparator voltage flips, and the controller enters the protection mode. Latch-up or self-recovery is provided by different part numbers to meet customer needs.

Typical application circuit is as follows:

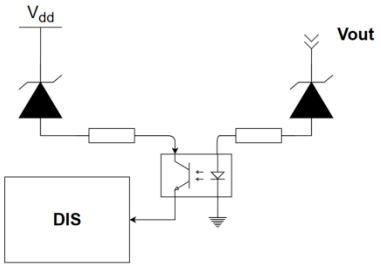


Figure 20. OVP Typical application circuit

9. Application and Implementation

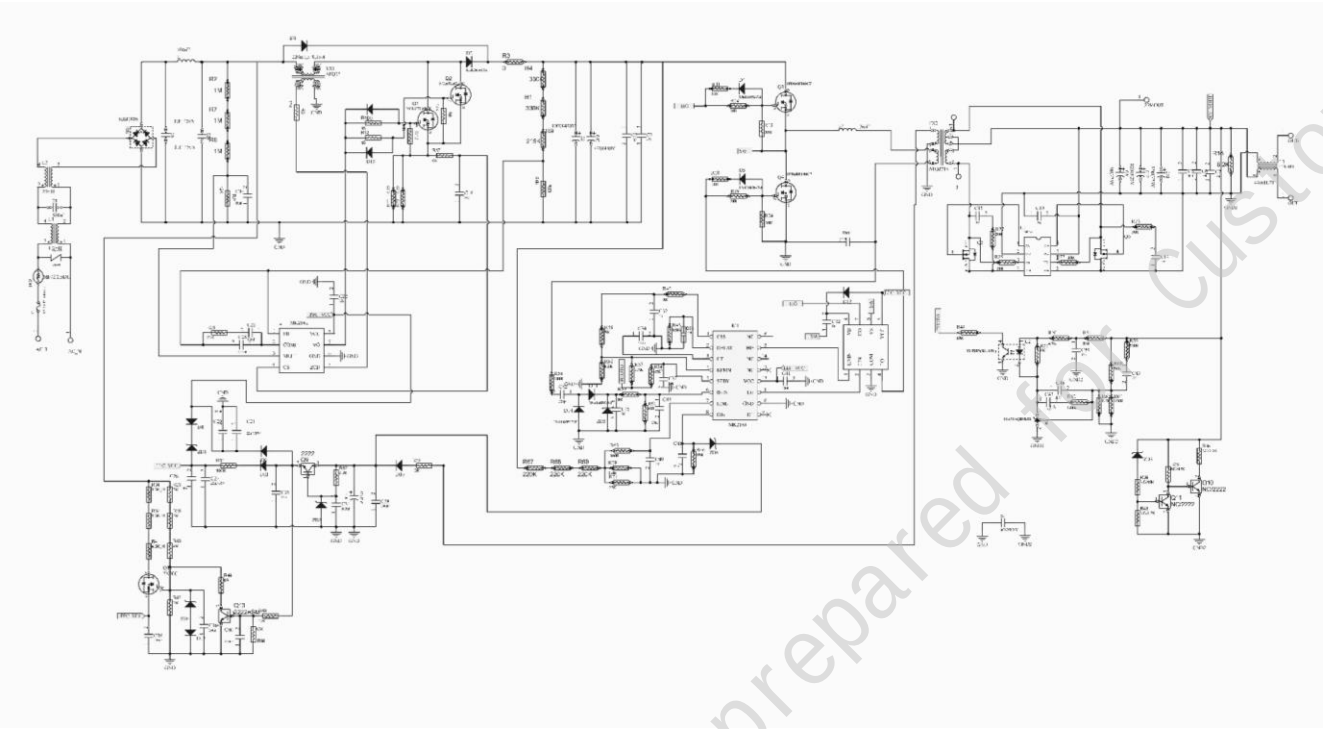


Figure 21. MK2189 Reference Design Circuit

10. Power Supply Recommendations

11. Layout

11.1 Layout Guidelines

To achieve high performance of the MK2189/L/D, the following layout tips should be followed.

- Multi-point grounding, signal ground and power ground need to be separated.
- The two drive signals are differentially traces, and the loop is as small as possible
- The resistances/capacitances of the ISEN, RF and CT pins need to be close to the IC.
- The VCC pin requires an MLCC (typical application:0.1uF) bypass capacitor as close as possible to filter out high-frequency noise.

11.2 Layout Example

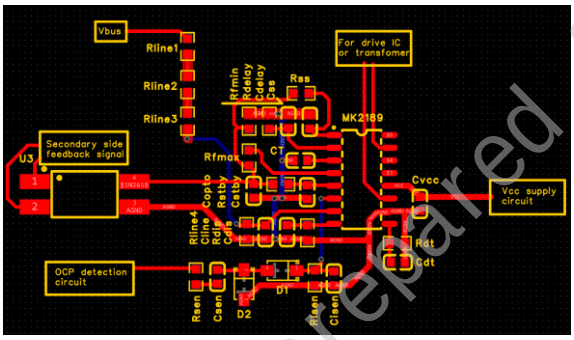


Figure 22. MK2189 Demo Board Layout

12. Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

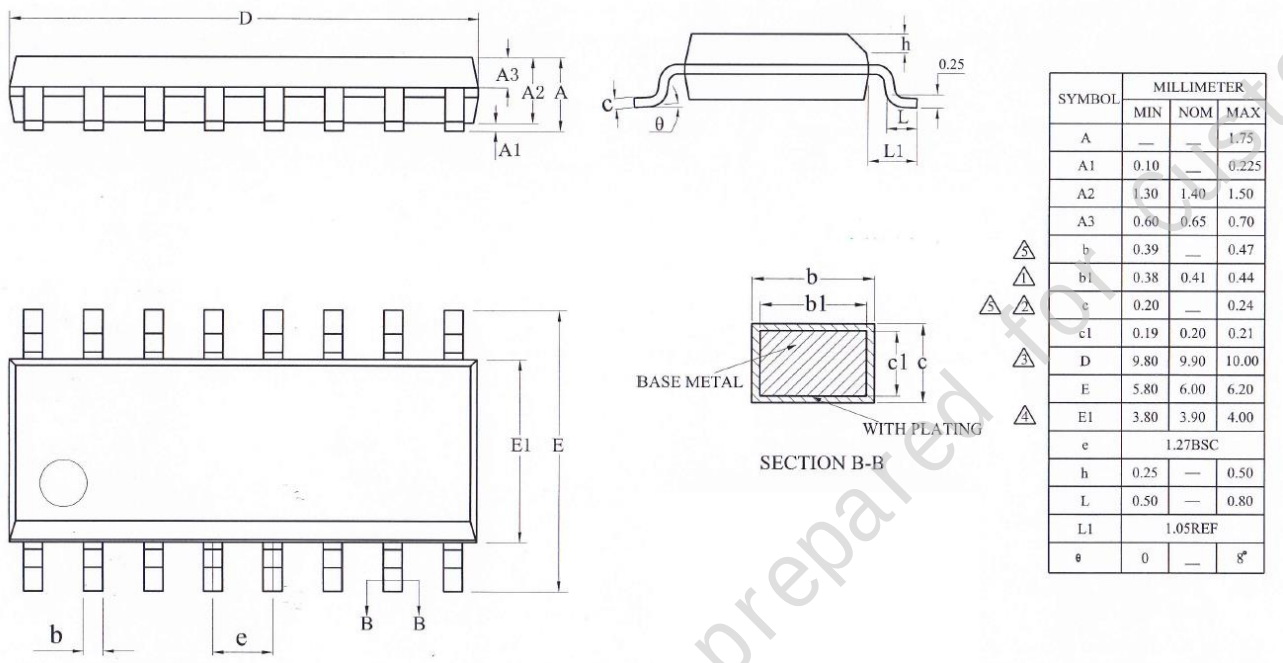
12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13. Mechanical, Packaging

13.1 Package Size



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 23. Package Dimensions

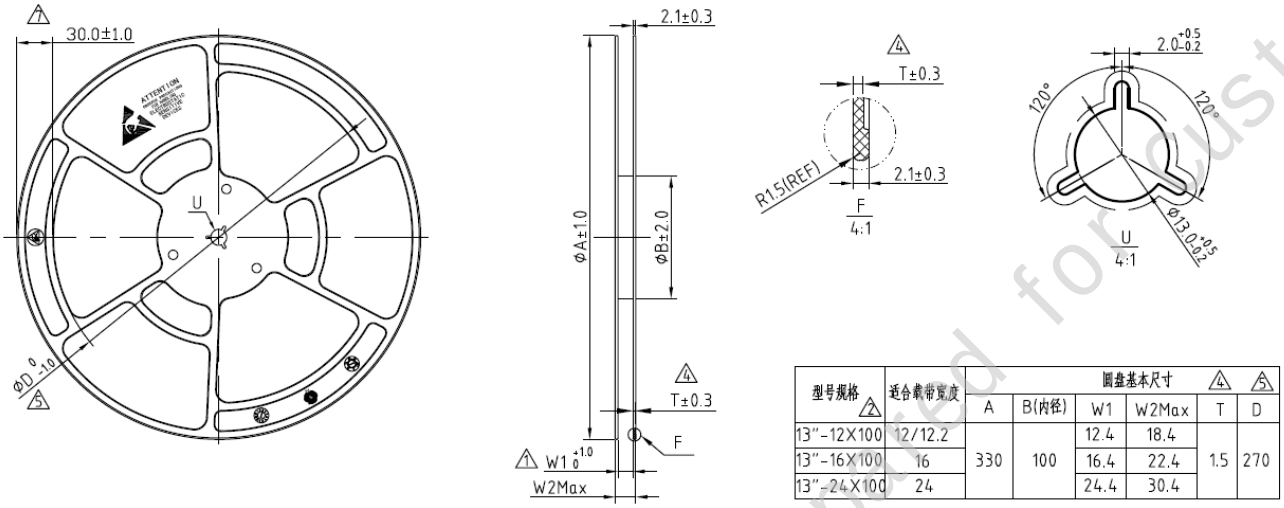
Notes：

(1) This drawing is subject to change without notice.

(2) The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

14. Reel and Tape Information

14.1 Reel and Tape Information



型号规格	适合载带宽度	圆盘基本尺寸					
		A	B(内径)	W1	W2Max	T	D
13"-12X100	12/12.2	330	100	12.4	18.4	1.5	270
13"-16X100	16			16.4	22.4		
13"-24X100	24			24.4	30.4		

Figure 24. Reel Dimensions

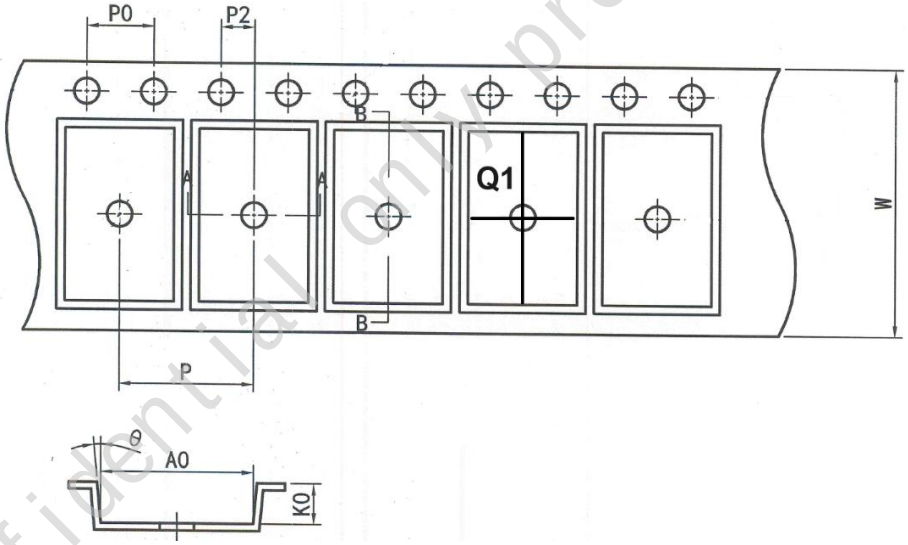


Figure 25. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

Device	Package Type	Pins	Quantities (PCS)	Reel Diameter (mm)	Reel Width W1(mm)	B0 (mm)	A0 (mm)	K0 (mm)	P0 (mm)	P (mm)	W (mm)	Pin1 Quadrant
MK2189 XAC	SOP-16	16	3000	330	16.4	10.4	6.7	2.1	4.0	8.0	16	Q1
MK2189 LXAC	SOP-16	16	3000	330	16.4	10.4	6.7	2.1	4.0	8.0	16	Q1
MK2189 DXAC	SOP-16	16	3000	330	16.4	10.4	6.7	2.1	4.0	8.0	16	Q1

15. Tape and Reel Box Dimensions

15.1 Reel Box Dimensions

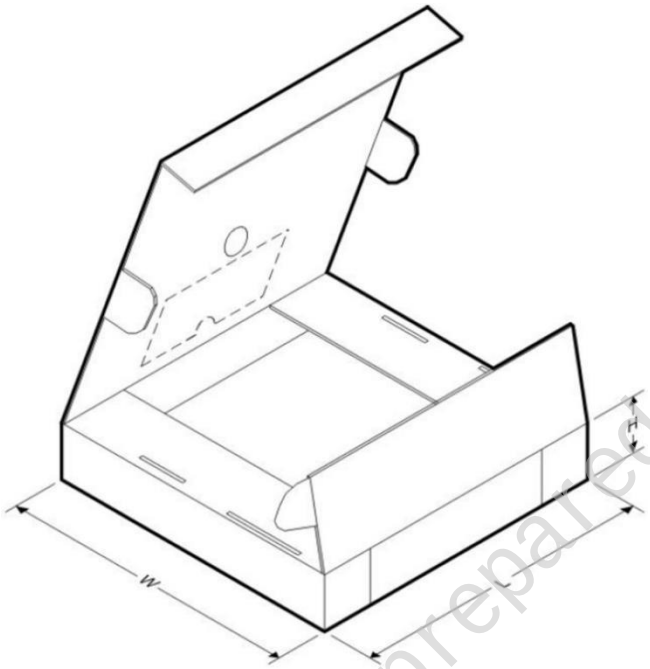


Figure 26. Rell Box Dimensions

Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MK2189XAC	SOP-16	16	6000	353	340	60
MK2189LXAC	SOP-16	16	6000	353	340	60
MK2189DXAC	SOP-16	16	6000	353	340	60