High Efficiency Offline PWM Controller with Wide VCC Range

1. Descriptions

MK2687V is a multi-mode PWM controller optimized for PD/fast charging applications. Its wide VCC operating voltage range allows it to cover the output range of PD/PPS from 3.3V-23V without using additional windings or linear step-down circuits.

In response to energy efficiency requirements, since PD/fast charging has multiple different output voltages, adaptive multi-mode is adopted. It adjusts to work at DCM/QR/CCM under different loads and different outputs. Under light load, it will work in burst mode to improve efficiency. Its maximum switching frequency is up to 65 kHz.

MK2687V provides comprehensive protection functions, including output overvoltage protection, VCC over voltage protection, overpower protection, brown in/out and secondary side SR short circuit protection, pin OPEN/SHORT protection.

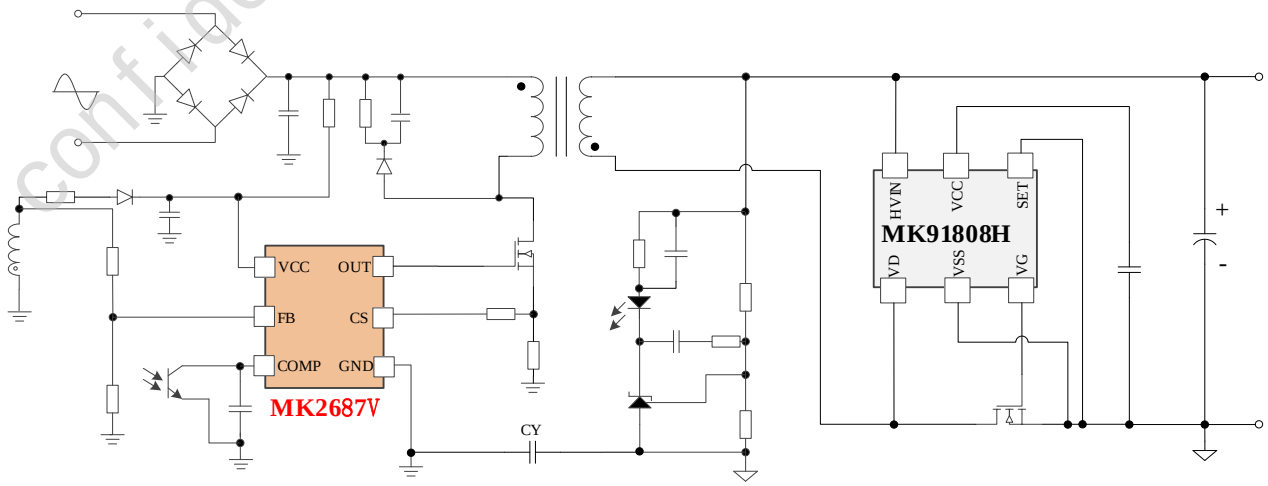
2. Features

- Wide range VCC operating voltage (10V-88V)
- Multi-mode control for different output voltages and loads
- Proprietary soft-start circuit reduces SR Vds stress
- Optimized efficiency easily meets energy efficiency labeling
- Over power protection
- Brown in/Brown out function
- VCC over voltage protection / Vout over voltage protection
- Secondary side SR short circuit protection
- External OTP setting protection
- Support PPS wide range output
- SOT23-6 package

2. Typical Application

- AC/DC PD adapter
- AC/DC general power supply

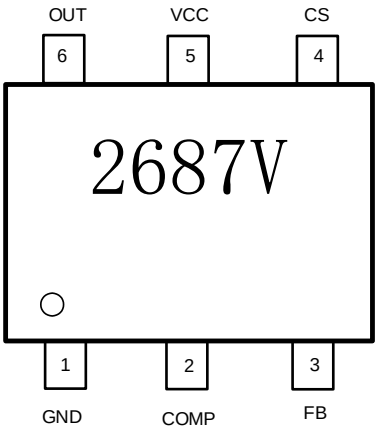
4. Simplified Application



5. Order Information

Order code	Description
MK2687VGSA	SOT23-6, tape and reel, 3000 pieces/reel

6. Pin Package



SOT23-6

6.1 Absolute Maximum Ratings (1)

VCC ……– 0.3 V to +100 V

COMP, FB……–0.3V to +5.5 V

CS…… -0.7V to + 5.5V

OUT…… –0.3V to +20 V

Operating junction temperature -40 ℃ to + 155 ℃

6.2 Recommended Operations conditions

VCC …… 10 V to 88V

Maximum junction temperature (T_J)..... +125 °C

6.3Thermal Resistance (2) θ_{JA} θ_{JC}

SOT23-6 .....100 66 °C/W

Notes:

(1) Exceeding this range may damage the device

(2) Measured on JESD51-7, 4 layers PCB

7. ESD Performance

		Value	Units
ESD parameter V_{ESD}	Human Body Model (HBM), all pins tested in accordance with ANSI/ESDA/JEDEC JS-001 test standards (1)	± 2000	V
	Component Charging Model (CDM), according to JEDEC JESD22-C101 standard tests all pins (2)	± 1000	V

Notes:

(1) According to the JEDEC JEP155 standard requirements, the Human Body Model (HBM) ESD level required for standard safety production is 500V

(2) According to the JEDEC JEP157 standard requirements, the component charging model (CDM) ESD level required for standard safety production is 250V

8. Electrical Parameters

Unless otherwise specified, T_A =25 °C, VCC=13V.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply (VCC pin)						
UVLO under voltage protection turn-on voltage	V_{CC_ON}	VCC rises to turn on	15.5	17	19.5	V
UVLO under voltage protection shutdown voltage	V_{CC_OFF}	VCC drops to turn off	6	7.2	8.5	V
UVLO under voltage protection hysteresis (1)	V_{CC_HYST}			10		V
VCC startup current	$I_{STARTUP}$		2	5	10	uA
VCC normal operating current	I_{OP}	COMP=2V, FB pin pull 150uA, CS=1V, OUT=1nF to GND	1	1.4	2.5	mA
Burst working mode current	I_{BURST}	COMP=0V, OUT=1nF to GND	200	280	400	uA
VCC hold threshold	V_{CC_HOLD}		7	8.3	9.5	V
VCC over voltage protection threshold	V_{CC_OVP}		89	93		V
VCC clamp threshold	V_{CC_CLAMP}			103		V
VCC latch voltage	V_{CC_LATCH}		3	4	5	V
Closed loop control (COMP pin)						
COMP open loop voltage	V_{COMP_OP}	COMP pin open circuit		4.4		V
COMP short circuit current	I_{COMP_SHORT}	COMP =0V	100	150	250	uA

Burst mode entry threshold	V_{BM_ET}		0.27	0.3	0.4	V
Burst Mode hysteresis voltage	V_{BM_HY}		0.02	0.05	0.09	V
OPP over power protection threshold	V_{OPP}		2.7	3	3.3	V
OPP deglitch time (1)	T_{D_OPP}			Tss *6		ms
The ratio of COMP to CS	A_{VCS}		2.3	2.5	2.7	V/V
Slope compensation voltage	V_{SLOPE}	Duty =75%	0.2	0.3	0.4	V
Current detection part (CS pin)						
Soft start time	T_{SS}		4	7	10	ms
Leading edge blanking time	T_{LEB}			330		ns
Rectifier short circuit protection threshold (OC FAULT)	V_{SR_SH}		1.1	1.2	1.3	V
Rectifier short circuit protection triggering period (1)	$T_{SR\ -SH}$			3		Cycles
Cycle by cycle maximum current limit	V_{CS_CBC}		0.75	0.77	0.79	V
Auxiliary winding voltage detection (FB pin)						
Valley detection current threshold	I_{FB_VALLEY}			10		uA
Brown in current threshold	I_{BNI}		82	94	99	uA
Brown out current threshold	I_{BNO}		74	85	93	uA
Brown out blanking time (1)	T_{BL_BNO}			Tss *7		ms
Output over voltage protection threshold	V_{FB_OVP}		3.45	3.6	3.7	V
Output over voltage protection blanking time (1)	T_{BL_OVP}			7		Cycles
Output short circuit protection threshold	V_{FB_ST}		0.15	0.2	0.25	V
Output short circuit protection shielding time (1)	T_{BL_ST}			7		Cycles
FB sampling time	T_{SAMPL}	CS=0.5V		1.5		us

FB high judgment threshold	V_{FB_H}		1.7	1.9	2.1	V
FB medium judgment threshold	V_{FB_M}		0.9	1	1.1	V
Driver section (OUT Pin)						
Driver low level voltage	V_{G_L}			0.2	0.5	V
Driver high level voltage	V_{G_H}	VCC=13 V, OUT Load=20mA	8			V
Driver high level clamping voltage	V_{G_HC}	VCC=V_{CC_OVP}		11		V
Driver rising time	T_R	Cload =1nF		210		ns
Driver falling time	T_F	Cload =1nF		30		ns
Control section						
Normal operating frequency	F_{SW_NOM}		60	65	70	kHz
Energy saving mode working frequency	F_{SW_GREEN}			25		kHz
Frequency jitter range (1)				±6		%
Frequency jitter period (1)				8		ms
Maximum duty cycle	D_{MAX}		74	77	80	%
Over temperature protection (1)	T_{HSD}			155		℃
Over temperature protection hysteresis (1)	T_{HSD_HYS}			30		℃

Note:

(1) Values are verified by characterization on bench, not tested in production.

9. Pin Function

Pin number	Pin name	Description
1	GND	Ground reference
2	COMP	Voltage feedback input pin
3	FB	Auxiliary winding voltage detection pin
4	CS	Current sense input pin
5	VCC	Power supply
6	OUT	Drive output pin

10. Internal Functional Block Diagram

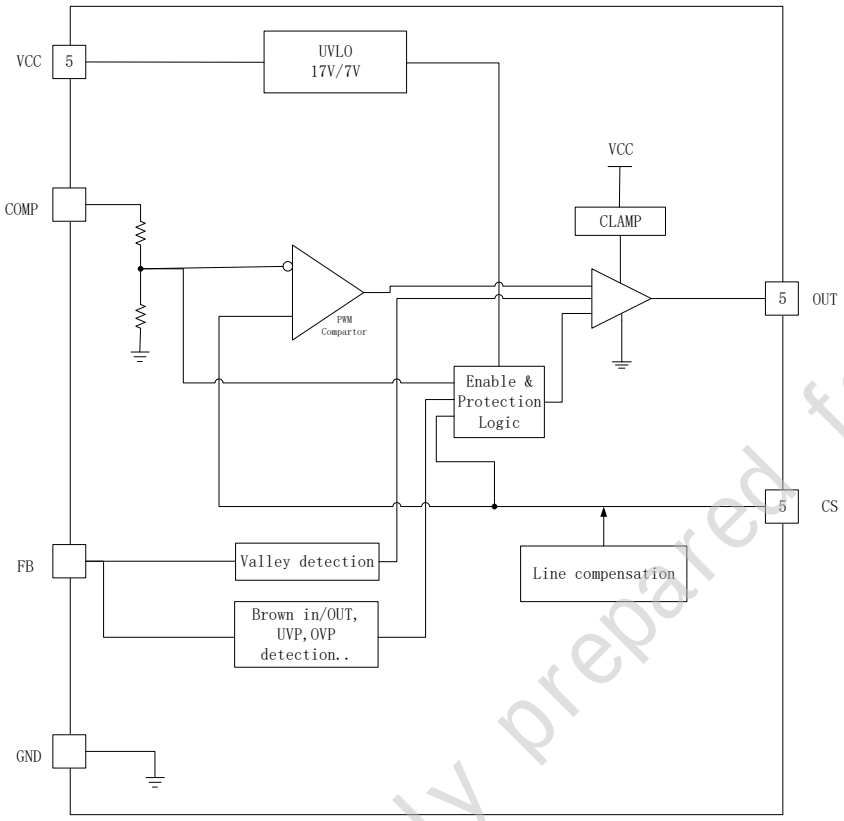


Figure 1 Internal functional block diagram

11. Function Description

Power Supply Starts

During startup, the bus capacitor charges the chip's VCC via the startup resistor. Since the startup current of the chip is very small (approximately 5μA), a larger resistance can be selected to minimize standby losses. Additionally, startup delay should also be considered when selecting the resistance value. Once VCC reaches the turn on voltage (V_{CC_ON}), the chip begins to emit pulses.

Soft Start

During the start-up process, because the output voltage is very low, if the frequency and CS voltage are not controlled, the chip will try to operate at the maximum switching frequency and maximum peak current due to the effect of the loop, which will cause the system to operate at a very deep CCM, bringing higher stress on the primary and secondary sides. MK2687V adopts multi stage control to optimize the primary and secondary stress during startup.

Operating Curve

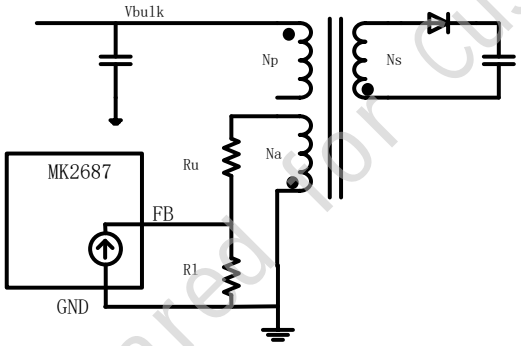
For PD applications, the chip has different operating frequency curves at different output voltages. The chip detects the FB pin voltage during the secondary side freewheeling period to determine the output voltage and adopts different frequency curves to optimize the efficiency at each output voltage point.

In order to improve the EMI impact, the chip also employs a dithering technique, where the frequency is distributed within a ±6% range.

Input Under Voltage Recovery (Brown In)

During the power on process, the PWM controller sends out a series of narrow pulses, in which the Brown in detection is completed. During the turn-on process of the primary MOSFET, the voltage of FB pin is about 0V. At this time, the current flowing out of the FB pin = (V_{BULK}*Na)/(Ru*Np). Only when this current is greater than I_{BNI}, the chip will consider that the Brown in condition has been met and start up normally.

If the brown in condition is not met, the chip enters the restart process after the narrow pulses



Input Under Voltage (Brown Out)

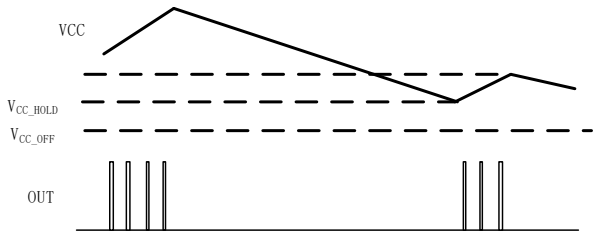
During normal operation, the chip is always in the primary side MOS opening process, detecting the outflow FB current. When the outflow current < I_{BNO} and the duration ≥ T_{BL_BNO}, the bus voltage is considered under voltage, it will turn off the driver. The chip enters the restart process.

VCC Hold

When operating under a particularly light load with an extremely low output voltage, the VCC voltage approximates Na*Vo/Ns. Should the switching frequency be significantly low, VCC voltage may decrease substantially. To address this, the chip includes a power supply hold mode. This mode activates when VCC voltage falls to the V_{CC_HOLD} threshold, compelling the chip to generate pulses to prevent VCC from dropping into the shutdown range. Due to these forced pulses, VCC voltage will begin to rise again. Once it reaches approximately 9.5V, the chip will cease forced pulsing.

However, in system design, it is preferable to maintain the VCC voltage consistently above V_{CC_HOLD} by optimizing the VCC capacitance, the turns ratio of the auxiliary winding, and the minimum load. This strategy helps avoid the

activation of the power supply hold mode, which can disrupt loop regulation and cause the output voltage to increase, potentially increasing ripple.



Control Mechanism

MK2687V is current mode PWM controller with cycle-by-cycle current limit. The switching current is detected by a sense resistor at CS pin. An internal leading edge blanking circuit with blanking time (T_{LEB}) blocks the sensed voltage spikes at initial power MOSFET ON state due to snubber diode reverse recovery and surge gate current at power MOSFET. The maximum cycle-by-cycle current limit is set by V_{CS_CBC}/R_{CS}.

MK2687V also clamps the maximum duty cycle to D_{MAX}. Once the D_{MAX} duty cycle is reached, the output turns off.

Input Line Compensation

MK2687V uses the detected input line voltage through the current at FB pin (I_{FB}) to generate the Iccs current going out of CS pin with external line compensation resistor R_{LR} to achieve more constant actual peak current regardless of line voltage.

Internal Slope Compensation

The chip includes built in slope compensation circuitry, which adds a linear ramp to the current sense input voltage. This ramp is proportional to the duty cycle and is used for PWM (pulse width modulation) generation. This feature significantly enhances closed loop stability when operating in continuous conduction mode (CCM). It also prevents subharmonic oscillation, which in turn reduces output ripple.

Voltage Feedback Loop

The COMP pin serves as the voltage loop feedback input and is connected to the output of a TL431 voltage reference via an optocoupler. It functions by comparing this feedback voltage with the current signal to generate the drive signal for the circuit.

For optimal loop performance and easier debugging, it is recommended to place a ceramic capacitor in parallel with the resistor that is connected in series with the diode on the secondary side of the optocoupler. This configuration can help stabilize the feedback signal and improve the overall response of the feedback loop.

Auxiliary Winding Voltage Detection (FB Voltage Detection)

During the freewheeling phase of the secondary side current, the voltage on the FB pin represents a fractional voltage from the auxiliary winding. This fraction indirectly reflects the output voltage. The FB voltage is sampled during the transformer's demagnetization period and compared against predefined thresholds to enable several critical functions:

Output Over Voltage Protection

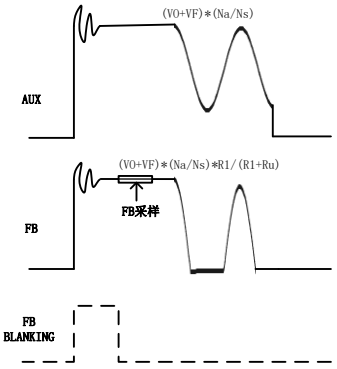
If the FB voltage exceeds V_{FB_OVP}, the output over voltage protection is triggered to safeguard against excessively high voltages.

Output Under Voltage Protection (Or Output Short Circuit Protection)

If the FB pin is lower than V_{FB_ST} for seven consecutive cycles, protection occurs, and the chip enters restart.

Efficiency Optimization

The detected output voltage and comp voltage determine the control curve, optimizing the system's efficiency based on real time operational conditions.



Valley Switching

After secondary side rectification process is done, the drain voltage starts oscillating with a frequency of approximately $1/2\pi\sqrt{(Coss \times Lp)}$, where Lp is the inductance of primary winding of the transformer and C_{OSS} is capacitance on the drain of primary MOSFET. When the oscillation ringing is below 0V at auxiliary winding, the chip clamps FB pin to ~0V, and senses the current at FB pin. When the current out of FB reaches a design value, a "possible" valley is locked and MK2687V turns on after propagation delay.

Protective Function

Reliable power supply system is achieved with protections including cycle by cycle current limit and over power protection, output over voltage protection, VCC over voltage protection, output under voltage protection, CS short circuit protection, synchronous rectifier short circuit protection, output short circuit protection etc. The behavior after protection is referred to in the following table. Detailed protection features are described in the following sessions.

MK2687V protection function	MK2687V protection mechanism
Over power protection	Restart
Output over voltage protection	Latch off
VCC over voltage protection	Latch off
CS short circuit protection	Restart
Synchronous rectifier short circuit protection	Latch off
Output short circuit protection	Restart

Over Power Protection (OPP)

The chip implements over power protection (OPP) by monitoring the voltage at the COMP pin. If the COMP voltage exceeds the set over-power threshold (V_{OPP}) and remains above this threshold for a duration longer than six times the soft-start time (T_{SS} * 6), the chip interprets this condition as an overload situation. In response, OPP is activated, and the chip initiates a restart process to prevent damage and ensure safe operation.

Cycle By Cycle Current Limit

The current mode control IC compares the CS signal with the COMP cycle by cycle, but when the output is short circuited or the optocoupler is open, the COMP voltage may rise extremely high, resulting in excessive I_{PK} current and causing transformer saturation. Therefore, the chip adds an addition protection level, the CS voltage will be compared with V_{CS_CBC} (~0.77V) cycle by cycle. After the blanking time T_{LEB}, as long as the CS reaches V_{CS_CBC}, the chip will chop drive signal immediately.

Secondary Side SR Short Circuit Protection (SSCP)

In the event of a short circuit in the secondary side synchronous rectifier, the peak current through the power MOSFET increases sharply upon activation. To address this, the chip is designed for rapid response. When the CS pin detects a voltage exceeding the predefined V_{SR_SH} threshold, the current sense blanking time is immediately reduced to 90ns. This allows the power MOSFET to be turned off instantaneously within the same switching cycle. If such conditions persist across three consecutive switching cycles, the chip activates its latch off SSCP mode to safeguard the system effectively.

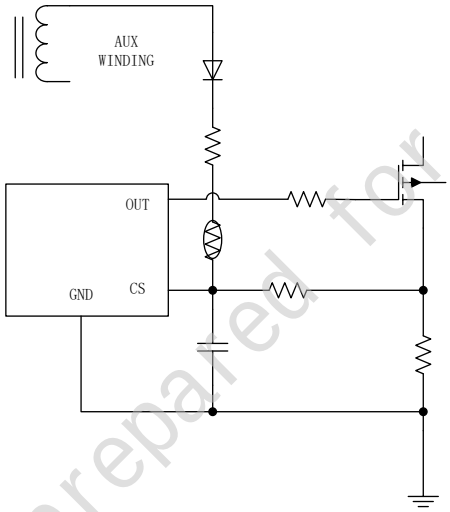
VCC Over Voltage Protection

When VCC reaches V_{CC_OVP}, the chip immediately stops driving output and latch off.

Over Temperature Protection (OTP)

The chip features built-in over-temperature protection that activates at a preset threshold temperature (T_{HSD}) and includes a hysteresis temperature (T_{HSD_HYS}) to prevent frequent toggling of the protection state.

Additionally, customers can enhance OTP by integrating an external Negative Temperature Coefficient (NTC) resistor into the CS pin circuit. As the board temperature increases, the resistance of the NTC resistor decreases. Should the voltage at the CS pin (V_{CS}) exceed the critical baseline value (V_{CS_CBC}) and this condition persists for fifteen consecutive cycles, the OTP is triggered. Following this, the chip initiates a latch off process to protect the system under excessive temperature conditions.

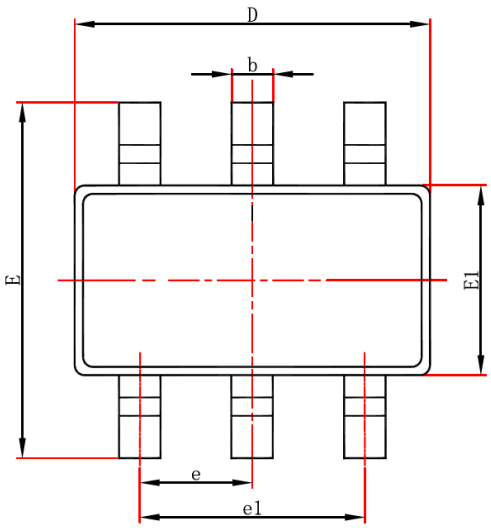


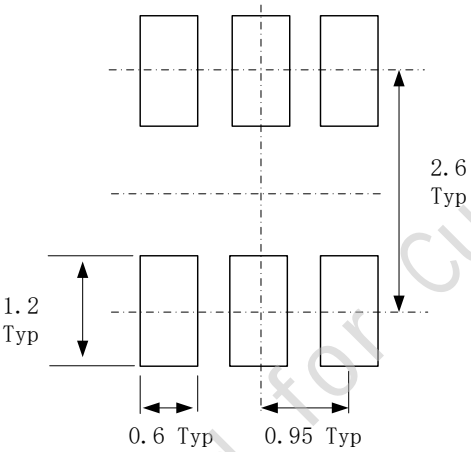
Other Protection Features

There are several critical protections designed in the MK2687V to prevent the power supply at fault state. In case listed below, MK2687V will trigger protection:

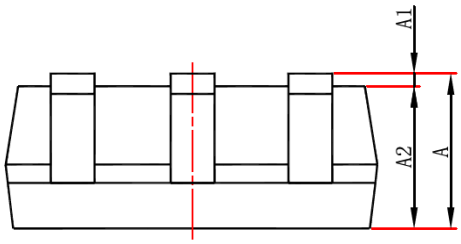
1. Adjacent Pins short
2. Pins open
3. CS short

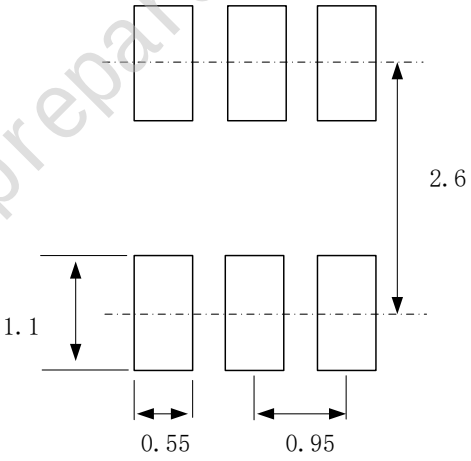
12. Package Size (SOT23-6)



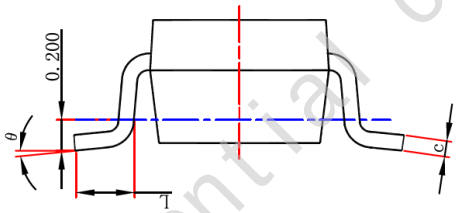


Recommended Land Pattern





Recommended Stencil Openings



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°